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A Temperature Compensation Method by Adjusting Gamma Voltages for High Luminance Uniformity of Active Matrix Organic Light-Emitting Diode Displays

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ABSTRACT In this paper, a temperature compensation method is proposed for active-matrix organic light-emitting diode (AMOLED) displays to achieve high luminance uniformity over a wide operating temperature range. The proposed temperature compensation method compensates for variation in OLED luminance according to temperature by adjusting the gamma voltages. To verify the proposed method, a built-in test circuit, which includes temperature sensors, current calculation block, current adjustment block, and gamma voltage generator, was fabricated using 90 nm complementary metal-oxide semiconductor process technology with 6 V high-voltage devices. The measurement results show that the proposed method achieves a high luminance uniformity with an OLED luminance variation of less than 1.54 cd/m^2 over the temperature range of −45°C to 60°C. Therefore, the proposed temperature compensation method is suitable for AMOLED displays requiring high luminance uniformity.

INDEX TERMS Organic light-emitting diode (OLED), temperature compensation, high luminance uniformity, gamma voltage.

I. INTRODUCTION

Active matrix organic light-emitting diode (AMOLED) displays have been widely used for small mobile devices including smartphones, smartwatches, head-mounted displays, and smart glasses to large-sized televisions. Recently, these displays have been developed to realize augmented reality (AR) and virtual reality (VR) applications. Compared to liquid crystal displays, OLED displays are more suitable for AR and VR applications because of their high contrast ratio, fast optical response, and excellent color reproducibility [1]–[4]. Particularly, outdoor AR and VR applications are used in a wide operating temperature range.

However, OLED luminance varies according to temperature, which increases due to increased OLED efficiency as the temperature increases [5]–[8]. Therefore, a driving method that can compensate for variation in OLED luminance according to temperature is necessary to achieve high luminance uniformity of the OLED over a wide operating temperature range.

Conventional AMOLED displays mainly compensated for OLED degradation [9], [10], and variations in threshold voltage and mobility of the backplanes [10], [11], such as thin-film transistors (TFTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs). However, these displays could not properly compensate for variation in the OLED luminance according to the temperature. The external compensation method in [9], [10] compensated for OLED degradation and variations in threshold voltage and mobility of the TFT. However, they could not sufficiently compensate for variation in the OLED luminance only by sensing the

anode voltage of the OLED, which could not fully represent the OLED luminance [7]. The internal compensation method in [11] compensated for variation in the threshold voltage of the MOSFET, but only for variation in specific OLED efficiency in a pixel structure, and thus could not accurately compensate for variation in the OLED luminance according to the temperature when the OLED efficiency varies.

In this paper, a temperature compensation method is proposed for AMOLED displays to achieve high luminance uniformity over a wide operating temperature range. The proposed temperature compensation method compensates for variation in the OLED luminance according to the temperature by adjusting the gamma voltages. Section II describes the proposed temperature compensation method along with the OLED luminance and efficiency, and the I-V characteristic of the MOSFET according to the temperature. In addition, the operation principle of the proposed temperature compensation method is explained with flowchart and block diagram. In Section III, the measurement results using a fabricated built-in test circuit are analyzed and compared with previous works to verify the proposed temperature compensation method. Finally, conclusions are given in Section IV.

II. PROPOSED TEMPERATURE COMPENSATION METHOD

A. OLED LUMINANCE AND EFFICIENCY AND I-V CHARACTERISTIC OF THE MOSFET ACCORDING TO TEMPERATURE

Fig. 1 shows the measurement results of white OLED luminance in the temperature range from −45°C to 60°C, representing that the OLED luminance increases as the temperature increases. Here, the OLED luminance is closely related to the OLED efficiency [5]–[8]. The OLED efficiency can be represented as quantum efficiency comprising the external quantum efficiency (η_{ext}) and internal quantum efficiency (η_{int}). The external quantum efficiency [5]–[6] is expressed as

$$\eta_{ext}(T) = \eta_{int}(T)\eta_{out} = \eta_r(T)\phi_f \chi \eta_{out}, \tag{1}$$

where η_{out} is an out-coupling efficiency, η_r is the ratio of the number of exciton formation events within an OLED device to the number of electrons, φ_f is the fluorescence quantum efficiency, χ is the fraction of excitons formed as singlets, and T is an absolute temperature. In addition, η_r is determined by the charge injection and the recombination of the electrons and holes, which are affected by the mobility. The mobility increases as the temperature increases due to increased hopping speed [5]–[8], which is thermally activated at high temperature. Therefore, the OLED efficiency increases as the temperature increases.

To achieve high luminance uniformity of the OLED over a wide operating temperature range, the current of the MOSFETs in a pixel, which drives the OLED, should be reduced since the OLED efficiency increases as the temperature increases. The drain current of the p-channel MOSFET

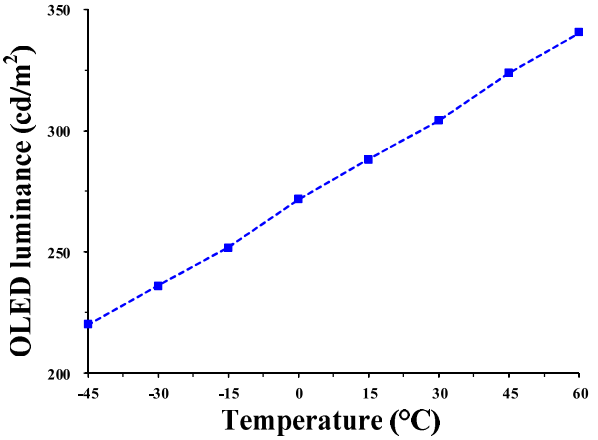

FIGURE 1. Measurement results of white OLED luminance in the temperature range from −45°C to 60°C under the OLED bias condition of 3.3 V.

(I_D) can be expressed as [12]

$$I_D(T) = \frac{1}{2}\mu\left(\frac{T}{T_{NOM}}\right)^{UTE} C_{ox}\frac{W}{L}(V_{SG} - |V_{th}|)^2, \tag{2}$$

where μ, T_{NOM}, UTE, C_{ox}, W, L, V_{SG}, and V_{th} are the mobility, nominal temperature at which the mobility is extracted, mobility temperature exponent, gate capacitance per unit area, channel width and length of the MOSFET, source-to-gate voltage of the MOSFET, and threshold voltage, respectively. Since UTE has a value between −1 and −1.5 in most CMOS process technologies, the mobility decreases as the temperature increases, and thereby I_D decreases as well [12]–[14]. Since the OLED luminance can be represented as a product of the OLED efficiency in (1) and the pixel driving current in (2) [11], the OLED luminance (L_{OLED}) can be expressed as

$$L_{OLED}(T) = \eta_{ext}(T)I_D(T). \tag{3}$$

Equation (3) should be independent of the temperature to achieve high luminance uniformity of the OLED over a wide operating temperature range. Therefore, the proposed temperature compensation method calculates the pixel current according to the temperature and adjusts the gamma voltages, which drive the pixel circuit, thus eventually making (3) independent of the temperature.

B. FLOWCHART AND ARCHITECTURE FOR THE PROPOSED TEMPERATURE COMPENSATION METHOD

Fig. 2 shows the flowchart of the proposed current calculation algorithm and current adjustment algorithm for the proposed temperature compensation method. The proposed current calculation algorithm performs the following steps (i) to (iii) to calculate the reference currents ($I_{REF}[k]$) according to the temperatures sensed by the four temperature sensors, and the OLED efficiency and driving current ratio for each gamma tap ($A_{IGAM}[k]$) in a look-up-table (LUT), where k is the gray level of 255, 190, 144, 98, 65, 40, 21, 10, 5, and 1.

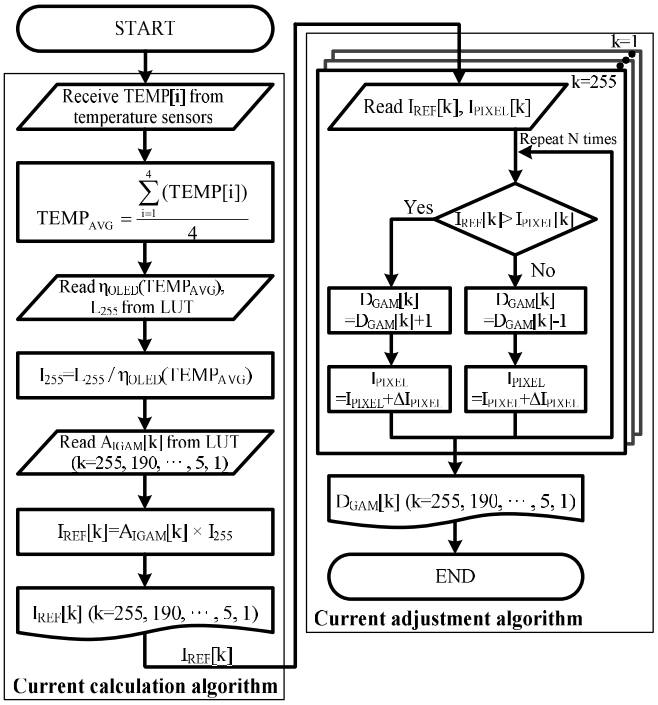

FIGURE 2. Flowchart of the proposed current calculation and current adjustment algorithms.

(i) The proposed current calculation algorithm reads the sensed temperatures (TEMP[i]) and averages them to determine a final temperature value ($TEMP_{AVG}$), where TEMP[i] is the temperature value sensed by the i^{th} temperature sensor. (ii) It reads the OLED efficiency according to $TEMP_{AVG}$ (η_{OLED} ($TEMP_{AVG}$)) and the OLED luminance at the 255 gray level (L_{255}) in the LUT, and it divides L_{255} by η_{OLED} ($TEMP_{AVG}$) to determine the driving current required to drive the OLED to L_{255} (I_{255}). (iii) It reads $A_{IGAM}[k]$ in the LUT and produces $I_{REF}[k]$ by multiplying $A_{IGAM}[k]$ and I_{255}. Through this simple arithmetic calculation, the proposed current calculation algorithm produces the final $I_{REF}[k]$ according to the gray level of the gamma tap.

Next, the proposed current adjustment algorithm performs the following steps (iv) to (vii) to adjust the current of the dummy pixel array ($I_{PIXEL}[k]$) and produces the gamma digital codes ($D_{GAM}[k]$). (iv) It receives $I_{REF}[k]$ and compares it with $I_{PIXEL}[k]$ when k is 255 at the 255 gray gamma tap. (v) It adjusts I_{PIXEL} [255] by increasing I_{PIXEL} [255] with D_{GAM} [255] when I_{REF} [255] is greater than I_{PIXEL} [255], and by decreasing I_{PIXEL} [255] with D_{GAM} [255] when I_{REF} [255] is less than I_{PIXEL} [255]. (vi) After N iterations, where N is the bit number of $D_{GAM}[k]$, it produces D_{GAM} [255] corresponding to the final I_{PIXEL} [255]. (vii) It sequentially repeats steps (iv) to (vi) from 255 to 1 gray gamma tap and then produces the final $D_{GAM}[k]$, which is used to produce gamma voltages.

Fig. 3(a) shows the block diagram of the test chip for organic light-emitting diode-on-silicon (OLEDoS) microdisplays. Fig. 3(b) shows the built-in test circuit implemented in the test chip to verify the proposed temperature compensation method by adjusting the gamma voltages. The built-in test circuit consists of four temperature sensors, a current calculation block, a current adjustment block, a gamma voltage generator, and a LUT containing information on OLED efficiency and driving current ratio for the gamma taps of the display as shown in Fig. 3(b).

The temperature sensors, which are located at the four corners of the pixel array of the test chip, sense the temperatures of the test chip and convert them to TEMP[i] using analog-to-digital converters (ADCs), and then average them as shown in Fig. 3(b). Since the single crystalline silicon substrate used in this work has a good thermal conductivity, which is 1.412 W/(cm·K) at 300K, the difference between the temperatures sensed at four corners was measured to be less than ± 1°C, representing that the sensed temperatures varied little depending on the images and the location of the pixel circuit in a chip. In addition, in order to reduce the temperature error, the temperature sensors perform one-point calibration. The current calculation block, which employs the proposed current calculation algorithm, consists of a current calculator and a current digital-to-analog converter (DAC). The current calculator calculates $D_{IREF}[k]$ based on the sensed temperature and the information in the LUT. The current DAC converts $D_{IREF}[k]$ to $I_{REF}[k]$. The current adjustment block, which employs the proposed current adjustment algorithm to produce $D_{GAM}[k]$, consists of a dummy pixel array, a current comparator (COMP), and a successive approximation register (SAR) logic array. COMP compares $I_{REF}[k]$ with $I_{PIXEL}[k]$ generated by the dummy pixel array and then produces a compared voltage (V_{CMP}). The SAR logic array performs the SAR operation according to V_{CMP} using the binary search algorithm [15] for each gamma tap, and it produces $D_{GAM}[k]$. Next, the gamma voltage generator produces $V_P[k]$ according to $D_{GAM}[k]$, and the dummy pixel array, which is driven by $V_P[k]$, produces $I_{PIXEL}[k]$. In the SAR operation, the SAR logic array initially resets $D_{GAM}[k]$ to 0 for all k and then changes the most significant bit (MSB) of D_{GAM} [255] to 1. COMP then compares I_{PIXEL} [255] corresponding to D_{GAM} [255] with I_{REF} [255] and produces V_{CMP}. When I_{REF} [255] is greater than I_{PIXEL} [255], V_{CMP} becomes high, and the SAR logic array maintains the MSB of $D_{GAM}[k]$ at 1. When I_{REF} [255] is less than I_{PIXEL} [255], V_{CMP} becomes low, and the SAR logic array changes the MSB of $D_{GAM}[k]$ to 0.

These comparison operations are repeated from the MSB to the least significant bit (LSB) of D_{GAM} [255] to produce the final D_{GAM} [255] as shown in Fig. 3(b). The gamma voltage generator then produces the final V_P [255] according to the final D_{GAM} [255], which is in the I-V curve of the driving MOSFETs used in the dummy pixel according to the temperature, when I_{PIXEL} [255] is near I_{REF} [255]. The current adjustment block sequentially repeats the SAR operation from 255 to 1 gray gamma tap and produces $D_{GAM}[k]$. Finally, the gamma voltage generator sends the above final $V_P[k]$ as gamma voltage ($V_{GAM}[k]$),

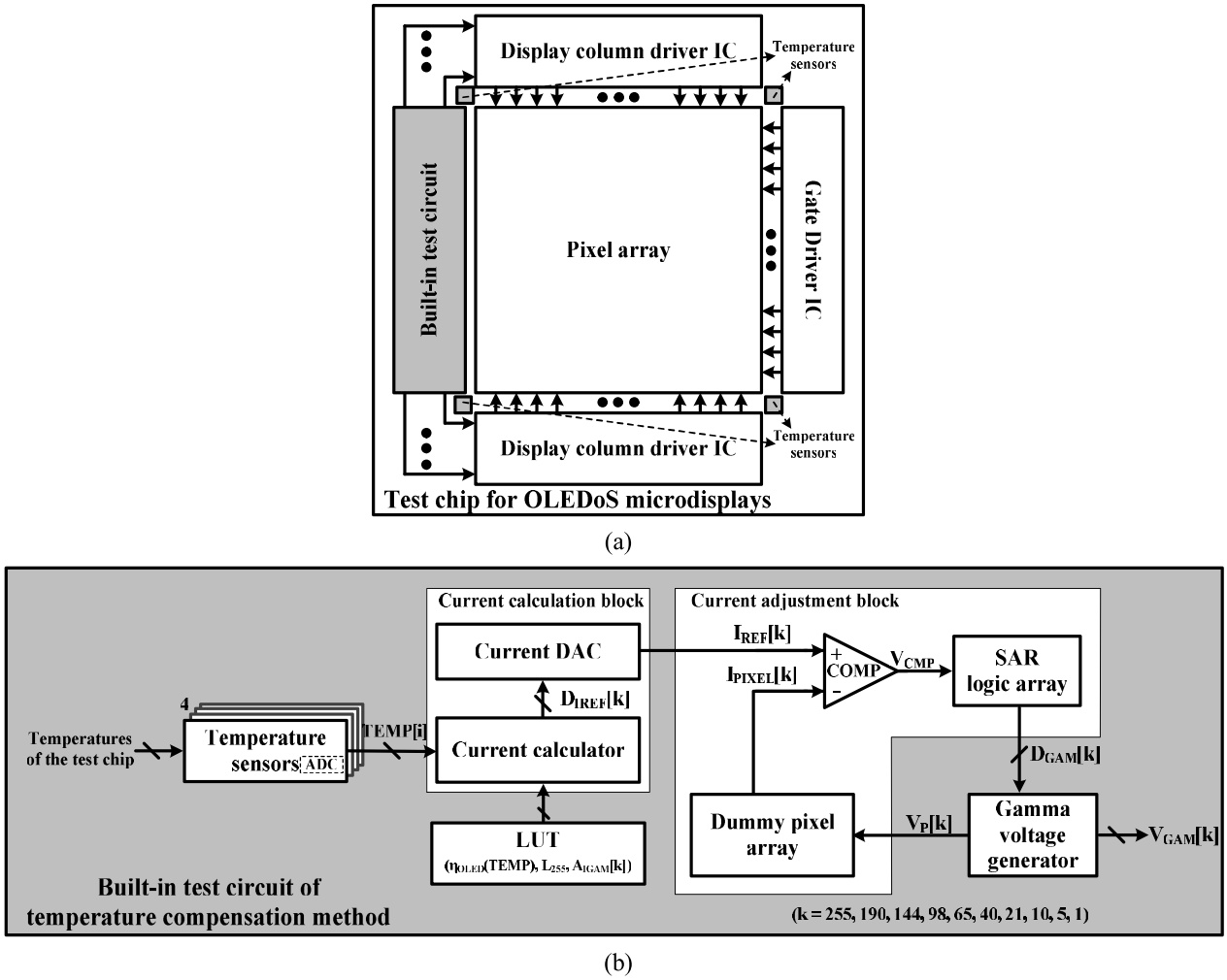

FIGURE 3. Block diagrams of (a) the test chip for OLEDoS microdisplays and (b) the built-in test circuit implemented in the test chip to verify the proposed temperature compensation method by adjusting gamma voltages.

corresponding to $I_{PIXEL}[k]$ in the I-V curve, to the display column driver IC in the test chip. Thus, the proposed temperature compensation method compensates for variations in OLED efficiency and the I-V characteristic of the driving MOSFET according to the temperature.

C. CIRCUIT IMPLEMENTATION

Fig. 4 shows the schematic of the temperature sensor core using bipolar junction transistors (BJTs), which produces a proportional-to-absolute temperature current (I_{PTAT}) and a complementary-to-absolute temperature current (I_{CTAT}). The temperature sensor core senses the temperature using I_{PTAT} and I_{CTAT}, which is obtained by $I_{PTAT}/(I_{PTAT}+I_{CTAT})$ to reduce the error caused by the process variations. Then, the sigma-delta ADC in the temperature sensors converts the sensed temperature to TEMP[i] [16]–[17]. Here, I_{PTAT} and I_{CTAT} are generated as follows. The voltage between the base and emitter of Q2 ($V_{BE,Q2}$) is equal to the sum of the voltage between the base and emitter of Q1 ($V_{BE,Q1}$) and the voltage drop across R1 because the node X is biased by an

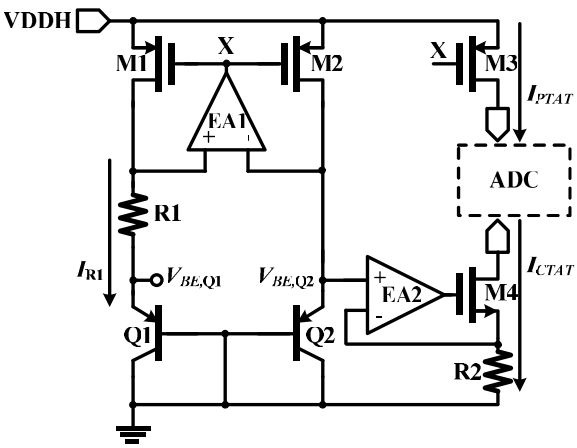

FIGURE 4. Schematic of the temperature sensor core.

error amplifier (EA1). Thus, the drain voltages of M1 and M2 become equal. Therefore, $V_{BE,Q2}$ can be expressed as

$$V_{BE,Q2} = V_{BE,Q1} + I_{R1} \cdot R1, \tag{4}$$

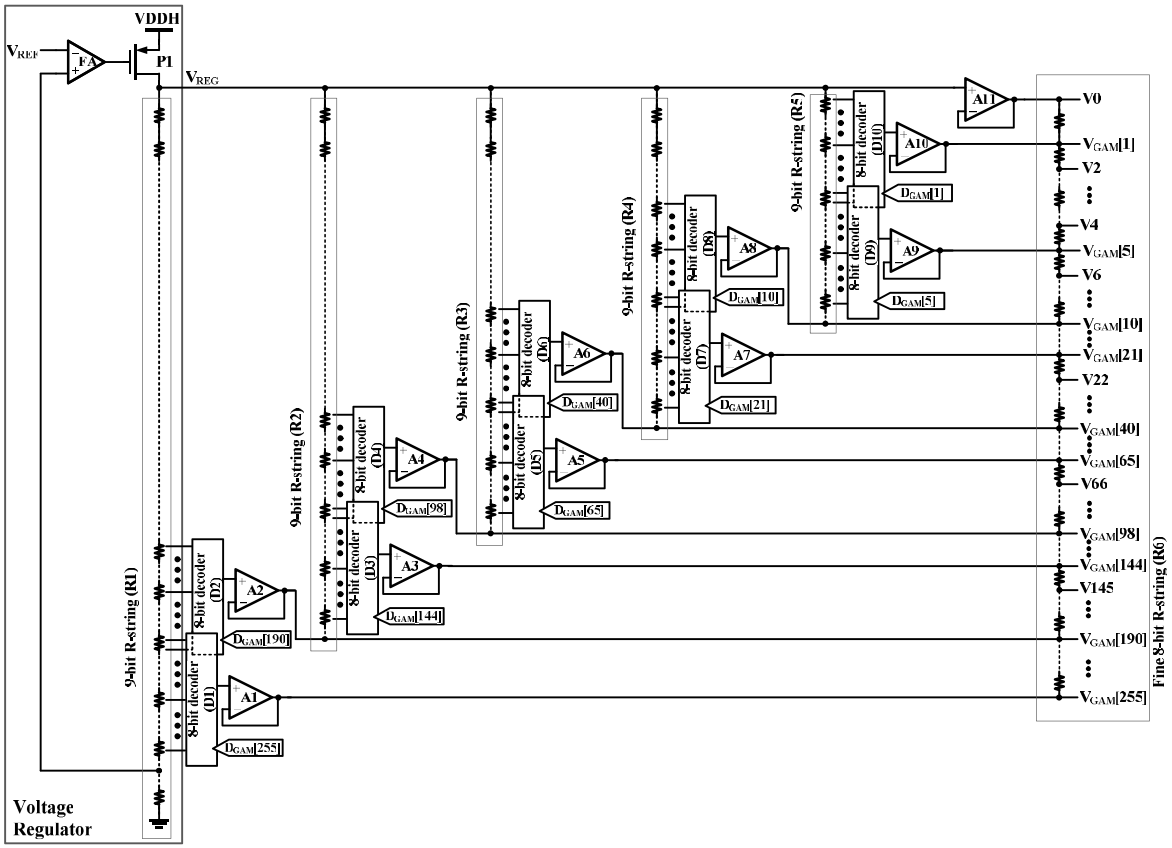

FIGURE 5. Schematic of the gamma voltage generator.

where I_{R1} is the current flowing through R1. The voltage between the base and emitter of BJT (V_{BE}) can be expressed as [16]

$$V_{BE} = \frac{kT}{q} \cdot \ln\left(\frac{I_C}{I_S}\right), \tag{5}$$

where k, T, q, I_C, and I_S are the Boltzmann's constant, temperature, electron charge, collector current, and saturation current, respectively. From (4) and (5), I_{PTAT} of M3 mirrored by M1 and M2 can be expressed as

$$I_{PTAT} = \frac{kT}{q} \cdot \frac{\ln\left(K_{M2}/K_{M1}\right)}{K_{M3}/K_{M1} \cdot R1}, \tag{6}$$

where K is the aspect ratio of the MOSFET. Therefore, I_{PTAT} is linearly proportional to the temperature. Moreover, $V_{BE,Q2}$, which becomes equal to the source voltage of M4 using the error amplifier (EA2), generates a current flowing through R2 (I_{CTAT}) that can be expressed as

$$I_{CTAT} = \frac{V_{BE,Q2}}{R2}. \tag{7}$$

From [16]–[17], I_{CTAT} is inversely proportional to the temperature because $V_{BE,Q2}$ decreases as the temperature increases.

Fig. 5 shows the schematic of the gamma voltage generator, which consists of a p-channel MOSFET (P1), a feedback amplifier (FA), five 9-bit R-strings (R1-R5), ten 8-bit decoders (D1-D10), eleven gamma buffer amplifiers (A1-A11), and a fine 8-bit R-string (R6). The five 9-bit R-strings produce fine voltages as the gray level lowers, while reducing the number of resistors by dividing the stage of the R-strings [18]. Each pair of 8-bit decoders (D1 and D2, D3 and D4, D5 and D6, D7 and D8, and

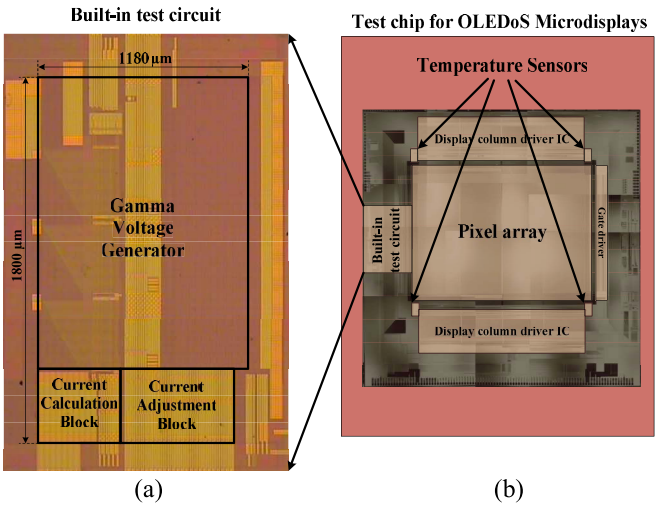

FIGURE 6. Photomicrographs of the (a) built-in test circuit for the proposed temperature compensation method and (b) test chip for OLEDoS microdisplays.

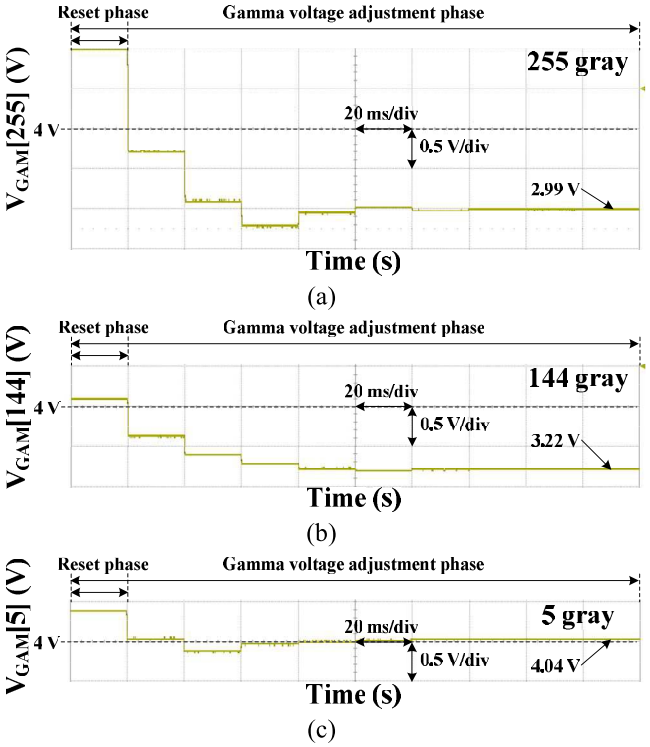

FIGURE 7. **Measured voltage waveforms of (a) 255, (b) 144, and (c) 5 gray gamma taps at room temperature.**

D9 and D10) shares the voltages produced by the 9-bit R-string depending on the gamma voltage of the corresponding 8-bit decoder. The voltage regulator, including P1, FA, and R1, receives a bandgap reference voltage (V_{REF}) as an input and generates a regulated voltage (V_{REG}), which is buffered through A11. Then, a 0 gray voltage (V0) is produced. D1 selects a voltage among the 9-bit voltages between V_{REG} and ground, which are divided by R1, according to D_{GAM} [255]. The selected voltage is then buffered through A1, and a gamma voltage of 255 gray gamma tap (V_{GAM} [255]) is produced. In the same manner as V_{GAM} [255], D2 selects a voltage among the 9-bit voltages between V_{REG} and ground, which are divided by R1, according to D_{GAM} [190]. The selected voltage is then buffered through A2, and a gamma voltage of 190 gray gamma tap (V_{GAM} [190]) is produced. Next, D3 selects a voltage among the 9-bit voltages between V_{REG} and V_{GAM} [190], which are divided by R2, according to D_{GAM} [140]. The selected voltage is then buffered through A3, and a gamma voltage of 140 gray gamma tap (V_{GAM} [140]) is produced. D4 selects a voltage among the 9-bit voltages between V_{REG} and V_{GAM} [190], which are divided by R2, according to D_{GAM} [98]. The selected voltage is then buffered through A4, and a gamma voltage of 98 gray gamma tap (V_{GAM} [98]) is produced. In this way, each gamma voltage is sequentially produced from a gray level of 255 to 1. The voltage interval of the 9-bit voltages for the gamma voltages selection decreases as the gray level lowers, thus increasing the sensitivity in the lower gray levels.

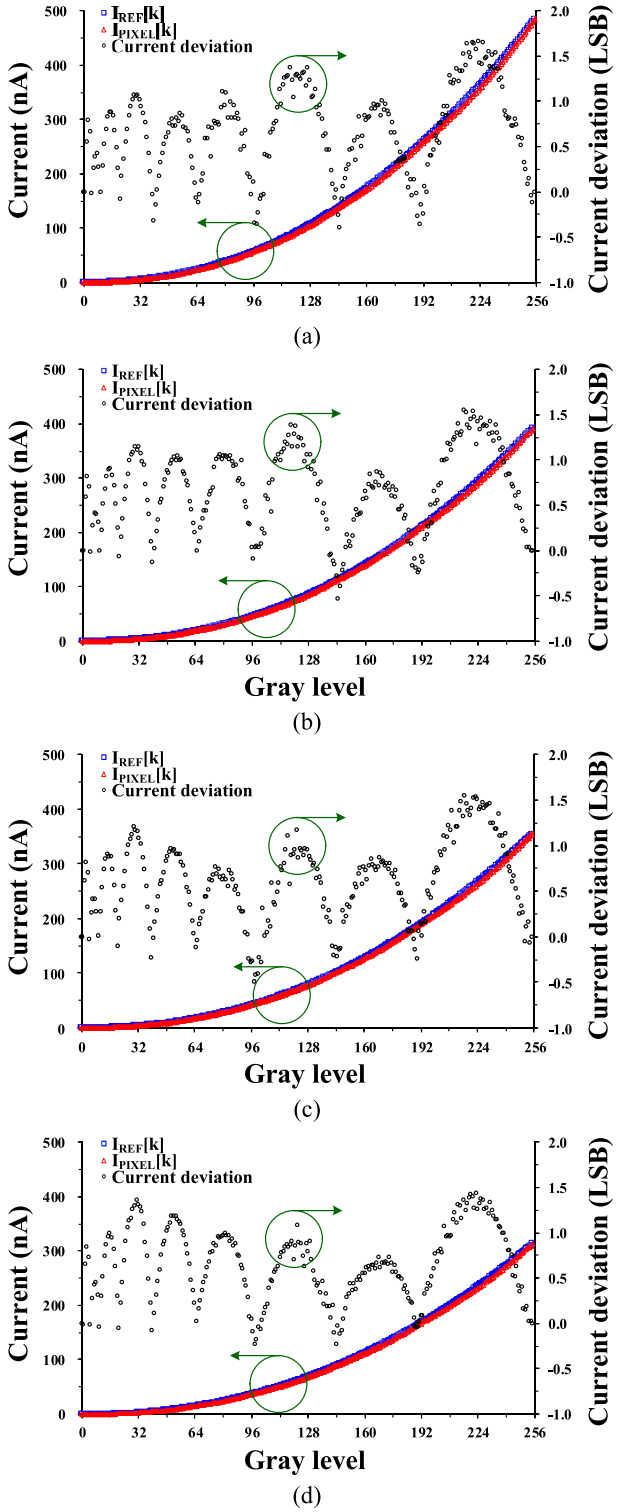

FIGURE 8. **Measurement results of I_{PIXEL}[k] and calculated I_{REF}[k] (on the left y-axis) and the current deviation (on the right y-axis) with respect to gray level when the temperatures is (a) −40°C, (b) 0°C, (c) 25°C, and (d) 60°C.**

III. MEASUREMENT RESULTS

To verify the proposed temperature compensation method, a built-in test circuit implemented in a test chip for OLEDoS

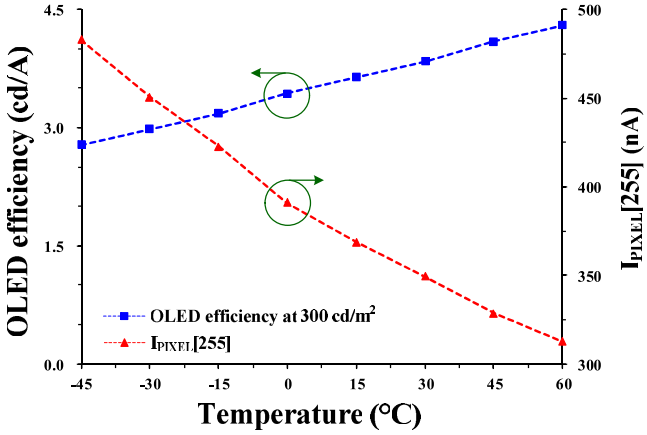

FIGURE 9. Measurement results of OLED efficiency at 300 cd/m^2 and I_{PIXEL} [255] in the temperature range from −45°C to 60°C.

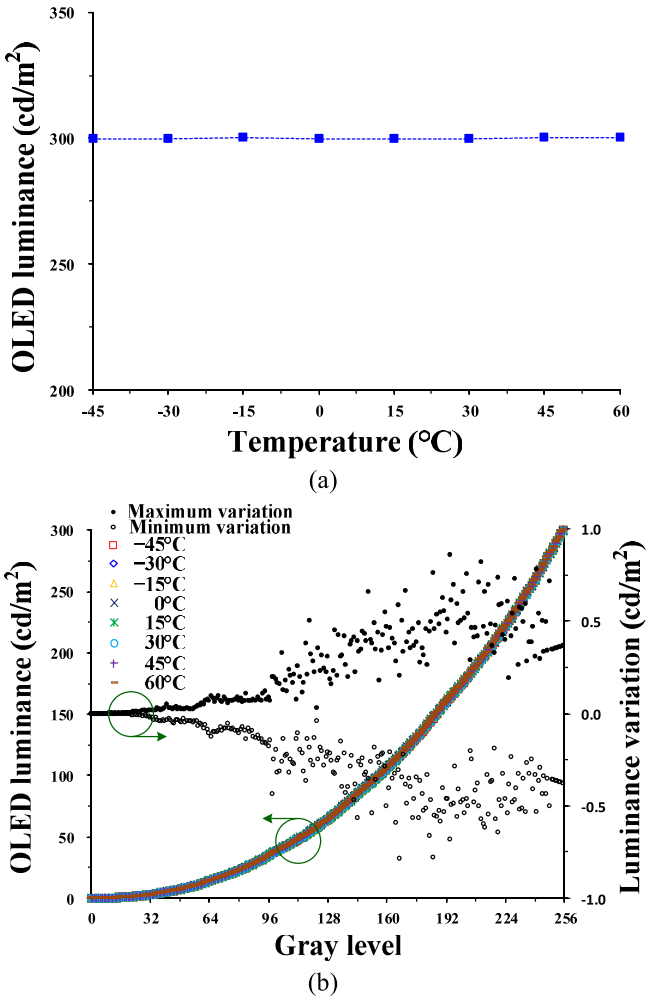

FIGURE 10. (a) Calculated OLED luminance according to temperature at the 255 gray level and (b) calculated OLED luminance (on the left y-axis) and its variation (on the right y-axis) according to the gray level in the temperature range from −45°C to 60°C.

microdisplays was fabricated using 90 nm standard CMOS process technology with 6 V high-voltage devices. Figs. 6(a) and (b) show the photomicrographs of the built-in test circuit and the test chip for OLEDoS microdisplays, respectively. The built-in test circuit includes the current calculation block, current adjustment block, and gamma voltage generator, and the test chip for OLEDoS microdisplays includes the built-in test circuit, temperature sensors, display column driver ICs, a gate driver, and a pixel array. The built-in test circuit occupies an area of 1180×1800 μm^2, excluding the temperature sensors, which are located at the four corners of the pixel array in the test chip.

TABLE 1. Performance summary.

Index	[9]	[10]	[11]	This work
Process with device	Low-temperature poly-Si TFT	Low-temperature poly-Si TFT	90 nm CMOS process with 6 V device	90 nm CMOS process with 6 V device
Area (μm × μm)	-	-	-	1180 × 1800
Temperature error of temperature sensor (°C)	-	-	-	−0.84 to 0.79
Current deviation (LSB)	-	-	-	−0.53 to 1.65
Temperature range (°C)	−20 to 60	−20 to 80	−45 to 60	−45 to 60
Luminance variation (cd/m^2)	28.00	2.76	11.30	1.54

Figs. 7(a), (b), and (c) show the measured voltage waveforms of the 255, 144, and 5 gray gamma taps at room temperature, respectively. In the reset phase, the gamma digital codes are 0 to reset the gamma voltages. In the gamma voltage adjustment phase, the gamma voltages are adjusted until $I_{PIXEL}[k]$ is near to $I_{REF}[k]$.

Figs. 8(a), (b), (c), and (d) show the measurement results of $I_{PIXEL}[k]$ and the calculated $I_{REF}[k]$ (on the left y-axis) and the current deviation (on the right y-axis) with respect to the gray level when the temperatures are −45, 0, 25, and 60°C, respectively. The current deviation between $I_{PIXEL}[k]$ and $I_{REF}[k]$ ranges from −0.53 LSB to +1.65 LSB over the entire gray level, demonstrating that the proposed compensation method effectively works.

Fig. 9 shows the measurement results of the OLED efficiency at 300 cd/m^2 and I_{PIXEL} [255] in the temperature range from −45°C to 60°C. The measured OLED efficiency, which is modeled as a linear equation, varies from 2.78 cd/A to 4.30 cd/A and the measured I_{PIXEL} [255] varies from 483 nA to 312 nA according to the temperature. The OLED luminance can be calculated as the product of the OLED efficiency and I_{PIXEL} [255]. Fig. 10(a) shows the calculated OLED luminance according to the temperature at the 255 gray level, which varies from 299.60 cd/m^2 to 300.34 cd/m^2 over the temperature range of −45°C to 60°C. Fig. 10(b) shows the calculated OLED luminance

(on the left y-axis) and its variation (on the right y-axis) according to the entire gray level in the temperature range from −45°C to 60°C, indicating that the proposed temperature compensation method achieves high luminance uniformity, which has an OLED luminance variation of less than 1.54 cd/m^2.

The performances of the proposed temperature compensation method are summarized and compared with those of previous works in Table 1. The proposed temperature compensation method achieves the least luminance variation, representing the best luminance uniformity compared to previous works.

IV. CONCLUSION

In this paper, a temperature compensation method is proposed and verified using a built-in-test circuit on a single-crystalline silicon wafer for high luminance uniformity AMOLED displays. The proposed temperature compensation method employs a simple algorithm to calculate the reference current. In addition, it employs a current adjustment algorithm, which compares the reference current with the current of the dummy pixel array to compensate for OLED luminance variation according to the temperature by adjusting the gamma voltages. To verify the proposed temperature compensation method, a built-in-test circuit was fabricated using 90-nm CMOS process technology with 6-V high-voltage devices. The measurement results show that the current deviation ranges from −0.53 LSB to +1.65 LSB over the temperature range of −45°C to 60°C. Moreover, the proposed temperature compensation method has an almost constant value of OLED luminance ranging between 299.60 cd/m^2 and 300.34 cd/m^2 over the temperature range of −45°C to 60°C, resulting in OLED luminance variation less than 1.54 cd/m^2. Therefore, the proposed temperature compensation method is suitable for AMOLED displays requiring high luminance uniformity.

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