Received 9 September 2019; revised 5 November 2019; accepted 5 November 2019. Date of publication 8 November 2019;
date of current version 27 April 2020. The review of this article was arranged by Editor L. F. Marsal.

Digital Object Identifier 10.1109/JEDS.2019.2952449

DC and 28 GHz Reliability of a SOI FET Technology

EDMUNDO A. GUTIÉRREZ-D.[1] (Senior Member, IEEE), JAIRO MÉNDEZ-V.[1], JULIO C. TINOCO[3], EMMANUEL TORRES RIOS[4], AND OSCAR V. HUERTA-G.[1,2]

1 Department of Electronics, National Institute for Astrophysics, Optics and Electronics, Puebla 72000, Mexico
2 Reliability Group, GlobalFoundries, Malta, NY 12020, USA
3 Centro Microna, Universidad Veracruzana, Veracruz 94294, Mexico
4 Department of Computers Science, ITESM, Puebla 72453, Mexico

CORRESPONDING AUTHOR: E. A. GUTIÉRREZ-D.(e-mail: edmundo@inaoep.mx)

This work was supported in part by the Mexico National Council for Science and Technology.

ABSTRACT We introduce experimental results of the I-V degradation characteristics of a Silicon SOI technology for RF applications when stressed under both; a 28 GHz and a DC stress input signals. Then we compare the effect of DC and RF stress on threshold voltage, transconductance, and drain current capability. We observe that reliability under RF stress is gate voltage dependent, and in some cases an improvement ("healing") of the I-V characteristics is observed. A hypothetical explanation for the degradation/enhancement under RF stress is attributed to a self-heating and self-healing (SH^2) mechanism. The degradation mechanism is also simulated, and the reliability model tested, with Cadence.

INDEX TERMS SOI, FET, 28 GHz, degradation, reliability.

I. INTRODUCTION

The SOI RF technology is considered as a candidate for the integration of 5G communication functions, such as RF power amplification [1], [2], where the circuits and transistors are operated under high-electric field stress and heat generation. Under such an operation condition, the threshold voltage, the transconductance, and the output conductance, degrade, which negatively impacts on the RF performance of amplifiers. Therefore, a reliability study under RF and DC conditions is a must. Thus, in this paper we introduce experimental work at both DC and 28 GHz stressing conditions, and run reliability simulations with the Cadence RelXpert model [3], where the model is compared to experimental results. The simulations are compared to experimental data with and without selfheating (SH), where we found that SH is less relevant in the subthreshold regime than in strong inversion when predicting device ageing.

II. EXPERIMENTAL PROCEDURE AND DEVICE TECHNOLOGY

Partially depleted SOI FET devices from a commercial 45nm node technology where measured under DC and 28 GHz stress conditions. The device is a Ground-Signal-Ground (GSG) RF transistor with a (W/L) geometry ratio of (40 μm/40 nm), and a nominal operation voltage of 0.8 V.

The FET ageing process is accelerated by applying an overvoltage of Vd = 1.6 V and a Vg = 0.8 V at stress time periods of 100, 300, 1000, 2000, and 3000, seconds, at room temperature. In some cases we extend the stress time up to 8000 seconds. The 28 GHz RF signal of an input power of −20 dBm is superimposed on the DC input Vg = 0.8 V, while the Vd is set at 1.6 V. The B1500A Keysight Semiconductor Device Analyzer (SDA), for DC biasing and I-V recording, is configured with an E8361A Keysight Vector Network Analyzer (VNA), which is used for RF stress and S-parameters recording as well. The data was taken from 5 different samples, and we only show the most representative data. Overall, the performance variation between different samples is not larger than 10 %.

Figures 1, 2, 3 and 4 show the measured degraded electrical characteristics, where a bias dependence of the degradation is evident. For instance, as shown in Figure 1, the degradation of the Id current ΔId is more pronounced at low Vg bias condition. In the subthreshold regime (Vg<0.3 V) the degradation is in the order of 65 a.u., while in the strong

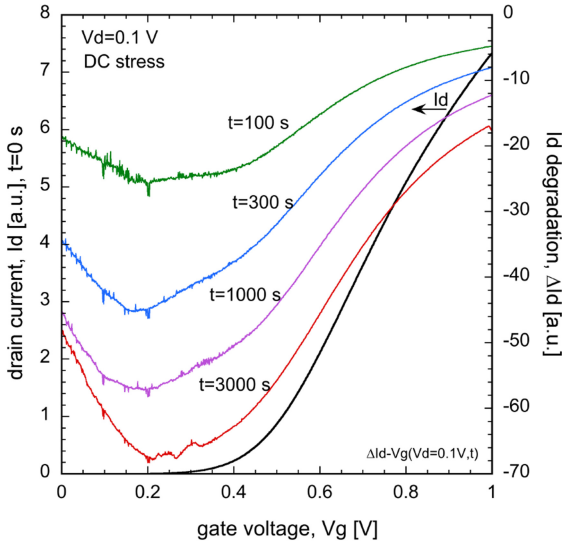

FIGURE 1. Measured Id and degradation ΔId versus Vg at Vd = 0.1 V for DC stress times of 100, 300, 1000, and 3000 s.

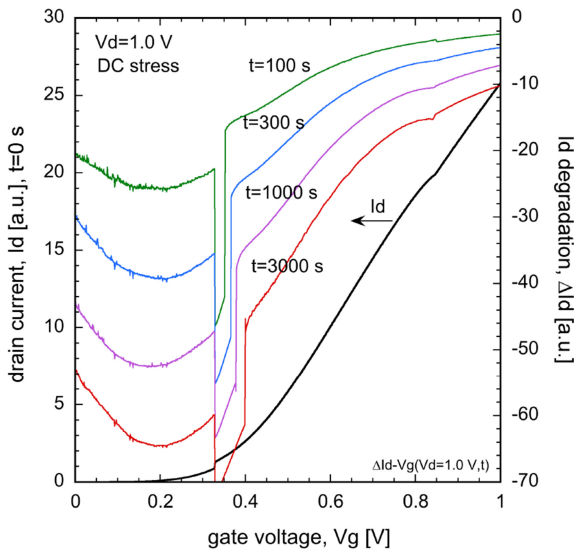

FIGURE 2. Measured Id and degradation ΔId versus Vg at Vd = 1.0 V for stress times of 100, 300, 1000, and 3000 s.

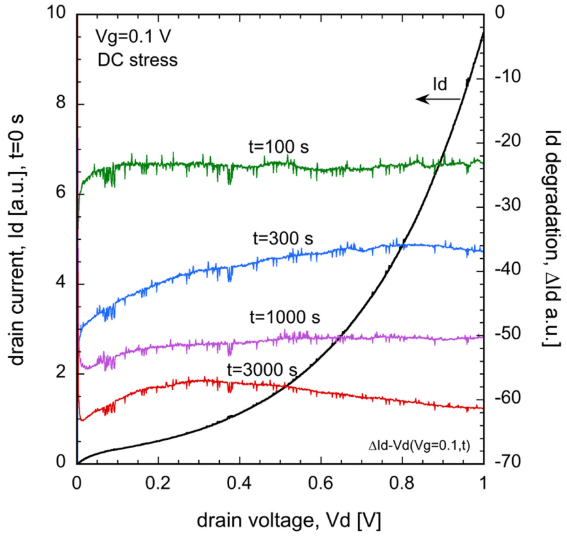

FIGURE 3. Measured Id and degradation ΔId versus Vd at Vg = 0.1 V for DC stress times of 100, 300, 1000, and 3000 s.

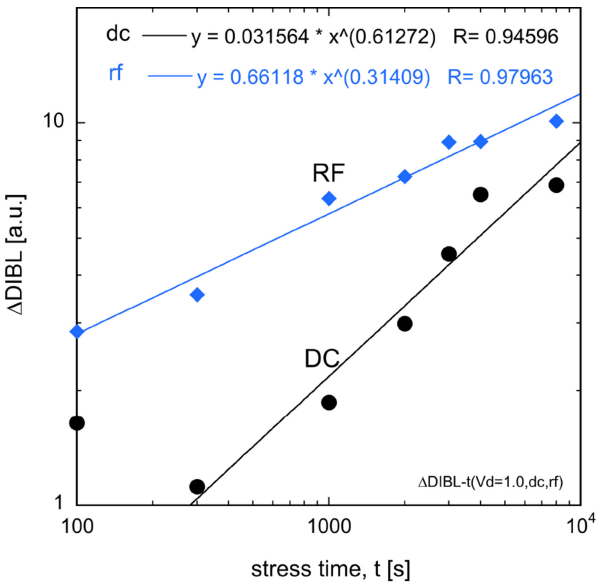

FIGURE 4. Measured ΔDIBL as a function of stress time under DC and RF stress condition.

inversion (Vg>0.6 V), the ΔId degradation is in the order of 20 a.u.. The experimental data of Figure 1 is for the FET device biased at Vd = 0.1 V, where hot carriers are not expected to show up.

When Vd is set to 1.0 V (see Figure 2), the kink effect shows up for 0.35 V <Vg< 0.85 V intervals, which is the fingerprint of hot-carriers. Again, in this case the degradation is larger at low Vg values (65 a.u.), but lower in the hot-carrier regime (0.35 V <Vg<0.85 V) (20 a.u.). The step in ΔId shown in Vg = 0.35 V and Vg = 0.85 V, correspond to the onset and offset of the hot-carrier regime. The discontinuity of ΔId at about Vg = 0.35 is caused by the shift of the hot carrier regime toward large Vg values at different stress times.

The drain-induce-barrier-lowering (DIBL) [4] effect is evident from Figure 3, where a large exponential injection of electrons from the source over the lowered channel barrier is shown as Id. The DIBL increases with the stress time as shown in Figure 4. When stressed under RF condition, the ΔDIBL increase is larger than when stressed under DC conditions. An immediate conclusion is that the RF stress increases the source-drain potential barrier.

The ΔId drain current degradation, in the subthreshold regime, is almost independent of Vd. However, in strong inversion at Vg = 1.0 V, the drain bias dependence is evident (see Figure 5). The sharp transition shown by ΔId at Vd below 0.2 V is correlated with the output conductance modulated by the degradation as shown in Figure 6. The output conductance

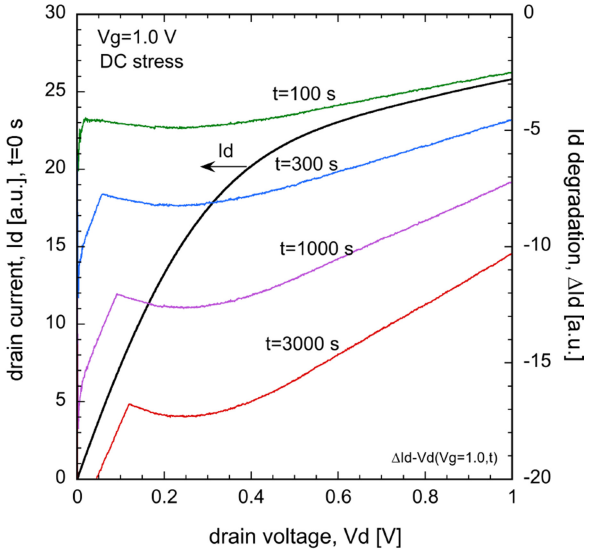

FIGURE 5. Measured Id and degradation ΔId versus Vd at Vg = 1.0 V for stress times of 100, 300, 1000, and 3000 s.

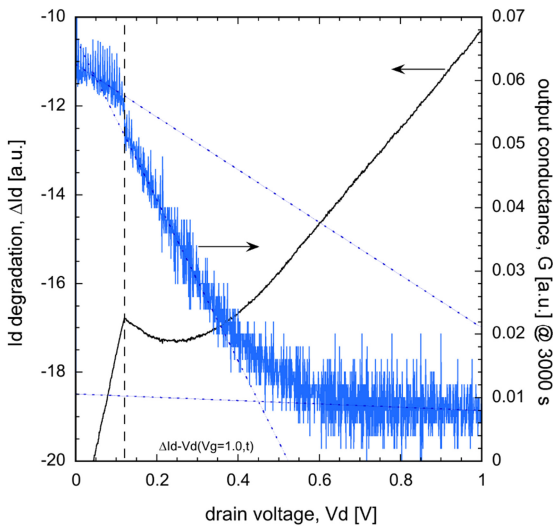

FIGURE 6. Measured output conductance G and ΔId for Vg = 1.0 V, stress time t = 3000 s, under DC stress.

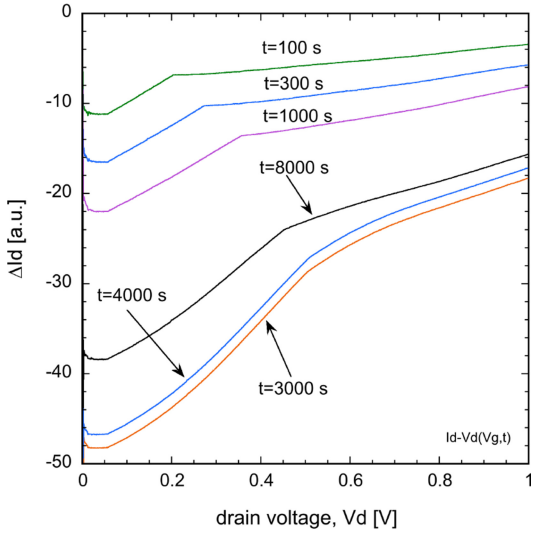

FIGURE 7. Measured ΔId as a function of Vd for Vg = 1.0 V, under RF stress condition.

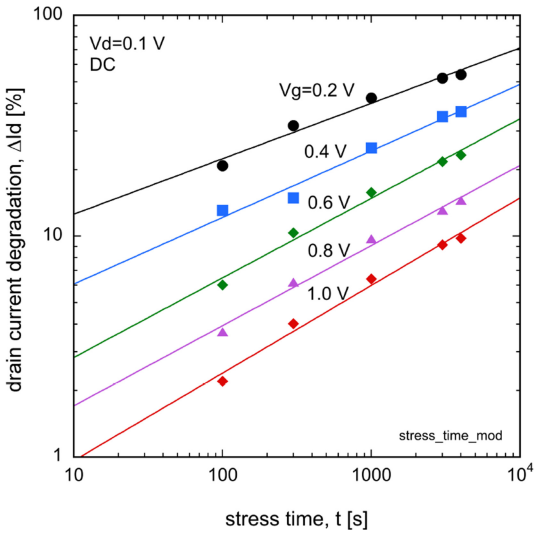

FIGURE 8. Drain current degradation ΔId versus stress time for Vd = 0.1 V for different Vg voltages under DC stress.

G shows a slope change just at the sharp transition of ΔId as indicated by the extrapolated straight lines.

Below that sharp transition, at Vd<0.12 V, the degradation ΔId increases linearly. A shown in Figure 5, the sharp transition shifts to larger Vd values as the stress time increases.

This is attributed to the threshold voltage V_T shift. When the device is stressed with a RF signal, the degradation ΔId is larger than under DC stress, and even shows a recovery for stress times larger than 3000 s as depicted in Figure 7. The degradation ΔId shows a saturation trend between 3000 and 4000 seconds, and then rolls down at t = 8000 s. The roll down of ΔId for t>3000 s is interpreted as a healing effect, i.e., a reduction of interface traps by annealing. The ΔId degradation under DC conditions is shown in Figure 8. This is for Vd = 0.1 V, and Vg = 0.2, 0.4, 0.6. 0.8, and 1.0 V. The degradation follows the power law

$$\Delta Id[a.u.] = at^b \tag{1}$$

as expected. When the device is stressed under RF conditions, the degradation ΔId deviates from the power law as shown in Figure 9.

The power law is fulfilled for Vg<0.6 V. For Vg=>0.6 V, ΔId deviates from the power law and rolls down for t >3000 s. The stress time of 3000 seconds signals the time where the degradation reduces.

III. ANALYSIS AND MODELLING

Because of the long time required for the DC/RF reliability experiments, a statistical analysis was conducted in only 3 different samples from the same process run. The threshold

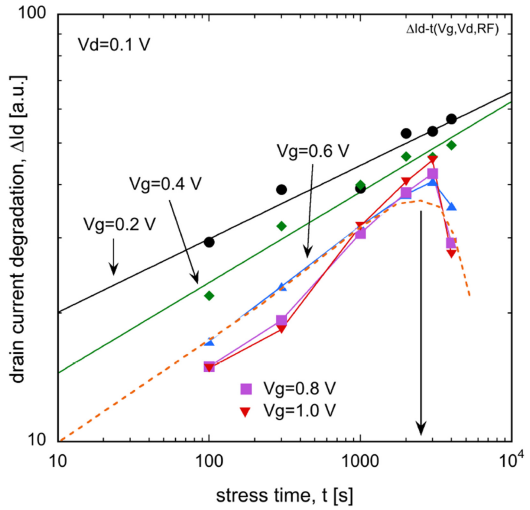

FIGURE 9. Measured ΔId degradation versus stress time under RF stress condition.

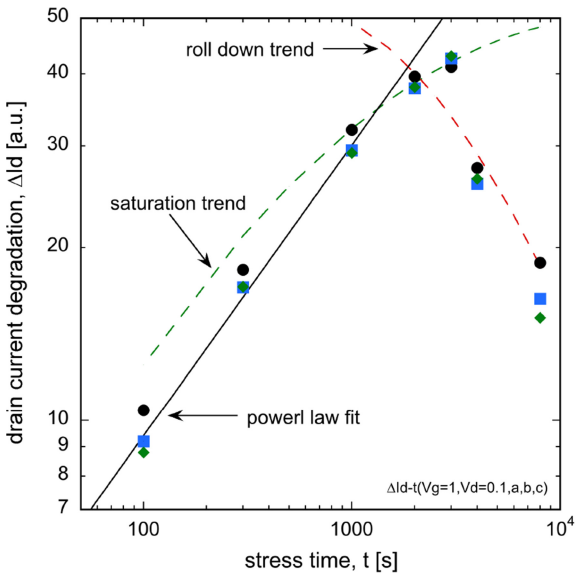

FIGURE 10. Measured ΔId versus stress time under RF stress for three different samples (symbols). Vg = 1.0 V, Vd = 0.1 V. Samples a, b, and c, stressed under RF condition are shown in symbols.

voltage V_T, the transconductance gm, the drain on-current I_{on}, and the drain off-current I_{off}, showed a variability of 10 a.u., 15 a.u., 12 a.u., and 28 a.u., respectively. The V_T was extracted using the Id constant value of 1 μA at Vd = 0.1 V, while the transconductance was extracted at the point of the maximum value of the dId/dVg derivative.

For the specific case of RF stress, three samples named *a*, *b*, and *c*, were stressed for up to 8000 seconds, with an RF input signal of −20 dBm superimposed on a Vg = 0.8 V and a Vd = 1.6 V. The drain current Id was monitored at the bias condition of Vg = 1.0 V and Vd = 0.1 V. The measured ΔId degradation versus stress time is shown in Figure 10. The roll down of ΔId after 3000 s is verified in at least three different samples. In average, Id at t = 8000 s recovers back to the same value at about t = 300 s.

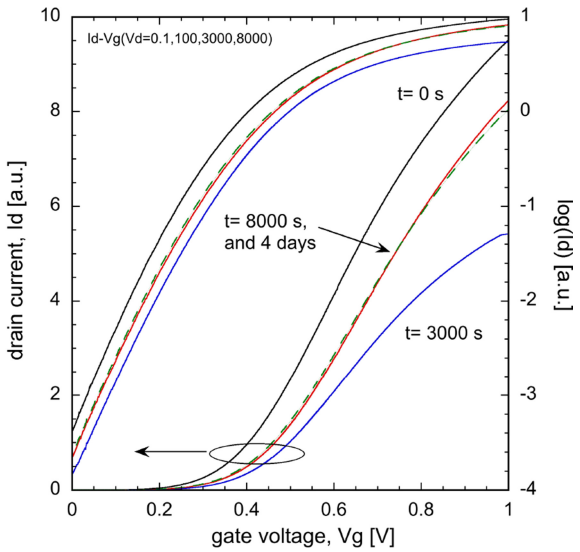

FIGURE 11. Measured Id-Vg curve for Vd = 0.1 V, for stress times t = 0, 3000, and 8000 s. The dashed line corresponds to the device stressed for 8000 s and measured 4 days after being saved in a box.

In the 100-1000 s period of time ΔId follows a power law. However, for t >1000 s a moderate deviation from the power law is shown, which is indicated by the dashed line "saturation trend".

From 3000 s onward ΔId rolls down, which is marked with the "roll down trend" dashed line.

In summary, we can say that two mechanisms working against the other are shown; one mechanism that tends to degrade the device, and another one that competes to heal the device. We interpret the ΔId roll down as regeneration or healing of the device. Indeed, the devices that were stressed for 8000 s, were unplugged from the test equipment, and saved in a box for four days. After 4 days the device was measured again. The I-V characteristics were measured again and compared to those at t = 0, 3000, and 8000 s, as shown in Figure 11. The dashed line corresponds to the device that was saved in a box, after being stressed for 8000 s. The difference between these two measurements is negligible. This minimum difference reinforces the fact that the 8000 s stressed device suffered a stable reversible regeneration, or in other words, a device healing. The saturation of current degradation versus stress time ΔId-t, shown in figures 9 and 10, as been explained in [5] as the contribution of two components: one called permanent degradation given by the interface trap generation with electron trapping, and a second one called recoverable attributed to hole trapping/detrapping. And as mentioned in the same reference, the permanent degradation is a dominant characteristic of digital circuits, but not the only one in other applications such as in power amplifiers. Thus the degradation model shown in equation (1) should be modified to account for the recoverable component.

$$\Delta Id[a.u.] = at^{(b-b't)} \quad (2)$$

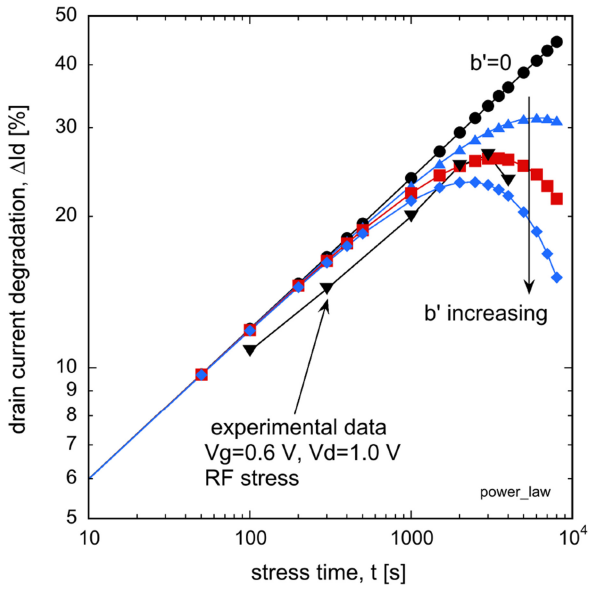

FIGURE 12. Calculated ΔId-t curve as per the model of equation (2).

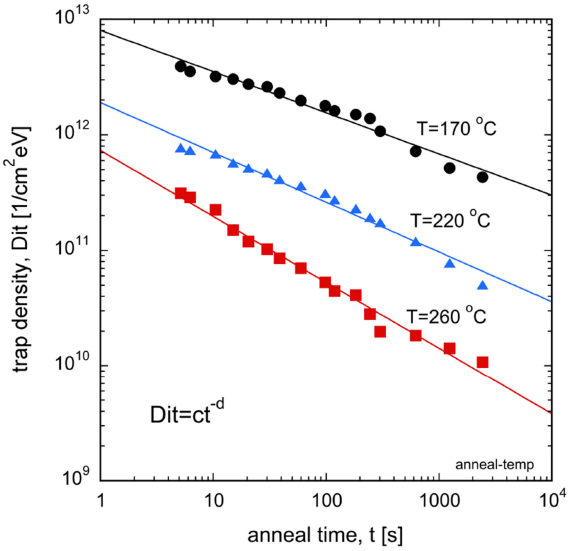

FIGURE 13. Trap density versus anneal time replotted from [7].

where b′ is the recoverable factor that models the saturation and roll down effect as shown in Figure 12.

The model of equation (2) is a first simple approach that yet requires accounting for temperature dependence as pointed out in [5]; the recoverable component has lower temperature activation energy than that of the permanent mechanism. Therefore, if the device temperature is raised because of selfheating effect [6], the recoverable mechanism could be activated earlier than that of the permanent one, and might enter into competition with trap annealing [7]. In [7] trap annealing has been observed to occur at 170 °C for annealing times as short as 1000 s (see Figure 13). However, the anneal kinetics is also a function of the crystal orientation, where <100> interface anneals faster than <111>. On top of the crystal orientation, the geometry of the transistor needs to be accounted for the reliability model [8]. In [8] the magnitude of the degradation as well as the saturation of the drain current degradation is a function of the FinFet width.

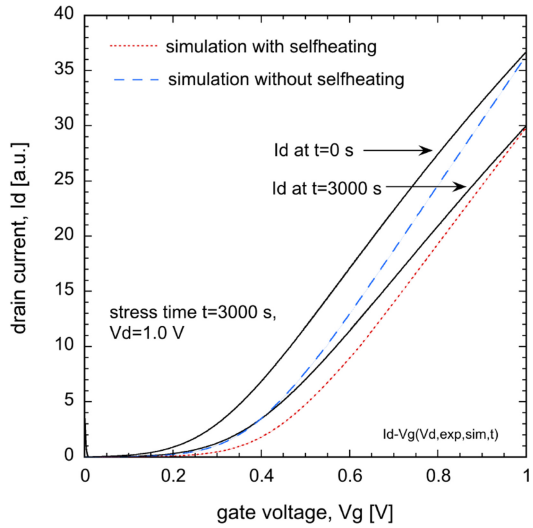

FIGURE 14. Experimental (continuous line) and Cadence simulation results (dotted and dashed lines) at t = 3000 s.

A Cadence simulation with the RelXpert module was conducted. The simulations were run with and without self-heating effects. The results are shown in Figure 14. A ΔId-t simulation predicts a power law relationship as that of Figure 8. However, as shown in Figure 14, a simulation including selfheating underestimates the degradation, while overestimates it when selfheating is accounted for.

IV. CONCLUSION

In general, the magnitude of the drain current degradation ΔId for both, DC and RF stress is similar. However, under RF stress the degradation deviates from the power law relationship. As seen from experimental data, the ΔId-t relationship tends to saturate at stress times longer than 2000 s, and rolls down for t > 3000 s. The saturation of ΔId is attributed to a recovery mechanism competing with a permanent degradation mechanism. The permanent degradation is associated to trap generation with electron trapping, while the recovery mechanism is associated to hole trapping/detrapping. However, the roll down of ΔId cannot be explained by the sole hole presence of trapping/detrapping mechanism. The selfheating mechanism might be also playing a role by raising the device local temperature, prompting to a local trap annealing effect in addition of an early triggering of hole trapping/detrapping. However, in this experimental work we were not able to measure the local temperature because of a lack of an on-wafer temperature sensor. However, the Cadence simulation points out to a recalibration of the selfheating model within the Cadence/SPICE model. Making the *b* slope a time-dependent function that can predict the deviation of the ΔId-t from the

power law relationship. From the circuit simulation point of view, this can be a simple straightforward solution for fast reliability simulations.

ACKNOWLEDGMENT

The first author acknowledges CONACyT-Mexico for the support given through the Ph.D. scholarships of two Ph.D. students, and also to INAOE for providing all the measurement facilities.

REFERENCES

[1] O. T. Ogunnika and A. Valdes-Garcia, "A 60GHz class-E tuned power amplifier with PAE>25% in 32 nm SOI CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Montreal, QC, Canada, 2012, pp. 65–68, doi: 10.1109/RFIC.2012.6242233.

[2] K. Ning and F. Buckwalter, "A 28-GHz, 18-dBm, 48% PAE stacked-FET power amplifier with coupled-inductor neutralization in 45-nm SOI CMOS," in *Proc. IEEE BiCMOS Compd. Semicond. Integr. Circuits Technol. Symp. (BCICTS)*, San Diego, CA, USA, 2018, pp. 85–88, doi: 10.1109/BCICTS.2018.8550832.

[3] D. Mahajan and V. Ruparelia, "Reliability simulation and analysis of important RF circuits using cadence Relxpert," in *Proc. IEEE Int. Conf. Electron. Comput. Commun. Technol. (CONECCT)*, Bengaluru, India, 2018, pp. 1–6, doi: 10.1109/CONECCT.2018.8482396.

[4] R. R. Troutman, "VLSI limitations from drain-induced barrier lowering," *IEEE Trans. Electron Devices*, vol. ED-14, no. 2, pp. 383–391, Apr. 1979, doi: 10.1109/JSSC.1979.1051189.

[5] V. Huard *et al.*, "New characterization and modeling approach for NBTI degradation from transistor to product level," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, USA, 2007, pp. 797–800, doi: 10.1109/IEDM.2007.4419068.

[6] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, J. T. Bunyan, and M. J. Uren, "Self-heating effects in SOI MOSFETs and their measurement by small signal conductance techniques," *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 2240–2248, Dec. 1996, doi: 10.1109/16.544417.

[7] M. L. Reed and J. D. Plummer, "Chemistry of Si-SiO_2 interface trap annealing," *J. Appl. Phys.*, vol. 63, no. 12, pp. 5776–5793, 1988, doi: 10.1063/1.340317.

[8] C.-L. Lin *et al.*, "Effects of fin width on device performance and reliability of double-gate n-type FinFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3639–3644, Nov. 2013, doi: 10.1109/TED.2013.2281296.

EDMUNDO A. GUTIÉRREZ-D. (M'95–SM'06) was born in Mexicali, Mexico, in December 1960. He received the Ph.D. degree from Katholieke Universiteit Leuven, Belgium, in 1993. He is a specialist in semiconductor device physics, particularly on cryogenic and magnetic behavior of advanced FET technologies, as well as dc, and RF reliability.

He was a Guest Professor with Simon Fraser University, Vancouver, Canada, in 1993, and lectured a Summer Ph.D. course with the Polytechnic University of Sao Paulo, Brazil, in 1993. From 2000 to 2002, he was a Design Manager with the Motorola Mexico Center for Semiconductor Technology, Puebla, Mexico. In 2002, he was a Guest Professor with the Technical University of Vienna, Austria. From 2005 to 2006, he was the Technical Director of the Intel Systems Research Center, Guadalajara, Mexico. He is currently a Professor with the Department of Electronics, National Institute for Astrophysics, Optics, and Electronics, Puebla. He has authored more than 145 refereed articles in journals and conference proceedings. He has authored the books entitled *Low Temperature Electronics, Physics, Devices, Circuits, and Applications* (Academic Press, 2001) and *Nano-Scaled Semiconductor Devices, Physics, Modelling, Characterisation, and Societal Impact* (IET Press, 2016). He has graduated 7 M.Sc. and 15 Ph.D. students.

Prof. Gutiérrez-D. is an Editor of IEEE ELECTRON DEVICE LETTERS and the IEEE TRANSACTIONS ON ELECTRON DEVICES, as well as a member of the Board of Governors of the IEEE Electron Devices Society.

JAIRO MÉNDEZ-V. is currently pursuing the Ph.D. degree with the Department of Electronics, National Institute for Astrophysics, Optics, and Electronics.

JULIO C. TINOCO received the Ph.D. degree in electrical engineering from the Centro de Investigación y de Estudios Avanzados (CINVESTAV-IPN), Mexico City, in 2004.

In 2006, he was a Post-Doctoral Researcher with the Universitat Rovira i Virgili, Tarragona, Spain. From 2007 to 2008, he was a Post-Doctoral Researcher with the Microwave Laboratory, Université catholique de Lovain, Louvan-la-Neuve, Belgium. He is currently a Researcher with the Micro and Nanotechnology Research Center, Universidad Veracruzana, Veracruz, Mexico.

EMMANUEL TORRES RIOS received the M.Sc. and Ph.D. degrees in electronics from the National Institute of Astrophysics, Optics and Electronics, Mexico. He has been a full-time Professor with the Tecnologico de Monterrey, Puebla, since 2015. He has been a member of the National Researchers' System level 1 from CONACyT Mexico, since 2016. He won a one year Post-Doctoral Fellowships from the Canadian Government (CBIE) in 2011, and research in heterojunction transistor modeling with Queen's University. His research focuses on FET transistors modeling, S-parameter measurements, and dc device characterization.

OSCAR V. HUERTA-G. received the Ph.D. degree in electronics from the National Institute for Astrophysics, Optics, and Electronics in 2019, where he was a Research Assistant with the Department of Electronics from February to August 2019. Since September 2019, he has been with the Reliability Group, GlobalFoundries, Malta, NY, USA.