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Fabrication and Characterization of Stacked Poly-Si Nanosheet With Gate-All-Around and Multi-Gate Junctionless Field Effect Transistors

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ABSTRACT Present work demonstrates the vertically double stacked nanosheet (NS) p-channel polycrystalline silicon (poly-Si) junctionless field-effect transistors (JL-FET) with tri-gate, omega-gate, and gate all around (GAA) structure. These structures offer more W_{eff} per existing footprint and better parallel resistance, resulting in smaller total resistance. Also, the GAA stacked NS device shows superior electrical properties, including high Ion/Ioff ratio ($>10^8$), steep subthreshold swing (SS) = 100 mV/dec, very low drain-induced-barrier-lowering (DIBL) = 0.127 mV/V and usually off at Vg = 0 V, owing to superior gate controllability. More, the 3D TCAD simulation has applied for analysis of physical characteristics of the proposed devices.

INDEX TERMS Gate all around, junctionless, nanosheet, multi gate, stacked FET.

I. INTRODUCTION

Under the rapid growth of the electronics industry based on the evolution of integrated-circuit (IC) technology to provide improvements in cost per function as well as performance. As the MOSFET channel length is scaled down, the suppression of off-state leakage current and the short-channel effects (SCEs) becomes an increasingly tricky technological challenge in the traditional planar transistor. The SCEs emerge into transistors are the most difficult challenge to maintain it. To solve SCEs, multi-gate field-effect transistor (FET) structures have been developed, such as FinFETs [1], gate-all-around-FETs [2], and nanowire FETs [3]–[4]. The gate control ability of the channel can be enhanced, and the SCE and current leakage have reduced. The gate-all-around (GAA)-based nanosheets have the strongest gate controllability to lower the leakage current. Also, Junctionless field-effect transistors (JL-FET) with high and uniform doping in channel and source/drain regions have much attraction [5]–[11]. JL-FET can avoid complex source and drain doping engineering, has a low thermal budget for flexible high-k metal gate adoption and it is easily integrated for 3D IC and NAND. Recently, the vertically stacked nanosheet (NS) structure [12]–[18] can promote the device performance rather than increase the footprint as well as the suitable candidate for the next generation. Hence, this study proposes a vertically double stacked NS JL-FET with multi-gate and GAA structure, as it profoundly promises that it can extend FET to sub-5 nm nodes. For IMEC prediction, thin-film transistors (TFT) are small enough and temperature compatible to integrate on the back-end of line (BEOL) at the advanced node chips. The 3D monolithic BEOL TFT may implement in near future to continue Moore's law [19]. For multi stacked channel, poly-Si is most suitable channel material on SiO_2 underneath for 3D monolithic BEOL TFT, owing to its process simple and compatible proves.

II. DEVICE FABRICATION

Fig. 2 shows the process flows and the schematic diagram of vertically double stacked NS JL-FET with multi-gate

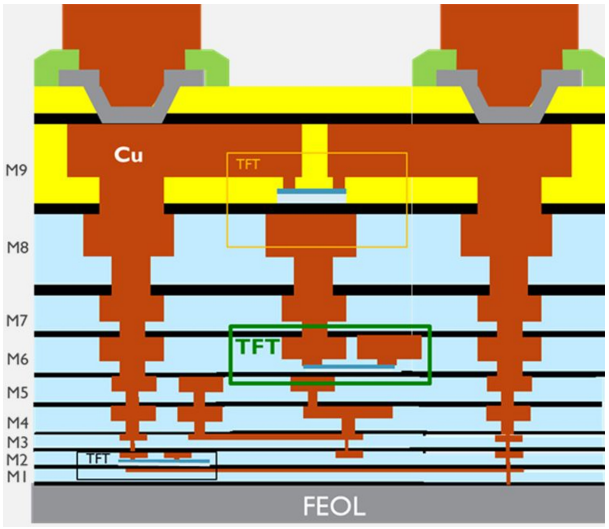

FIGURE 1. Thin-film transistors are small enough and temperature compatible to integrate on the BEOL at the advanced node chips [19].

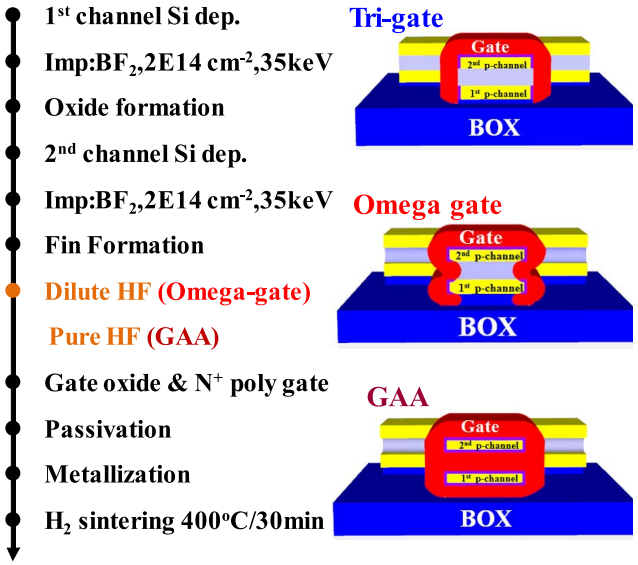

FIGURE 2. The schematic diagram and the process flows of stacked NS JL-FET with tri-gate, omega-gate, and GAA structure.

and GAA structure. Initially, a 400 nm-thick layer of the thick thermal SiO_2 layer was deposited on 6-inch bulk silicon wafers. Then, the amorphous silicon (α-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C. Next, the α-Si layer was annealed at 600°C for 24 hours in a nitrogen ambient to form the first poly-Si layer in solid-phase recrystallized (SPC) process. After SPC process, the first poly-Si layer was implanted with 35 keV boron difluoride (BF_2) ions at a dose of 2×10^{14} cm^{-2}, which was followed by furnace annealing at 600°C for 4 hours as first a p-type active layer. A 30 nm-thick SiO_2 layer deposited on the first poly-Si layer. Next, an α-Si layer was deposited as a second poly-Si layer by the SPC as mentioned above process. The second poly-Si

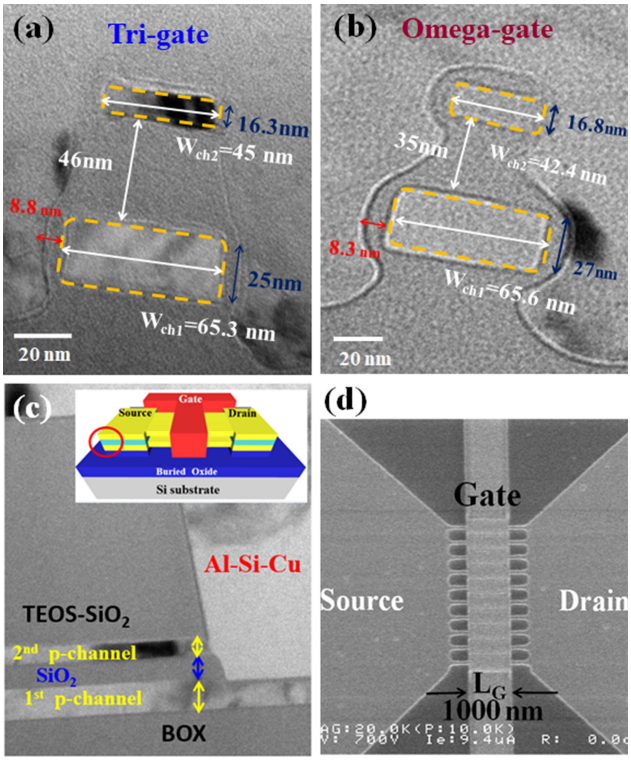

FIGURE 3. The cross-sectoinal TEM image of the stacked NS JL-FET with (a) tri-gate structure, (b) omega-gate structure and (c) source/drain contact of the stacked NS JL-FET device. (d) The top-view SEM image of the device with ten pieces of NS.

layer was defined by implanting as the same condition as a first poly-Si layer and furnace annealing at 600°C for 4 hours. The active layers of the vertically stacked channel were composed of two p-type channel and one inter later. The channel of nanosheet was patterned by electron beam lithography (EBL) and reactive ion etching (RIE). After that, the interlayer and the buried oxide were etched by dilute hydrofluoric acid (HF) to form the omega-gate structure, and pure HF to form the GAA structure. The dilute HF has low isotopically etching rate, we control the etching time (time mode) to form Omega gate. On the other hand, pure HF has high isotopically etching rate and we control the etching time to form the GAA channel profile [20]. Then, an 8 nm-thick thermal oxide was deposited by LPCVD as the gate oxide layer, and a 200 nm-thick in-situ doped N^+ poly-silicon was deposited as a gate electrode. The gate electrode was patterned by EBL and RIE. Subsequently, a 200 nm-thick tetraethylorthosilicate (TEOS) oxide layer was deposited as a passivation layer by LPCVD. EBL and RIE defined the contact window. Then, a 400 nm-thick Al-Si-Cu metallization was performed. Finally, all devices were sintered at 400°C for 30 minutes for repairing of a dangling bond.

III. RESULTS AND DISCUSSION

A. TRI-GATE AND OMEGA-GATE

Fig. 3 (a) shows the cross-sectional transmission electron microscopy (TEM) image of the stacked NS JL-FET with

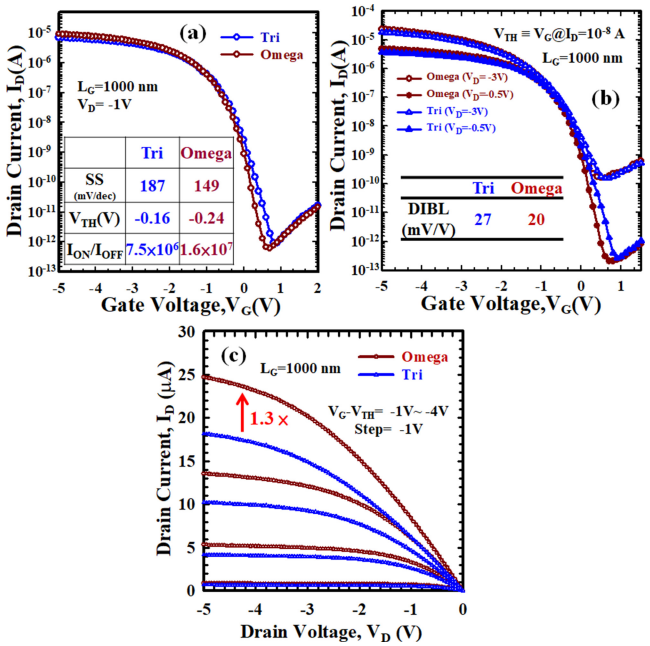

FIGURE 4. (a) The I_D-V_G curves of the tri-gate device, and omega-gate device. (b) The I_D-V_D characteristic of the tri-gate device, and omega-gate device at $V_D = -0.5$V, and -3V as $L_G = 1000$ nm. (c) The transfer I_D-V_D curves of the tri-gate device, and omega-gate device with different V_G-V_{TH} values.

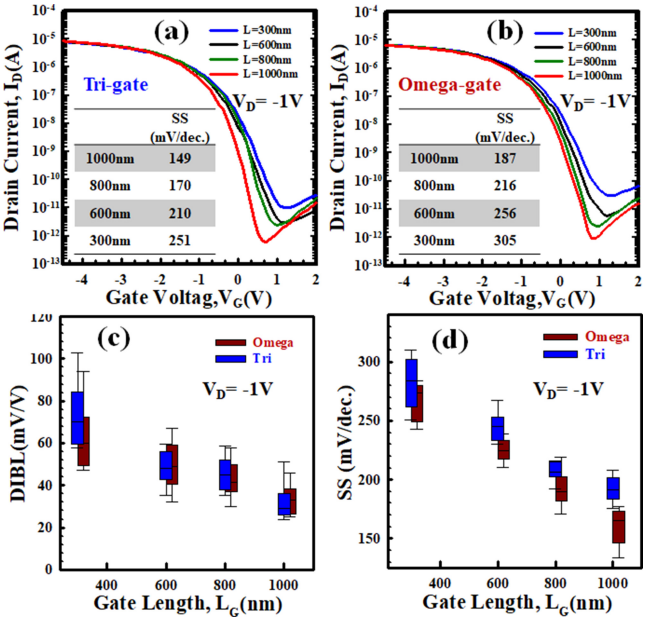

FIGURE 5. The L_G dependence on I_D-V_G curves of (a) the tri-gate device, and (b) the omega-gate device at $V_D = -1$ with L_G from 300 nm to 1000 nm. The statistically experimental value of (c) SS, and (d) DIBL at $V_D = -1$ with different L_G.

tri-gate structure. The first channel of the device has a width and height of 65.3 and 25 nm; the second channel is 45 and 16.3 nm. The gate oxide thickness is approximately 8.8 nm. The total W_{eff} of the stacked NS JL-FET with tri-gate is $(0.045 + 0.0163 \times 2 + 0.025 \times 2) \times 10 = 1.276$ μm. Fig. 3 (b) also shows a TEM image of the stacked NS JL-FET with omega-gate structure. The first channel of the device has a width and height of 65.6 and 27 nm; the second channel is 42.4 and 16.8 nm. The gate oxide thickness is approximately 8.3 nm. The total W_{eff} of the stacked NS JL-FET with omega-gate is $(0.0424 + 0.0168 \times 2 + 0.027 \times 2) \times 10 = 1.300$ μm. Fig. 3 (c) displays the TEM image of the source/drain contact of the stacked NS JL-FET device. These structures used the metal of Al-Si-Cu contact through the first channel and the second channel. Fig. 3 (d) shows the top-view SEM image of the device with ten pieces of NS.

Fig. 4 (a) presents the I_D-V_G curves of the stacked NS JL-FET devices at $V_D = -1$V and gate length (L_G) = 1000 nm. The subthreshold slope (SS) of the tri-gate device, and of the omega-gate device are 187 mV/dec, and 149 mV/dec, respectively. The V_{TH} of the tri-gate device, and of the omega-gate device are -0.16 V, and -0.24 V which are extracted by the constant current at $I_D = 10^{-8}$ A. The On/Off current ratio (I_{ON}/I_{OFF}) of the tri-gate device, and of the omega-gate device are 7.5×10^6, and 1.6×10^7, respectively. Fig. 4 (b) plots the transfer characteristic of the stacked NS JL-FET measures at $V_D = -0.5$ V, and -3 V. The drain-induced-barrier-lowering (DIBL) of the tri-gate device, and omega-gate device are 27 mV/V, and 20 mV/V which are extracted by the constant current method at $I_D = 10^{-8}$ A. Fig. 4 (c) presents the I_D-V_D characteristics of the tri-gate device, and omega-gate device. Comparing with the tri-gate device, the saturation current of the omega-gate device reveals 1.3 times of the saturation current at V_G-$V_{TH} = -4$ V and $V_D = -5$ V. As mentioned above, the result exhibits the stacked NS JL-FET with omega-gate shows the excellent electrical characteristics than tri-gate. Also, the device with omega-gate has higher saturation current is explained to its lower S/D parasitic resistance than the device with tri-gate. Hence, the DIBL of the tri-gate device is higher than omega-gate device due to the device with omega-gate has the superior gate controllability.

Fig. 5 (a)-(b) plots the L_G dependence on I_D-V_G curves of the tri-gate device, and omega-gate device at $V_D = -1$ V with L_G from 300 nm to 1000 nm. It reveals negative diversification with increasing L_G. Fig. 5 (c)-(d) shows the statistical DIBL and SS variation extracted from 20 devices of the tri-gate device, and omega-gate device. Squaring up the less electric field at channel edge to suppress barrier induced, the $V_{TH}$of p-type transistor is extracted by the constant-current method at $I_D = 10^{-8}$ A. The evidence shows the DIBL and SS of both devices have gradually increased the value from $L_G = 1000$ nm to 300 nm. As the SS increases from 187 mV/decade to 305 mV/decade for Tri-gate and from 149 mV/decade to 251 mV/decade for Omega-gate. The variation of SS and DIBL are not obvious in the long channel but are large in short channel of the vertically double stacked GAA NS JL-FET. As mentioned above characteristics, the stacked NS JL-FET with omega-gate structure shows the better gate controllability, such as

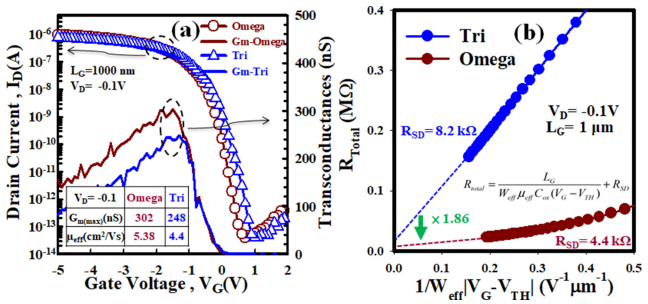

FIGURE 6. I_D-V_G curves and transconductance characteristics of the Tri-gate device and Omega-gate device with L_G = 1 μm at V_D = −0.1V and V_S = 0V. The Omega-gate device reveals a better transconductance (gm) than the Tri-gate device. The inserted plot shows mobility values. (b) Total Resistance (R_{total}) of the tri-gate and omega-gate stacked NS JL-FET devices as a function of gate voltage at V_D = −0.1 V.

high I_{ON}/I_{OFF}, steep SS, and low DIBL. Consequently, the stacked NS JL-FET with omega-gate structure can lower the leakage current at off-state and effectively suppress the short channel effects.

Fig. 6 (a) plots the transfer I_D-V_G characteristics and transconductance (Gm) of the tri-gate and omega-gate stacked NS JL-FET at $V_D = -0.1$ V. The Gm of the tri-gate device and omega-gate device are 248 nS and 302 nS, respectively. The tri-gate device and omega-gate device maximum field-effect mobility (μ_{eff}) were determined from the Gm as 4.4 cm^2/Vs and 5.38 cm^2/Vs, respectively. Fig. 6 (b) displays the total resistance (R_{total}) curves calculated based on the I_D-V_G characteristics. The normalized R_{SD} of the tri-gate and omega-gate contact devices were 8.2 kΩ and 4.4 kΩ where the X-axis was equal to 0, respectively.

Fig. 7 (a)-(b) indicates temperature dependence on I_D-V_G curves of stacked NS JL-FET with tri-gate, and omega-gate structure at $V_D = -1$ V with temperature from 50°C to 200°C, varied in steps of 25°C. These experimental results indicate positive variation with increasing temperature. Fig. 7 (c)-(d) plot the impact of temperature on the SS, and the V_{TH} of the tri-gate device, and omega-gate device extracted from 20 devices of the tri-gate device, and omega-gate device. Quasi, the SS is less sensitive to temperature in the omega-gate device. These results can be explained that omega-gate device has superior gate controllability and less occurrence of the thermal emission leakage current. Still, the statistical V_{TH} with different temperature exhibits a similar variation of both devices.

B. GATE-ALL-AROUND

Fig. 8 (a) shows the cross-sectional TEM image and Fig. 8 (b) shows scanning transmission electron microscopy (STEM) dark-field images of the stacked NS JL-FET with GAA structure. The first channel (bottom channel) of the stacked NS JL-FET has a width and height of 126.6 and 8.3 nm, respectively; the corresponding values for the second channel (top channel) are 96.6 nm and 7 nm. The gate oxide thickness of the stacked NS device is approximately 8.3 nm. The total W_{eff} of the stacked NS JL-FET is

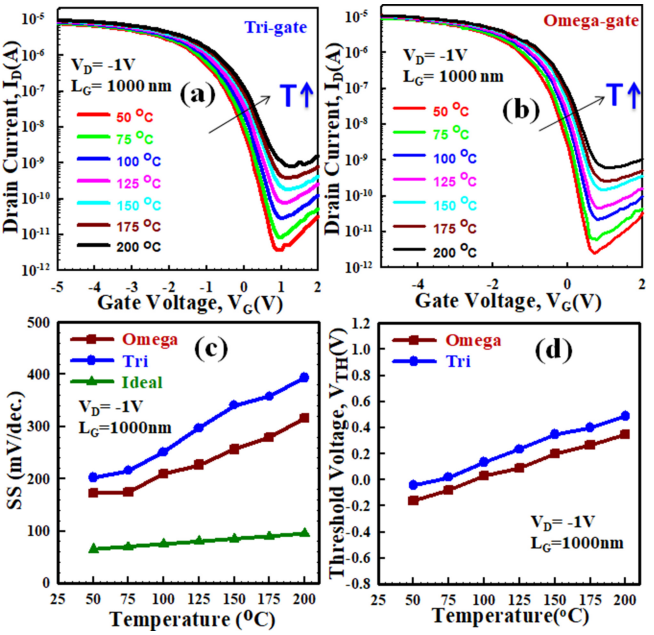

FIGURE 7. The temperature dependence on I_D-V_G curves of (a) the tri-gate device, and (b) the omega-gate device at V_D = −1 with temperature from 50°C to 200°C, varied in steps of 25°C. The statistically experimental value of (c) SS, and (d) DIBL at V_D = −1 with different temperature.

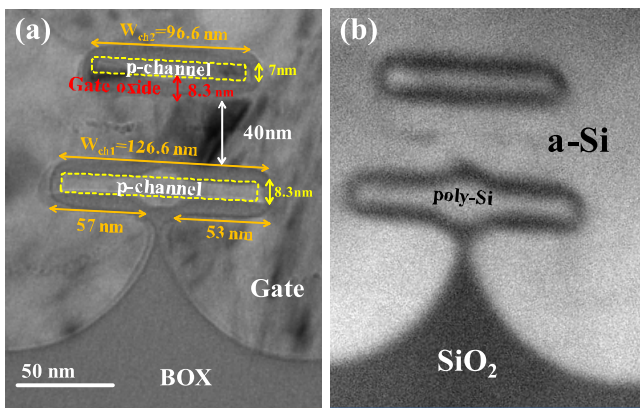

FIGURE 8. The cross-sectional (a) TEM image, and (b) STEM dark-field image of stacked NS JL-FET with GAA structure.

(0.0966×2+0.007×2+0.0083×2+0.057+0.053+0.1266)×10 = 4.604 μm. Also, the dark-field image of STEM has appeared with the high contrast, leading to discriminate Si as brightness and SiO_2 as darkness.

Fig. 9 (a) plots the I_D-V_G curves of the stacked NS JL-FET with GAA structure at $V_D = -1$ V. The subthreshold slope (SS) is 100 mV/decade, the threshold voltage (V_{TH}) is −1.3 V which is extracted by the constant current at $I_D = 10^{-8}$ A. Fig. 9 (b) plots of transfer I_D-V_G characteristics of the stacked NS JL-FET with GAA structure at $V_D = -1$ V, −0.5 V, and −3 V. The I_{ON}/I_{OFF} is 2.03×10^8 and the SS is 100 mV/decade for the stacked NS JL-FET with GAA structure at $V_D = -1$ V, and L_G = 1000 nm. As V_D is at −3 V and −0.5 V, the V_{TH} is −1.3057 V and −1.306 V.

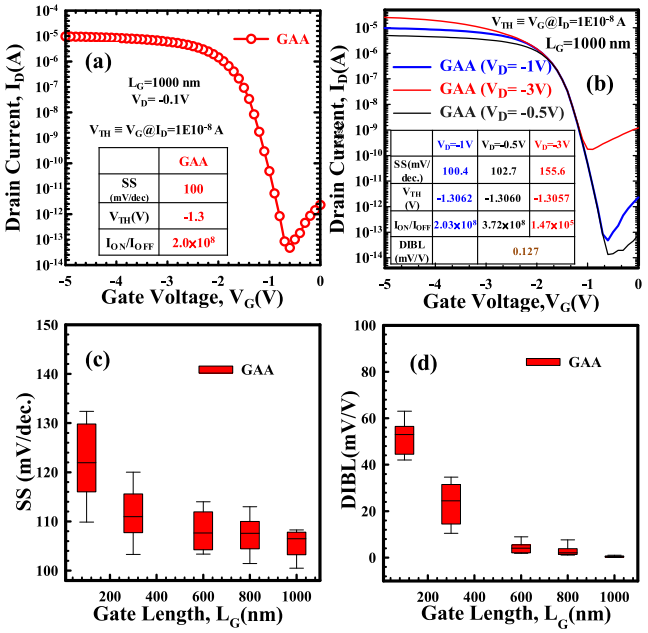

FIGURE 9. (a) The experimental I_D-V_G characteristics at $V_D = -0.1$ V and $L_G = 1000$ nm. (b) Comparison of the I_D-V_G curves of the stacked NS JL-FET with structure in $L_G = 1000$nm at $V_D = -1$ V, -0.5 V, -3 V. (c) The statistical SS, and (d) the DIBL variation extracted from 20 devices from $L_G = 100$ to 1000 nm at $V_D = -1$V of stacked NS JL-FET with GAA structure.

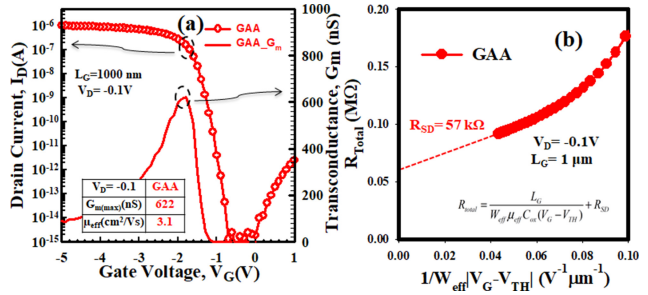

FIGURE 10. (a) I_D-V_G curves and transconductance characteristics of the GAA device with $L_G = 1$ μm at $V_D = -0.1$V and $V_S = 0$V. The inserted plot shows mobility values. (b) R_{total} of the GAA stacked NS JL-FET devices as a function of gate voltage at $V_D = -0.1$ V.

The V_{TH} is almost the same while the V_D is from low to high voltage. The DIBL value of the stacked NS JL-FET with GAA structure is 0.127 mV/V. Fig. 9 (c)-(d) show the statistical SS and DIBL variation extracted from 20 devices of the stacked GAA NS JL-FET from $L_G = 100$ nm to 1000 nm. The difference between SS and DIBL are not apparent in the long channel but are large in short channel of the stacked GAA NS JL-FET. As mentioned above characteristics, the stacked GAA NS JL-FET shows the strongest gate controllability, such as high I_{ON}/I_{OFF}, steep sub-threshold swing, and low DIBL. Hence, the stacked GAA NS JL-FET is capable of lowering the leakage current at off-state and effectively suppressing the short channel effects.

Fig. 10 (a) plots the transfer I_D-V_G characteristics and Gm of the GAA stacked NS JL-FET at $V_D = -0.1$ V. The Gm of the GAA device is 622 nS. The GAA device μ_{eff} was determined from the Gm as 3.1 cm^2/Vs. Fig. 10 (b) displays the R_{total} curves calculated based on the I_D-V_G characteristics. The normalized R_{SD} of the GAA contact devices were 57 kΩ where the X-axis was equal to 0.

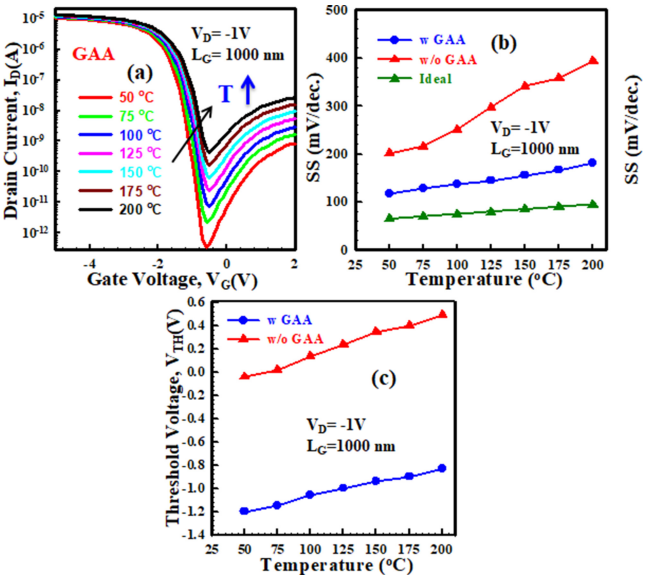

FIGURE 11. (a) The I_D-V_G curves of the stacked NS JL-FET with GAA at various temperatures from 50°C to 200°C and at $L_G = 1000$ nm, $V_D = -1$ V, (b) the statistical SS versus different temperature of the stacked NS JL-FET with GAA and without GAA, and (c) the statistical V_{TH} versus different temperature of the stacked NS JL-FET with GAA and without GAA.

TABLE 1. Comparison with the previous studies on Si GAA devices.

Symbol	Stacked GAA JL-FET	Ref.[21]	Ref.[20]	Ref.[22]
Si Crystalline	Poly	Poly	Mono	Mono
Junction Type	Junctionless	Junctionless	Inversion	Inversion
Number of Stacks	2	1	4	1
S.S.(mV/dec.)	~100	~99	~70	~121
DIBL(mV/V)	~0.13	~15.22	NA	NA
I_{ON}/I_{OFF} (V_G:V_D)	>10^8 (-3V:-0.1V)	>10^7 (3V:1V)	>10^4 (-3V:-1V)	>10^7 (5V:1V)

Fig. 11 (a) shows the temperature dependence on I_D-V_G curves of stacked NS JL-FET with GAA structure at $V_D = -1$ V with temperature from 50°C to 200°C, varied in steps of 25°C. These experimental results indicate positive variation with increasing temperature. Fig. 11 (b) shows the impact of temperature on SS of stacked NS JL-FET with GAA and without GAA. SS is less sensitive to temperature in the stacked NS JL-FET with GAA. These results can be explained that stacked NS JL-FET with GAA structure has superior gate controllability and less occurrence of the thermal emission leakage current. However, the statistical V_{TH} with different temperature has shown a similar variation of both structures in Fig. 11 (c).

The comparison with the previous studies on Si GAA devices are summarized in Table 1. The stacked GAA JL-FET in this work exhibits the lower DIBL

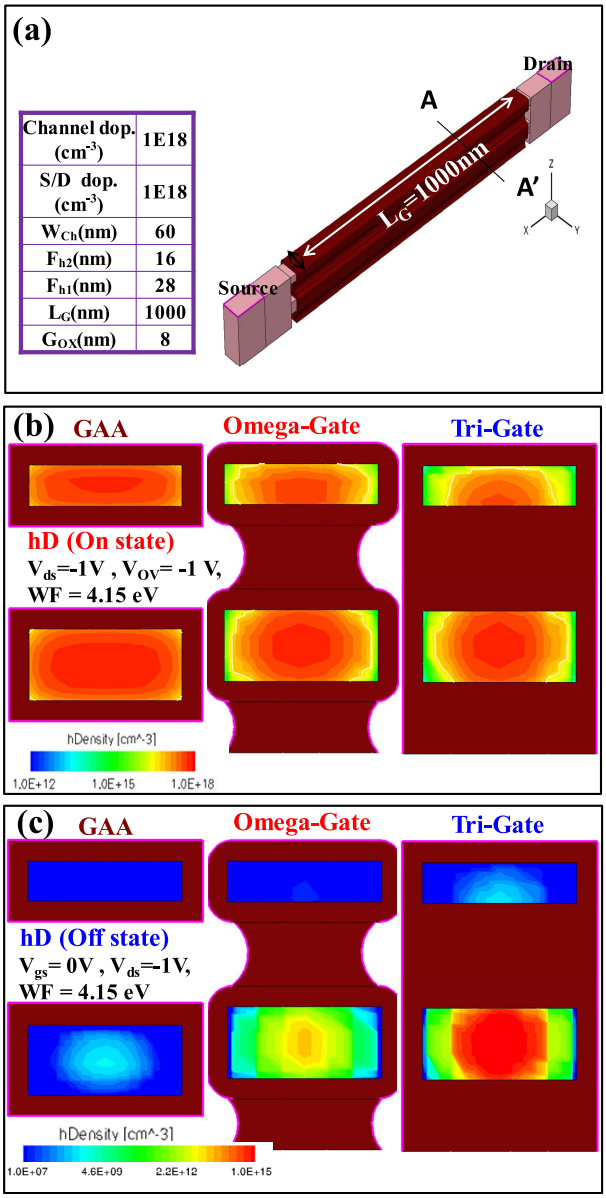

FIGURE 12. (a) The simulation 3D structure and the primary parameters of the stacked NS JL-FET with tri-gate, omega-gate, and GAA structure. The device hole concentration in (c) the on-state, and (c) the off-state.

and higher I_{ON}/I_{OFF} ratio compared with the previous studies [20], [21], [22].

C. TCAD SIMULATION

This part exhibits the simulation technique of 3D-TCAD [23] for the stacked NS JL-FET with tri-gate, omega-gate, and GAA structure. By using single NWs to stand for ten NWs of the real device as well as the dimensions of tri-gate, and omega-gate, and GAA devices are the same to compare the gate controllability in the stacked NS JL-FET. The primary parameters of the stacked NS JL-FET have shown in Fig. 12 (a). The TCAD doping concentration is defined to fit real experimental data. Besides Fig. 12 (b)-(c) presents the hole density distributions in the channel as the stacked NS device operate at on state ($V_{ds} = -1V$, $V_{OV} = -1V$) and off state ($V_{gs} = 0V$, $V_{ds} = -1V$) of both devices. The stacked NS JL-FET with GAA structure shows the best gate controllability. In off state, the GAA shows the lowest hole density which can adequately be depleted in the junctionless device. The results confirm the truth of body current for both on current and off current. Also, the GAA and NS structure ensures that lower leakage current at $V_{gs} = 0V$.

IV. CONCLUSION

In this study, the stack NS JL-FET based on a poly-Si channel with tri-gate, omega-gate, and GAA structure are successfully fabricated and characterized by a simple process. The stacked NS JL-FET with GAA structure also presents superior electrical performance and excellent gate controllability for fully depleting at off state. By utilizing a wider and stacked structure, the device performance can be enhanced to exceed what can be achieved using FinFET structure. Furthermore, the stacked NS JL-FET with GAA structure has shown the less sensitive to temperature than the stacked device without GAA structure. More, the result of TCAD-based comparative results on stacked NS JL-FET show GAA, which has better gate controllability due to the wider W_{eff}, maybe a trend for next-generation CMOS device. As mentioned above, this proposed device is a high potential for the monolithic multilayer 3D stacked integrated circuit applications for the next generation.

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