

Received 29 May 2019; revised 7 October 2019; accepted 20 October 2019. Date of publication 25 October 2019; date of current version 8 November 2019.
The review of this article was arranged by Editor C. Bulucea.

Digital Object Identifier 10.1109/JEDS.2019.2949566

Impact of Random Dopant Fluctuation on n-Type Ge Junctionless FinFETs With Metal–Interlayer–Semiconductor Source/Drain Contact Structure

SEUNG-GEUN JUNG AND HYUN-YONG YU ^{ID} (Member, IEEE)

School of Electrical Engineering, Korea University, Seoul 02841, South Korea

CORRESPONDING AUTHOR: H.-Y. YU (e-mail: yuhykr@korea.ac.kr)

This work was supported in part by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT, and Future Planning under Grant 2017R1A2B4006460, in part by the Nano Material Technology Development Program through NRF funded by the Ministry of Science, ICT and Future Planning under Grant 2015M3A7B7045490, in part by the Ministry of Trade, Industry & Energy, under Project 20003551, and in part by the Korea Semiconductor Research Consortium Support Program for the Development of the Future Semiconductor Device.

ABSTRACT The impact of random dopant fluctuation (RDF) on n-type Ge junctionless FinFETs (JLFETs) with metal–interlayer–semiconductor (MIS) source/drain (S/D) contact structure is firstly investigated via 3-D technology computer aided design (TCAD) simulations. The estimation and evaluation of standard deviations in threshold voltage (V_{th}), on-state current (I_{on}), off-state current (I_{off}), subthreshold swing (SS), and drain induced barrier lowering (DIBL) by different Ge nanowire doping concentrations and different heights for RDF effects are performed. The results show a decreasing trend of RDF with lower doping concentration of the device. Furthermore, the influence of MIS S/D on RDF of n-type Ge JLFET is assessed through a comparative analysis between an n-type Ge JLFETs with and without MIS S/D structure. The analysis results estimate that MIS S/D can reduce performance variation to approximately 0.0237 V for σV_{th} , 5.75×10^{-5} A/ μm for σI_{on} , 4.30×10^{-10} A/ μm for σI_{off} , 0.548 mV/dec for σSS , and 12.3 mV/V for DIBL, without severe performance degradation of the current nominal values. This estimation gives a significant insight on variability prediction of the 7 nm n-type Ge JLFET device with MIS S/D structure.

INDEX TERMS Junctionless FET, germanium, metal-inter layer-semiconductor source/drain, 3-D TCAD, random dopant fluctuation (RDF), line-edge roughness (LER).

I. INTRODUCTION

Junctionless field effect transistors (JLFETs) contain the same concentration of a single doping species across the semiconductor region, have been proposed as one of promising alternatives over conventional fin field-effect transistors (FinFET), which are more complicated to process and costlier to manufacture [1], [4]. Moreover, it is expected that the JLFETs can maintain scaling down of complementary metal-oxide-semiconductor (CMOS) technology owing to restrained short channel effects (SCEs) by increased effective channel length [1]–[8]. In addition, to improve device characteristics like on-state current, adopting new channel

materials as a favorable technique, for instance, in the case of non-silicon (non-Si)-based JLFETs, is being considered as of late [2]–[5], [9].

Germanium (Ge) is a feasible candidate, as it is known for its higher mobility and slightly better performance compared to Si when used in JLFETs [10]. Nevertheless, the typically used n-type Ge JLFET device with metal-semiconductor (MS) Source/Drain (S/D) structure faces the critical problem of severe Fermi-level pinning (FLP) near the valence band edge of Ge, as illustrated in Fig. 2(a). The high density of metal-induced gap states (MIGS) between the metal and the semiconductor stimulates the FLP, which

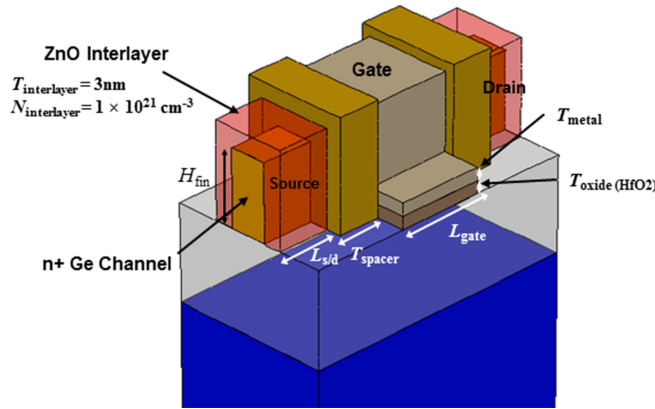


FIGURE 1. 3-D figure of the 7 nm n-type Ge JLFET with MIS S/D structure. Device structure is designed according to ITRS specification.

in turn triggers high Schottky barrier, occurring as a very large hole off-state current [11], [15], [16]. For this reason, the MS structure critically disturbs the n-type Ge JLFETs operating in enhancement-mode. Therefore, FLP should be considered in evaluating the realistic performance of n-type Ge JLFETs.

To overcome FLP phenomenon, the metal-interlayer-semiconductor (MIS) S/D structure has been suggested [3], [12]–[16]. This structure inserts an ultrathin interlayer between the metal and the semiconductor that decreases the density of MIGS, thereby, mitigating the FLP. Accordingly, with lower Schottky barrier, as shown in Fig. 2(b), the n-type Ge JLFETs with MIS S/D structure is enable to operate for enhancement-mode [3].

The electrical characteristics of JLFETs strongly depend on doping concentration and the dimension of semiconductor nanowires, so the sensitivity of their performance variation by random dopant fluctuation (RDF) is at a highly vulnerable position [6]–[9]. This calls as well for an imperative evaluation of this performance variability. In addition, as mentioned above, the effects of severe FLP on JLFET devices are worth considering during performance evaluation as the JLFET with and without MIS S/D structure shows big differences in current characteristics because of Schottky barrier and contact resistivity differences [3]. On this note, focusing on the variability evaluation of the new JLFET device which including MIS S/D is also important, finding proper range of channel doping concentration and demonstrating the impact of MIS S/D on variability.

In this study, performance variation by RDF of the n-type Ge JLFETs with MIS S/D structure is firstly demonstrated with 3-D technology computer aided design (TCAD) simulator. Next, we calculate the RDF standard deviation of the performance parameters, including threshold voltage (V_{th}), on-state current (I_{on}), off-state current (I_{off}), subthreshold swing (SS), and drain induced barrier lowering (DIBL) by different doping concentrations of Ge. Moreover, we calculate RDF effects by different device heights. Furthermore, the nominal values and RDF effects of n-Ge JLFET with

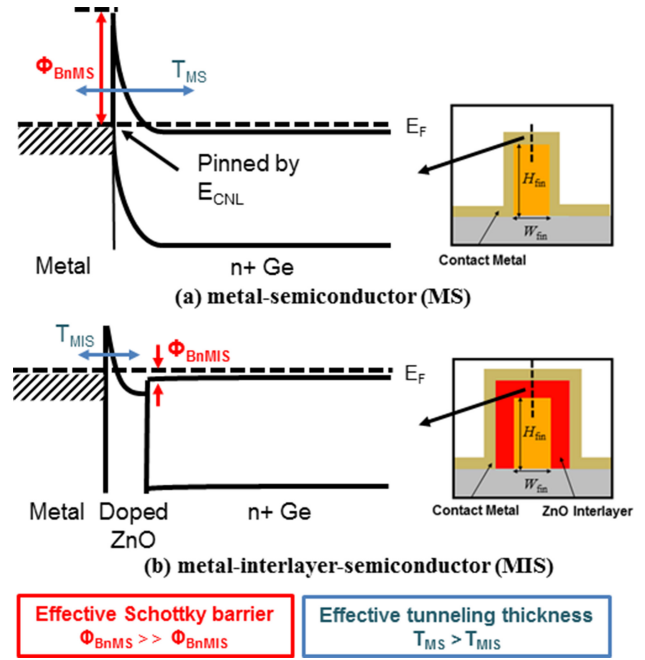


FIGURE 2. Band diagram of (a) metal-semiconductor (MS) and (b) metal-interlayer-semiconductor (MIS) S/D structure applied to the 7 nm n-type Ge JLFETs.

TABLE 1. Design parameters used in 7 nm n-type Ge JLFET.

Quantity	Value	Description
L_{gate}	14 nm	Physical gate length
T_{oxide}	2 nm	Gate oxide thickness
H_{fin}	12 nm	Fin height
W_{fin}	6 nm	Fin width
T_{inter}	3 nm	Interlayer thickness
N_{inter}	$1 \times 10^{21} \text{ cm}^{-3}$	Interlayer doping concentration
$L_{S/D}$	10 nm	Source/drain length
T_{spacer}	7 nm	Spacer thickness
V_{DD}	0.7 V	Power supply voltage

and without MIS S/D are compared to evaluate the impact of MIS S/D when RDF is applied.

II. DEVICE DESIGN AND SIMULATION METHOD

Based on electrical device performance and physical properties of 7 nm high performance logic technology in logic trend section of 2015 ITRS specification, n-type Ge JLFET with MIS S/D structure is implemented in Sentaurus 3-D TCAD with the same simulation structure as our previous work [3], [17]. Figure 1 shows a 3-D figure of the n-type Ge JLFET with the MIS S/D structure. The nanowire that maintains the doping concentration for all regions assumes fabrication from Ge on insulator (GOI). Table 1 shows the specific parameters of the device design. The Ge nanowire is set at default width and height of 6 nm and 12 nm, respectively, according to the ITRS specification. A 3 nm-thick zinc oxide (ZnO) is used as the interlayer (IL) for the MIS structure to provide small contact resistivity corresponding to the low conduction band offset [14]. The ZnO

TABLE 2. Channel doping concentrations and work functions used for the simulation of 7 nm n-type Ge JLFET.

Quantity	Value	Description
N_{channel}	$1 \times 10^{19} \text{ cm}^{-3}$	Ge channel doping concentration
	$2 \times 10^{19} \text{ cm}^{-3}$	
	$3 \times 10^{19} \text{ cm}^{-3}$	
Φ_m	4.83 eV	Work function of metal gate for different Ge doping concentration
	4.93 eV	
	5.03 eV	

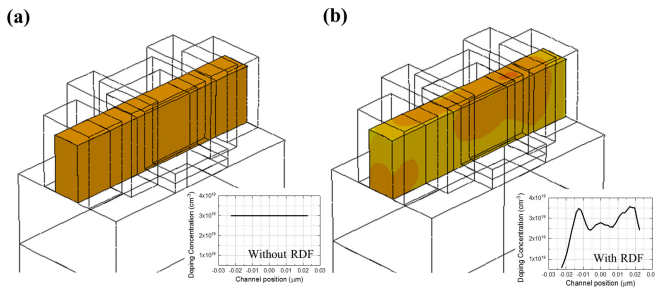


FIGURE 3. 3-D figure of a Ge channel (a) without and (b) with, RDF effect. Insets show the 1-D plot of the Ge channel doping concentration by channel position along the transport direction.

IL is doped for $1 \times 10^{21} \text{ cm}^{-3}$ doping concentration as it can provide lower contact resistivity due to the thinner effective tunneling thickness by band bending of heavily doped ZnO [13]. The gate dielectric oxide is made up of 2 nm-thick hafnium oxide (HfO_2), and the S/D metal used is titanium (Ti) due to the small difference between metal work function and Ge’s electron affinity. For the device physics, models of Jain–Roulston bandgap narrowing, drift-diffusion, density gradient quantization to realize the quantum confinement at the channel of Ge substrate, transverse electric field dependent mobility, doping dependence mobility, high field saturation mobility, and Shockley–Read–Hall doping dependence were employed to demonstrate the carrier transport behavior, while the Wentzel–Kramer–Brillouin (WKB) non-local tunneling model which is basic tunneling probability model at contact was applied for tunneling probability approximation at the MIS S/D structure.

To our simulated n-type Ge JLFET with MIS S/D structure, RDF effects are incorporated to the device for variability estimation. For comparison of each variability condition, a total of 200 samples of randomized profile which was typically used in published results were created [20]. Table 2 shows the parameters used in the variability simulation. The doping concentration of Ge nanowire is set within $1 \times 10^{19} \text{ cm}^{-3}$ to $3 \times 10^{19} \text{ cm}^{-3}$ to observe the change of RDF process variation by different doping concentrations. Note that Ge doping concentrations below $3 \times 10^{19} \text{ cm}^{-3}$ are required to meet the ITRS subthreshold swing target based on our previous work [6]. In case of the metal gate work function, it is calibrated to make the devices obtain off-state current of 1 nA/ μm ; for this reason, 4.83, 4.93, and 5.03 eV are applied for each Ge doping concentration. Figure 3 shows

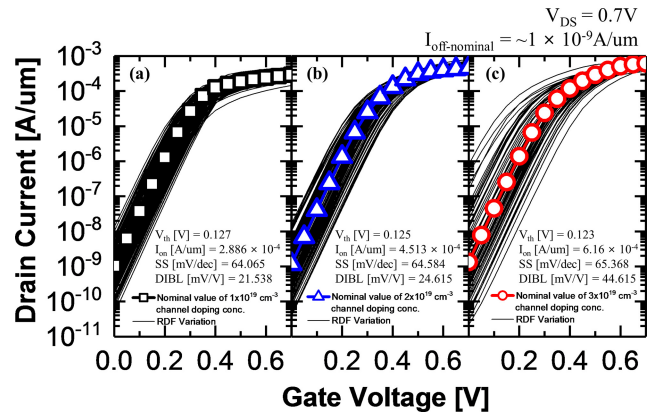


FIGURE 4. RDF 200 I_D - V_G simulations of n-type Ge JLFETs with MIS S/D structure by (a) $1 \times 10^{19} \text{ cm}^{-3}$, (b) $2 \times 10^{19} \text{ cm}^{-3}$, (c) $3 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentrations at drain voltage of 0.7 V and their nominal value.

the structure of the channel devices, including RDF effects. The Sano method was employed to generate randomized doping, considering the long-range coulomb potential of the number density associated with discrete dopant and the screening factor calculated with $2N^{1/3}$ (N is impurity concentration) [18]. The polarization effect near the interface between dielectric and germanium was ignored [20]. The parameters V_{th} , I_{on} , I_{off} , SS, and DIBL were compared for each condition.

III. RESULTS AND DISCUSSION

A. RDF EFFECTS OF N-TYPE GE JLFETS WITH MIS S/D STRUCTURE

The effects of RDFs on the device are evaluated through the generated 200 different randomized doping profile samples containing different Ge doping concentrations. Figure 4 shows the I_D - V_G curves of the simulations illustrating the RDF effects for a biased drain voltage of 0.7 V. The nominal values are extracted from the devices with different doping concentrations, with the same I_{off} of nominal value ($I_{\text{off-nominal}}$) for 1 nA/ μm , by modifying the gate metal work function to normalize the gate controllability of the devices near the off state. With lower Ge doping concentration, the simulated I_D - V_G profiles exhibits lower absolute variations as current values are more concentrated to nominal value. In general, the absolute value of RDF effects becomes severe with higher doping concentrations. In effect, not only conventional MOSFETs but also the n-type Ge JLFETs with MIS structure follows the tendency [14].

Based on the data provided by Fig. 4, we calculate the standard deviation (σ) of V_{th} , I_{on} , I_{off} , SS, and DIBL corresponding to the Ge doping concentrations by RDF, as shown in Fig. 5. General standard deviation (σ) calculation (the square root of the variance) is performed to quantify the amount of variation by RDF effect; σ increases with higher Ge doping concentration. Specifically, for a concentration of $1 \times 10^{19} \text{ cm}^{-3}$ to $3 \times 10^{19} \text{ cm}^{-3}$, σV_{th} is approximately 2.86 times higher for 0.0237–0.0677 V; σI_{on} varies from $5.75 \times 10^{-5} \text{ A/um}$ to $1.10 \times 10^{-5} \text{ A/um}$ (approximately

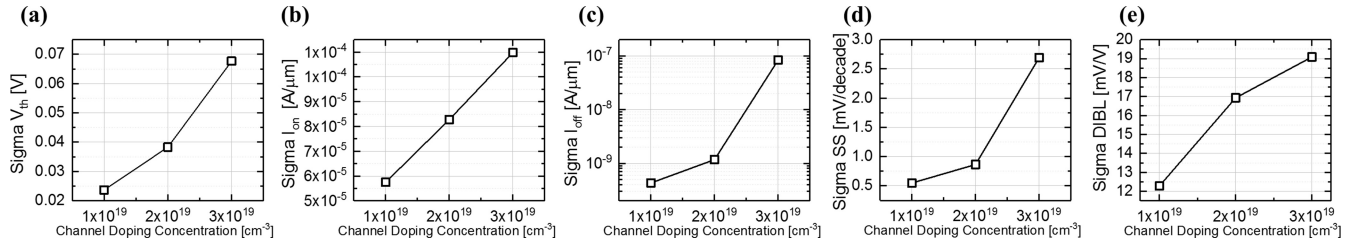


FIGURE 5. Standard deviation (σ ,sigma) of (a) V_{th} , (b) I_{on} , (c) I_{off} , (d) SS, and (e) DIBL by RDF effect by Ge doping concentration in the n-type Ge JLFET with MIS S/D structure.

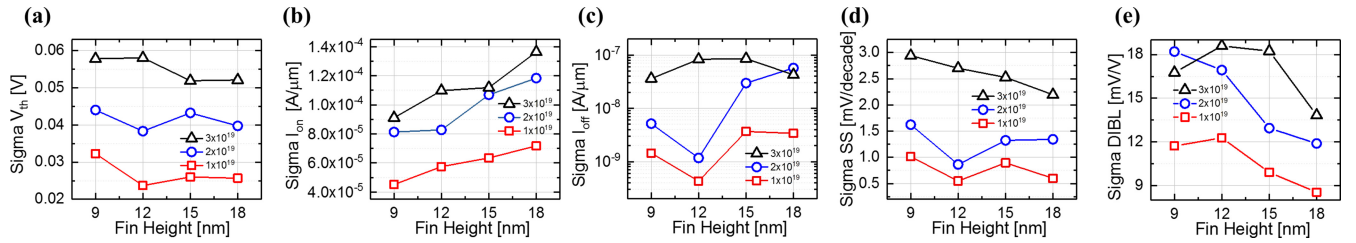


FIGURE 6. Standard deviation (σ) of (a) V_{th} , (b) I_{on} , (c) I_{off} , (d) SS, and (e) DIBL by RDF effect by different fin height and Ge doping concentration in the n-type Ge JLFET with MIS S/D structure.

TABLE 3. Standard deviation to mean ratio of the performance parameter variation caused by RDF effect with different Ge doping concentrations.

Quantity	$1 \times 10^{19} \text{ cm}^{-3}$ Ge doping conc.	$2 \times 10^{19} \text{ cm}^{-3}$ Ge doping conc.	$3 \times 10^{19} \text{ cm}^{-3}$ Ge doping conc.
$\sigma V_{th} / \mu V_{th}$	18.3%	29.6%	38.1%
$\sigma I_{on} / \mu I_{on}$	20.5%	18.6%	17.7%
$\sigma I_{off} / \mu I_{off}$	67.6%	109.0%	442.0%
$\sigma SS / \mu SS$	0.85%	1.33%	4.04%
$\sigma DIBL / \mu DIBL$	48.2%	60.2%	56.9%

1.91 times higher); σI_{off} changes from $4.30 \times 10^{-10} \text{ A}/\mu\text{m}$ to $8.31 \times 10^{-8} \text{ A}/\mu\text{m}$ (approximately 193 times higher); σSS ranges from 0.548 mV/dec to 2.69 mV/dec (approximately 4.91 times higher) and; $\sigma DIBL$ differed from 12.3 mV/V to 19.1 mV/V (approximately 1.55 times higher), for Ge doping concentration range of $1 \times 10^{19} \text{ cm}^{-3}$ to $3 \times 10^{19} \text{ cm}^{-3}$. Among these values, the rate of change for σI_{off} is much higher than for the other parameters.

The standard deviation of the performance parameter variation caused by the RDF effect is divided by their mean as shown in Table 3. Conventionally, σ depicts the absolute performance variation value, which has the same unit as performance value; on the other hand, σ -to-mean (μ) ratio has percentage units useful in comparing the relative variability for different devices, as well as for different performance values. From the table, σ/μ of V_{th} , I_{off} , and SS increases with higher Ge doping concentration, sharing the same tendency for absolute values in Fig. 5. In contrast, σ/μ of I_{on} decreases with higher Ge doping concentration, which means that the increment of μI_{on} is much higher than σI_{on} . Moreover, the peak value of $\sigma DIBL$ appears in $2 \times 10^{19} \text{ cm}^{-3}$ of Ge doping concentration. The difference in $\sigma I_{on} / \mu I_{on}$ and $\sigma DIBL / \mu DIBL$ between different concentrations is relatively smaller than for the other

parameters; thus, the mentioned singularity of the values of σI_{on} and $\sigma DIBL$ is not that significant when comparing variations for different Ge doping concentrations. Interestingly, for the same Ge doping concentration, $\sigma SS / \mu SS$ shows the minimum value, while $\sigma I_{off} / \mu I_{off}$ shows the maximum, implying extreme variability as compared to the other parameters.

Figure 6 shows the σ values of V_{th} , I_{on} , I_{off} , SS, and DIBL for fin heights of 9 nm to 18 nm. Note that, the variation for all fin heights increases with higher doping concentration, except for few points. Table 4 lists the σ/μ of RDF applied devices by fin height extracted from Fig. 6. The gate metal work function is modulated to obtain 1 nA/ μm off-state current for Ge doping concentration. No performance parameters show any clear tendency with fin height. For instance, σV_{th} in Fig. 6(a) roughly decreases with increased fin height, but in Table 4, σ/μ increases with higher fin for all Ge doping concentrations. Thus, the rate of μV_{th} decrement due to poor gate controllability is much higher than σV_{th} decrement for different heights. In contrast, in Fig. 6 (b) and (c), σI_{on} and σI_{off} relatively increases with higher fin but σ/μ shows the opposite tendency. Accordingly, for V_{th} , I_{on} , and I_{off} these trends can change depending on whether the absolute variation or the relative variation is important. Furthermore, σSS and $\sigma DIBL$ in Fig. 6 (d) and (e), respectively, share a tendency of decrease with σ/μ for increased fin height. Meanwhile, for the same Ge doping concentration and height, $\sigma I_{off} / \mu I_{off}$ has the highest value among the others, as in Table 4. Moreover, the 12 nm fin height gives lowest variation for σI_{off} , $\sigma I_{off} / \mu I_{off}$, σV_{th} , $\sigma V_{th} / \mu V_{th}$, σSS , and $\sigma SS / \mu SS$ in $1 \times 10^{19} \text{ cm}^{-3}$ and $2 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentrations. For $3 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration, the 18 nm fin height reflects minimum variation for I_{off} , SS, and DIBL.

TABLE 4. Standard deviation to mean ratio of the performance parameter variation caused by RDF effect with different height and Ge doping concentrations.

Quantity	9 nm	12 nm	15 nm	18 nm
$1 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration				
$\sigma V_{th}/\mu V_{th}$	20.9%	18.3%	22.4%	23.8%
$\sigma I_{on}/\mu I_{on}$	22.6%	20.5%	16.9%	15.1%
$\sigma I_{off}/\mu I_{off}$	164%	67.6%	143%	105.0%
$\sigma SS/\mu SS$	1.57%	0.85%	1.4%	0.93%
$\sigma DIBL/\mu DIBL$	47.0%	48.2%	36.8%	35.5%
$2 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration				
$\sigma V_{th}/\mu V_{th}$	27.9%	29.6%	42.5%	41.0%
$\sigma I_{on}/\mu I_{on}$	25.6%	18.6%	18.1%	16.4%
$\sigma I_{off}/\mu I_{off}$	350.0%	109.0%	302%	378.0%
$\sigma SS/\mu SS$	2.48%	1.33%	2.03%	2.07%
$\sigma DIBL/\mu DIBL$	54.1%	60.2%	51.5%	41.2%
$3 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration				
$\sigma V_{th}/\mu V_{th}$	35.9%	38.1%	58.4%	70.0%
$\sigma I_{on}/\mu I_{on}$	22.6%	17.7%	14.8%	14.5%
$\sigma I_{off}/\mu I_{off}$	696%	442.0%	273%	155.0%
$\sigma SS/\mu SS$	4.37%	4.04%	3.78%	3.29%
$\sigma DIBL/\mu DIBL$	53.0%	56.9	55.3%	45.2%

B. IMPACT OF MIS S/D STRUCTURE ON RDF EFFECTS OF N-GE JLFET

To verify the impact of MIS S/D on RDF-induced variation, the RDF influence and performance of n-Ge JLFET with MIS S/D for $1 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration are compared with the unpinned MS S/D for $3 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration. For the n-Ge JLFET with MIS S/D structure, a doping concentration of $1 \times 10^{19} \text{ cm}^{-3}$ is selected, which shows the σV_{th} below 25 mV (Fig. 5), the extracted value for our device dimension from Pelgrom plot of V_{th} variation for industry’s 14 nm technology node logic FinFET devices [19]. For the unpinned S/D structure, a Schottky barrier of 0.3 eV is employed to assume FLP alleviation. Figure 7 shows the nominal values of n-Ge JLFETs with unpinned MS S/D and MIS S/D. Comparing the performance of both devices, n-Ge JLFET with MIS S/D shows approximately 9.5% I_{on} and 19% I_{off} degradation, and nearly 1.2% SS and 20% DIBL enhancement relative to the device with unpinned MS S/D. These values are much lower than the current degradation rate of the device with unpinned MS S/D for $3 \times 10^{19} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration: approximately 34.2% I_{on} and 97.9% I_{off} degradation (not shown for brevity). Therefore, using MIS S/D structure on n-Ge JLFET contributes to much lower current degradation.

Furthermore, as shown in Fig. 5, decreasing Ge doping concentration can restrain the RDF performance variation of n-Ge JLFETs, but severe current degradation by doping dependent mobility could occur [14]. However, decreasing Ge doping concentration makes hard to maintain on-state current as the device acts as a rectangular cuboid resistor and the carriers uniformly flow in the entire area of the fin in on-state [3], [8]. However, a MIS S/D would enable the n-Ge JLFET to maintain an on-state current, with performance

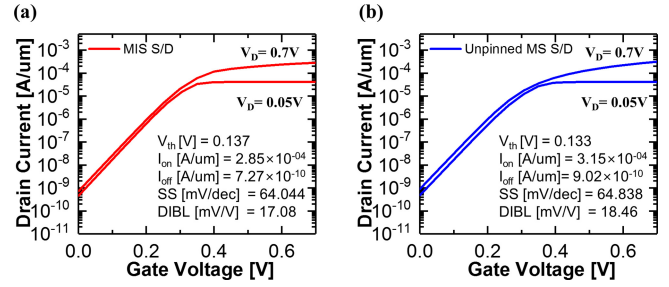


FIGURE 7. Nominal I_D - V_G simulations of n-type Ge JLFETs with (a) unpinned MS S/D structure for $3 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration and (b) MIS S/D structure for $1 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration. The drain bias voltages are selected for 0.7 V and 0.05V.

TABLE 5. Standard deviation comparison between n-Ge JLFET with unpinned MS S/D for $3 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration and MIS S/D for $1 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration.

Quantity	Unpinned MS S/D	MIS S/D
σV_{th} [V]	0.0555	0.0237
σI_{on} [A/um]	9.86×10^{-5}	5.75×10^{-5}
σI_{off} [A/um]	2.62×10^{-8}	4.30×10^{-10}
σSS [mV/dec]	1.43	0.548
$\sigma DIBL$ [mV/V]	33.4	12.3

almost similar to that of n-Ge JLFET with unpinned MS S/D, due to its lower contact resistivity, as described in our previous work [3]. The results in Fig. 7 show that using MIS S/D, instead of the unpinned MS S/D, could effectively reduce the Ge doping concentration with restrained I_{on} , I_{off} degradation and SS, DIBL enhancement.

Besides low performance degradation, n-Ge JLFET with MIS S/D structure shows reduced performance variations. To recall with Fig. 3(a), the $3 \times 10^{19} \text{ cm}^{-3}$ Ge doped n-Ge JLFET with unpinned MS S/D shows estimated RDF standard deviations of 0.0555 V for σV_{th} , 9.86×10^{-5} A/um for σI_{on} , 2.62×10^{-8} A/um for σI_{off} , 1.43 mV/dec for σSS , and 33.4 mV/V for $\sigma DIBL$. On the other hand, using the MIS S/D structure for the $1 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration produced approximate variations of 0.0237 V for σV_{th} (reduced by nearly 57.3%), 5.75×10^{-5} A/um for σI_{on} (reduced by roughly 41.6%), 4.30×10^{-10} A/um for σI_{off} (reduced by approximately 98.4%), 0.548 mV/dec for σSS (reduced by almost 61.7%), and ~ 12.3 mV/V for $\sigma DIBL$ (reduced by almost 63.2%) in table 5. As a result, the MIS S/D structure effectively lowered the RDF effects.

IV. CONCLUSION

The impact of RDFs on n-type Ge JLFETs with MIS S/D structure is firstly investigated through 3D TCAD. For the RDF process, σ and σ/μ for V_{th} , I_{on} , I_{off} , SS, and DIBL at different doping concentrations are calculated. When RDF is applied, σ and σ/μ for all performance parameters, except for $\sigma I_{on}/\mu I_{on}$, increased with increasing Ge doping concentration. Specifically, for the same doping concentration, $\sigma I_{off}/\mu I_{off}$ shows the maximum variability, while $\sigma SS/\mu SS$

showed the minimum. When RDF is compared by varying fin heights, σ and σ/μ ratio of V_{th} show an increasing tendency with higher fin, while those of I_{off} , SS, and DIBL share an opposite tendency; nevertheless, no clear pattern is observed with fin height for all parameters. Furthermore, a Ge doping concentration below $1 \times 10^{19} \text{ cm}^{-3}$ is recommended as compared to the Pelgrom plot of industry's logic FinFET devices in terms of V_{th} variation.

Additionally, the impact of MIS S/D on RDF of n-Ge JLFET at $1 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration is evaluated against MS S/D for $3 \times 10^{19} \text{ cm}^{-3}$ Ge doping concentration. As a result, compared to MS S/D, MIS S/D can reduce performance variation by 57.3% for σV_{th} , 41.6% for σI_{on} , 98.4% for σI_{off} , 61.7% for σSS , and 63.2% for DIBL without severe performance degradation of current values, and with enhanced SS and DIBL. This confirms that MIS S/D structure has RDF immunity, aside from its capacity to enable n-Ge JLFET operation in enhancement-mode.

ACKNOWLEDGMENT

The EDA tool was supported by the IC Design Education Center (IDEC), South Korea.

REFERENCES

- [1] J.-P. Colinge *et al.*, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, pp. 225–229, Feb. 2010.
- [2] Y. Kamata *et al.*, "Superior cut-off characteristics of $L_g=40 \text{ nm}$, $W_{fin}=7 \text{ nm}$ poly Ge junctionless Tri-gate FET for stacked 3D circuits integration," in *VLSI Symp. Tech. Dig.*, Jun. 2013, pp. T94–T95.
- [3] S.-G. Jung, S.-H. Kim, G.-S. Kim, and H.-Y. Yu, "Effects of metal–interlayer–semiconductor source/drain contact structure on n-type germanium junctionless FinFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3136–3141, Aug. 2018.
- [4] Y.-R. Jhan, V. Thirunavukkarasu, C.-P. Wang, and Y.-C. Wu, "Performance evaluation of silicon and germanium ultrathin body (1 nm) junctionless field-effect transistor with ultrashort gate length (1 nm and 3 nm)," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 654–656, Jul. 2015.
- [5] R. Yu *et al.*, "Device design and estimated performance for p-type junctionless transistors on bulk germanium substrates," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2308–2313, Sep. 2012.
- [6] N. D. Akhavan, G. A. Umana-Membreno, R. Gu, J. Antoszewski, and L. Faraone, "Random dopant fluctuations and statistical variability in n-channel junctionless FETs," *Nanotechnology*, vol. 29, no. 2, Dec. 2017, Art. no. 025203.
- [7] A. Koukab, "On threshold voltage modeling and variability in junctionless nanowires FETs," in *Proc. Electron Devices Solid State Circuit (EDSSC)*, 2012, pp. 1–2.
- [8] G. Leung and C. O. Chui, "Interactions between line edge roughness and random dopant fluctuation in nonplanar field-effect transistor variability," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3277–3284, Oct. 2013.
- [9] S. M. Nawaz, S. Dutta, and A. Mallik, "A comparison of random discrete dopant induced variability between Ge and Si junctionless p-FinFETs," *Appl. Phys. Lett.*, vol. 107, no. 3, Jul. 2015, Art. no. 033506.
- [10] P. Razavi, G. Fagas, I. Ferain, R. Yu, S. Das, and J. P. Colinge, "Influence of channel material properties on performance of nanowire transistors," *J. Appl. Phys.*, vol. 111, no. 12, pp. 1–8, Jun. 2012.
- [11] T. Nishimura, K. Kita, and A. Toriumi, "Evidence for strong Fermi-level pinning due to metal-induced gap states at metal/germanium interface," *Appl. Phys. Lett.*, vol. 91, no. 12, Sep. 2007, Art. no. 123123.
- [12] S. Gupta, P. P. Manik, R. K. Mishra, A. Nainani, M. C. Abraham, and S. Lodha, "Contact resistivity reduction through interfacial layer doping in metal–interfacial layer–semiconductor contacts," *J. Appl. Phys.*, vol. 113, no. 23, Jun. 2013, Art. no. 234505.
- [13] J.-K. Kim *et al.*, "The efficacy of metal–interfacial layer–semiconductor source/drain structure on sub-10-nm n-type Ge FinFET performances," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1185–1187, Dec. 2014.
- [14] C. Shin *et al.*, "Random dopant fluctuation-induced threshold voltage variation-immune Ge FinFET with metal–interlayer–semiconductor source/drain," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4167–4172, Nov. 2016.
- [15] G.-S. Kim *et al.*, "Effect of hydrogen annealing on contact resistance reduction of metal–interlayer–n-germanium source/drain structure," *IEEE Electron Device Lett.*, vol. 37, no. 6, pp. 709–712, Jun. 2016.
- [16] G.-S. Kim *et al.*, "Effective Schottky barrier height lowering of metal/n-Ge with a TiO₂/GeO₂ interlayer stack," *ACS Appl. Mater. Interfaces*, vol. 8, no. 51, pp. 35419–35425, Dec. 2016.
- [17] *International Technology Roadmap for Semiconductors (ITRS)*, ITRS, Denver, Co, USA, 2015. [Online]. Available: <http://public.itrs.net/>
- [18] N. Sano, K. Matsuzawa, M. Mukai, and N. Nakayama, "On discrete random dopant modeling in drift-diffusion simulations: Physical meaning of 'atomistic' dopants," *Microelectron. Rel.*, vol. 42, no. 2, pp. 189–199, Feb. 2002.
- [19] M. D. Giles *et al.*, "High sigma measurement of random threshold voltage variation in 14nm logic FinFET technology," in *VLSI Symp. Tech. Dig.*, Jun. 2015, pp. T150–T151.
- [20] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov, "Simulation study of individual and combined sources of intrinsic parameter fluctuations in conventional nano-MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 3063–3070, Dec. 2006.
- [21] A. R. Brown, G. Roy, and A. Asenov, "Poly-Si-gate-related variability in decananometer MOSFETs with conventional architecture," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 3056–3063, Nov. 2007.
- [22] N. Sano, K. Yoshida, C.-W. Yao, and H. Watanabe, "Physics of discrete impurities under the framework of device simulations for nanostructure devices," *Materials*, vol. 11, no. 12, pp. 2559–2571, Dec. 2018.



SEUNG-GEUN JUNG received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2016, where he is currently pursuing the Ph.D. degree.

His current research interests include CMOS and memory technology.



HYUN-YONG YU received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2002, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 2009.

He has been a Professor with the Department of Electrical Engineering, Korea University, since 2012.