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Leading-Edge Thin-Layer MOSFET Potential Modeling Toward Short-Channel Effect Suppression and Device Optimization

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ABSTRACT A novel compact model has been developed, which considers the origin of the short-channel effect (SCE) on the basis of the potential distribution along the channel. Thus an enlargement of the insight into SCE suppression in advanced thin-layer MOSFETs is enabled. The model is extended to include the diffusion region resistance effects caused by the drain-side doping by applying the methodology of the industry-standard high-voltage MOSFET model HiSIM_HV. Usage for studying possible device optimizations revealed that clear improvements in the subthreshold characteristics due to suppression of SCEs can be achieved by slightly increasing the drain-side diffusion resistance. Disadvantageous effects on the device and circuit performances were found to be negligible.

INDEX TERMS Short channel transistor, compact modeling, double-gate MOSFET, subthreshold characteristics.

I. INTRODUCTION

Scaling-down of the MOSFET size continues further to fulfill in particular low-power and increased integration-density requirements. For the high integration densities, 3D chip-bonding techniques have also been developed [1]–[7]. In addition to the integration-density increase, however, a device-performance enhancement is of course desirable. As solutions for both requirements, thin-layer MOSFETs have been developed such as extremely thin SOI MOSFET (ETSOI) [8]–[12], multi-gate MOSFETs (MG-MOS) with thin silicon layer-thickness (t_S) [13]–[17], or FinFETs [13], [18]–[21]. Nevertheless, even such very thin layer devices are still suffering from the short-channel (SC) effects in spite of an aggressive substrate-thickness reduction [22]–[25]. Our present investigation aims at analyzing the reasons for the SC effects observed in these leading-edge device technologies and at developing a device-optimization scheme for enabling further suppression of the SC effects. The focus is given on MG-MOSFETs, which provide the common structure for any type of thin-layer MOSFETs.

The scaling rule of $L/t_S \approx 2.5$, where L is the channel length and t_S is the substrate thickness, has been proposed for MG-MOSFETs and has been verified to preserve the principle MOSFET function of the gate control [26]. By reducing L, the potential distribution along the channel direction becomes non-negligible. Several analytical models usually applied a semi-parabolic function of the potential distribution to describe the SC effects along the channel, leading to the traditional solution originally developed by Young 30 years ago [27], [28]. We have developed a compact description of the SC effects by considering the complete channel-potential distribution, which results from the superposition of the contributions due to source/channel junction, channel part controlled by gate, and channel/drain junction [29]. This SCE-model has been verified to reproduce the SC effects

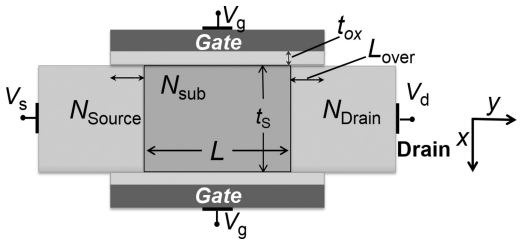

FIGURE 1. DGMOS device structure and main device parameters.

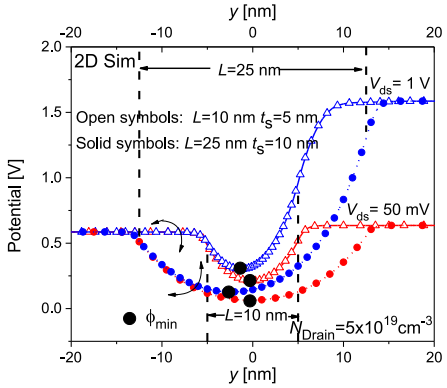

FIGURE 2. 2D numerical device simulation results of potential distributions in the middle of the substrate along the channel of the studied scaled devices at the gate voltage V_{gs} of −0.2V with channel lengths L of 10nm and 25nm.

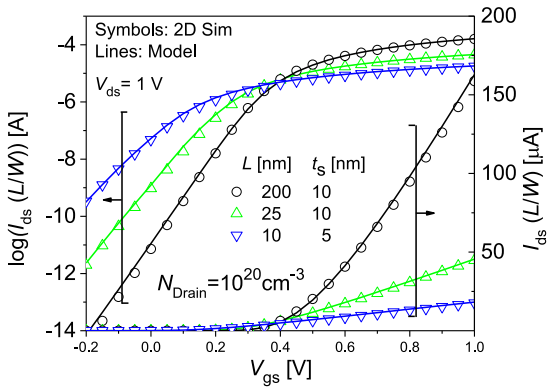

FIGURE 3. Drain current characteristics for different scaled technologies normalized by the channel length L and the width W. Device parameters are listed in Table 1.

TABLE 1. Device parameters used in simulations.

Symbol	Quantity	Value
L	Channel length	200, 25, 10 nm
W	Channel width	1 μm
t_S	Silicon thickness	10, 5 nm
t_{ox}	Equivalent Oxide Thickness	1.5 nm
L_{over}	Gate overlap length	10 nm
N_{sub}	Channel doping concentration	10^{15} cm^{-3}
N_{Source}	Source doping concentration	10^{20} cm^{-3}
N_{Drain}	Drain doping concentration	1×10^{20}, 5×10^{19} cm^{-3}

accurately. Here we extend our previous SCE-model [30], for inclusion of the diffusion resistance effects, which is realistic for actually fabricated devices. Change in drain doping concentration N_{Drain} leads to an increase/decrease of the resistance in the drain-side diffusion region. The double-gate (DG) MOS is applied as a specific MG-MOS for the quantitative optimization, because the gate contributions from other sides is usually not large and most of the device performance is determined by the control from two opposite gates. The present investigation is based on 2D numerical device simulations [31], where microscopic physical insights are available for any structural variations. The developed extended SCE-model is implemented into HiSIM, an industry-standard compact model developed on the basis of the complete potential distribution [32]. An improved device structure is studied, which has a reduced drain doping concentration respect to the highly doped region typically used. Device optimization is achieved in order to reduce the impact of the SC effects without seriously affecting the ON-state performance of the transistor. Important parameters, such as Subthreshold-slope (*SS*), Drain Induced Barrier Lowering (*DIBL*), OFF/ON-state current (I_{OFF}/I_{ON}), effective current (I_{eff}), maximum transconductance ($g_{m,max}$), output conductance (g_{ds}) are compared to analyze the improvements obtained after optimization.

This paper is organized as follows: Section II presents main performance features of the studied DG-MOSFET. The compact SCE-model development is reported in Section III. The device optimizations for suppressing the SC effects are presented and discussed in Sections IV and V. Finally, Section VI concludes our investigation.

II. DEVICE AND PERFORMANCE CHARACTERISTICS

The studied DG-MOSFET structure is depicted in Fig. 1 together with the main device parameters. Table 1 lists the device-parameter values used in this work. High impurity concentrations at source (N_{Source}) and drain (N_{Drain}) diffusion regions are normally important to keep the device operation within ideal conditions by avoiding the resistance effects. A high impurity concentration in the diffusion regions induces only negligible potential drop within these regions, resulting also in a negligible depletion extensions into the source/drain diffusion regions. The potential distribution along the channel direction in the middle of the substrate in depth, obtained from 2D device simulation results, is shown in Fig. 2 for two different channel lengths L. The resulting *I-V* characteristics of 2D device simulations are depicted in Fig. 3 for different L lengths for studied devices (see Fig. 1). It can be seen that the subthreshold slope is still further degraded, even when L is scaled down together with an additional t_S reduction. The potential distribution within the substrate along the channel is confirmed to accurately describe the SC effects.

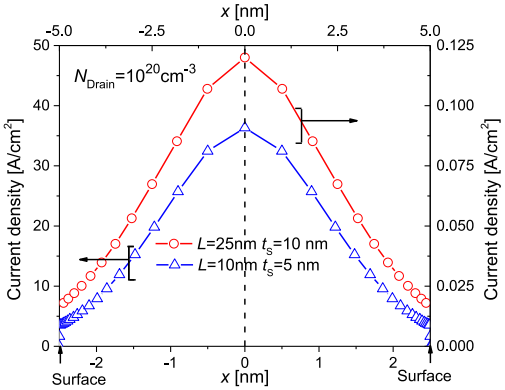

FIGURE 4. Current densities across the substrate between the 2 gate surfaces in the middle of the channel $y = 0$, at $V_{gs} = -0.2$V and $V_{ds} = 50$ mV.

TABLE 2. Analytical description and explanations used in model equations.

Parameter	Quantity	Value
A_0	Potential gradient	$(V_{biSource} - \phi_{min}) / (L_0/2)^3$
B_0	Position of potential minimum	y_{min}
C_0	Potential minimum	ϕ_{min}
L_0	Minimum long-channel length that preserves no subthreshold degradation	Value to extract.
y_{sym}	Auxiliary variable	$L/2 - \frac{2\cdot(V_{biDrain} - V_{biSource})}{E_{Source} + E_{Drain}}$
y_{min}	Potential minimum position	$-L/4 + y_{sym}/2$
$V_{biSource}$	Built in potential at source/channel junction	
$V_{biDrain}$	Built in potential at drain/channel junction	

III. COMPACT SCE MODELING AND ITS VERIFICATION

A. BASIC MODELING OF SC EFFECTS

As can be concluded from Fig. 4 the main origin of the SC effects is the deeper current flow in the x direction around the middle of the substrate. The ratio of this current flow deeper in the substrate diminishes according to the gate voltage V_{gs} increase, namely according to the formation of an inversion layer at surface. A relatively large source-drain leakage current occurs around the substrate middle when the unavoidable electric field, induced between source and drain diffusion regions, exceeds the field induced by V_{gs}, which then leads to a punch-through effect. In principle the lateral-electric-field contribution can be modeled by considering the 2D Poisson equation

$$\frac{d^2\phi(x,y)}{dx^2} + \frac{d^2\phi(x,y)}{dy^2} = \frac{qN_{sub}}{\varepsilon_S} \tag{1}$$

where $\phi(x,y)$ is the potential at the channel position (x, y), and ε_S is the semiconductor permittivity. A compact SCE-model has been developed by focusing on the potential distribution along the channel at the depth where the maximum-current flow occurs. For modeling this potential distribution, the overlap of the two junction distributions, one at source/channel and other at channel/drain, and the gate-control induced potential determined by V_{gs} are superimposed. The resulting total potential distribution for a long-channel transistor is approximated by a cubic function of position y

$$\phi(y) = A_0 \cdot (y + B_0)^3 + C_0 \tag{2}$$

where, A_0, B_0 and C_0 are model parameters, which are mostly determined by the junction profile. Thus the values of these model parameters are written as a function of the electric field induced in the junctions summarized in Table 2. By reducing the channel length the two potential distributions at the junctions start to overlap, which leads to an increase of the minimum potential ϕ_{min} along the channel (see Fig. 2). This described mechanism is exactly the origin of the SC effects. The final SCE-model equations are [29].

$$\Delta\phi_{min}(V_{gs}, V_{ds}, L) = -2 \cdot A_0 \cdot \left(y_{min} - \frac{L_0 - L}{2}\right)^3 \tag{3}$$

where $\Delta\phi_{min}$ is the potential-minimum increase in comparison to the long-channel device, and y_{min} is the position where this minimum potential occurs. y_{min} is determined by the balance between the fields at the source/channel and the channel/drain junctions as

$$y_{min} = -\frac{V_{ds}}{E_{Source} + E_{Drain}} \tag{4}$$

The electric fields E_{Source} and E_{Drain} at source and drain junctions, respectively, are determined by the impurity profiles at these junctions and V_{ds}. The potential minimum ϕ_{min} for the long-channel transistor is calculated by solving the Poisson equation. For the long-channel transistor this value is practically independent of the drain voltage (V_{ds}). However, for a short-channel case the ϕ_{min} value is influenced strongly by V_{ds} additionally, due to the overlap between the potential distribution at source/channel and channel/drain junctions.

The modeled $\Delta\phi_{min}$ has been implemented into HiSIM_MG as the lateral potential distribution in the form [33], [34]

$$V'_G = V_{gs} - V_{FB} + \Delta\phi_{min} \tag{5}$$

which is used to calculate the value of the surface potential f_S at $x = 0$ by solving the Poisson equation together with the Gauss Law

$$\phi_S(y) = V'_G + \frac{Q_{sem}(y)}{C_{ox}} \tag{6}$$

where Q_{sem} is the total charge induced in the semiconductor channel, which is a function of ϕ_S. $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate capacitance per unit of area for oxide permittivity ε_{ox}. This implicit function is solved iteratively using a 1D Newton method implemented in Verilog-A, an accurate initial analytical value is used to increase the speed of calculation with very low cost in terms of time. Once f_S is determined

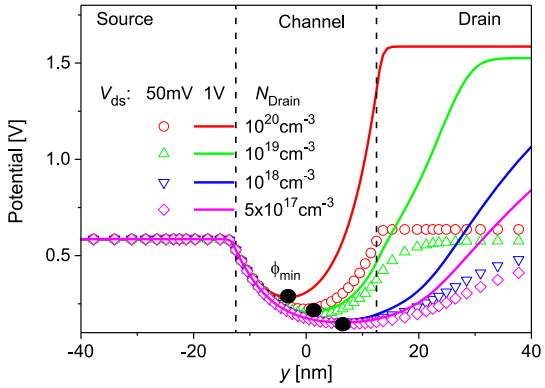

FIGURE 5. **Potential distribution along the channel in the substrate middle for different drain doping concentrations N_{Drain} at V_{ds} = 50mV and 1V by fixing $V_{gs} = 0$. The studied device parameters are $L = 25$nm, $t_S = 10$nm, $t_{ox} = 1.5$nm and $N_{sub} = 10^{15}$cm^{-3}.**

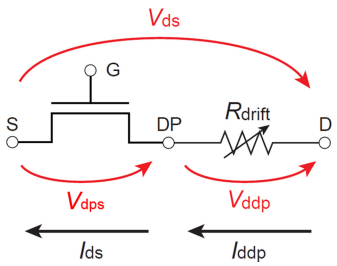

FIGURE 6. **MOSFET modeling including the bias-dependent drain-resistance effect.**

as a function of bias conditions, all device performances are written as a function of these potential values. Since the potential distribution is known, the drain current can be written by considering both the diffusion and the drift component. Particularly, in the subthreshold regime the diffusion contribution dominates the device characteristics.

B. INCLUSION OF RESISTANCE EFFECT

We have further extended the SCE-model to include the resistance effect of the diffusion regions, which is needed for measured-data reproduction of fabricated devices. The potential distributions from 2D device simulation are depicted in Fig. 5 for different drain-side doping concentrations, i.e., different drain-diffusion resistances and for two different V_{ds} values. It can be seen that the potential distribution extends deep into the drain region, when N_{Drain} reduces. According to the potential-distribution extension into the drain region, a reduction of the minimum potential value f_{min}, which is the main origin of the SC effects, is observed. This means a suppression of the SC effects [29] is achieved.

Modeling of the potential-distribution extension into the drain is done by using the HiSIM_HV modeling concept [35], as schematically illustrated in Fig. 6. Due to the resistive drain region, the major potential drop for the potential applied between source and drain occurs within the drain diffusion region. This feature of the potential distribution is modeled by introducing the internal node DP obtained by an iterative solution. The position of DP is where the gate control is diminished and the field induced within the resistive drain-side diffusion region drives the current flow. The difference of potential between the drain terminal with applied voltage V_{ds} and the node DP is the potential drop along the resistance R_{drift}. Thus model parameters of the diffusion region are mostly related to the impurity concentration in this region, and the potential-distribution feature is strongly influenced by the impurity-concentration difference between the channel and the diffusion region.

Eq. (6) is solved within the framework of the HiSIM_HV modeling. Namely, the node-DP potential is determined so that the intrinsic current density determined by the conventional MOSFET function becomes equal to that flowing within the resistive diffusion region [35].

C. MODEL VERIFICATION

To verify the developed model, calculated *I-V* characteristics are compared to those of 2D-device simulation results [31]. Silicon and Silicon Dioxide are used as semiconductor and oxide materials. Fig. 7 compares the studied devices with $t_s = 10$nm for different L without the drain-diffusion-resistance effect. For the shortest channel length, a huge leakage current in subthreshold region is observed. This device with L=15nm, presents high degradation due to SC effects, which is never used for real applications. Non-smoothness is observed only for extreme cases, the limitation of the developed model is $L > 2t_S$, when the normal MOSFET control is maintained as the scaling rule determines. Fig. 8 shows the comparison using the same technology but with the diffusive drain resistance effect. It is seen that the SC effect is obviously reduced with reduced N_{Drain}, which is well reproduced with the developed model. Low drain doping concentration in the drain side can benefit the subthreshold region ensuring the turn-off of the transistor, however, the transistor will drive a lower current in the ON-state condition due to the potential drop within the low doped drain region. Influence of the drain resistance effect for SCE-suppression is discussed in the next section.

IV. DEVICE OPTIMIZATION

With use of the SCE-model including the diffusion-resistance effects, the device optimization for further suppressing the SC effect is investigated. For this purpose, we have fixed the device parameters to the values shown in Table 1 and only N_{Drain} is varied. Figs. 9 and 10 compare the device characteristics of a transistor with $t_s = 5$nm and $L = 10$nm for different bias conditions and two different drain doping concentrations, $N_{Drain} = 1 \times 10^{20}$ and 5×10^{19}cm^{-3}. The subthreshold characteristics are strongly improved with the t_s reduction in comparison to the $t_S = 10$nm case (see Fig. 7). However, the short-channel effect is still observable in the V_{ds} dependence of the subthreshold region. Reduction in drain doping clearly improves the immunity of the device to SC effects.

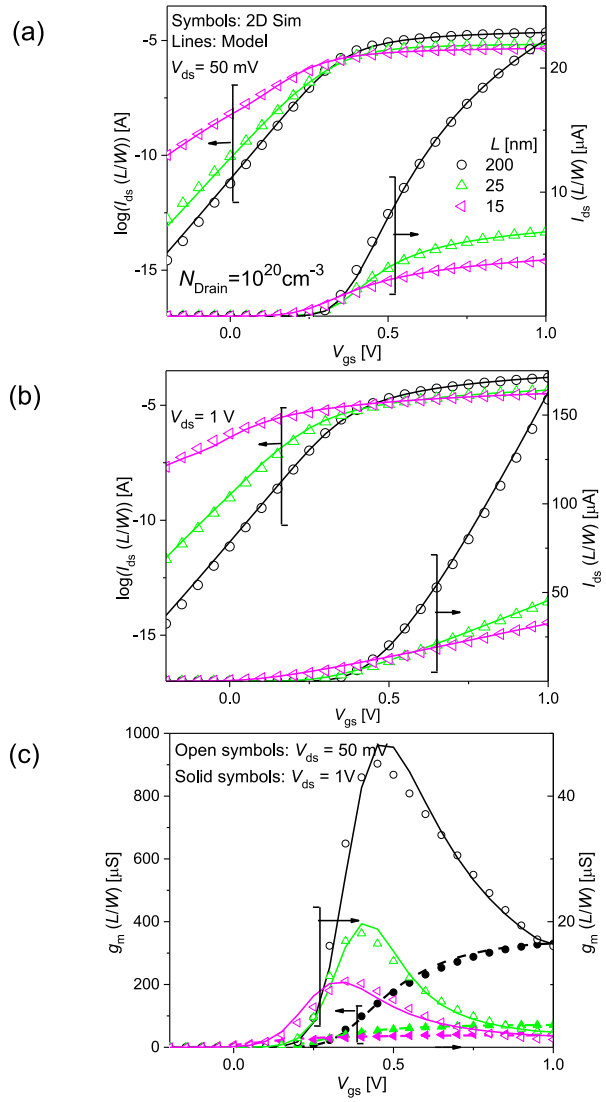

FIGURE 7. Transfer characteristics at (a) V_{ds} = 50mV and (b) V_{ds} = 1V for different channel length L. (c) Transconductances at V_{ds} = 50mV and 1V. The studied device parameters are t_S = 10nm, t_{ox} = 1.5nm and N_{sub} = 10^{15}cm^{-3}.

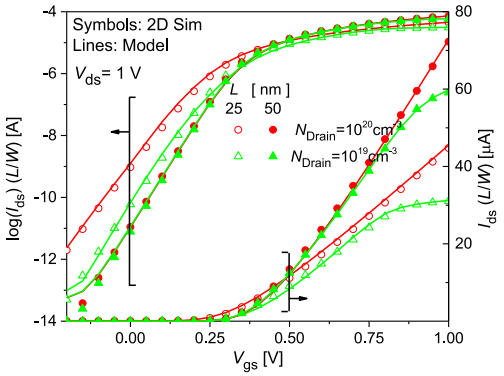

FIGURE 8. Comparison of *I-V* characteristics with 2D device simulation and developed model at V_{ds} = 1V for different drain doping concentrations and channel lengths. The studied device parameters are t_S = 10nm, t_{ox} = 1.5nm and N_{sub} = 10^{15}cm^{-3}.

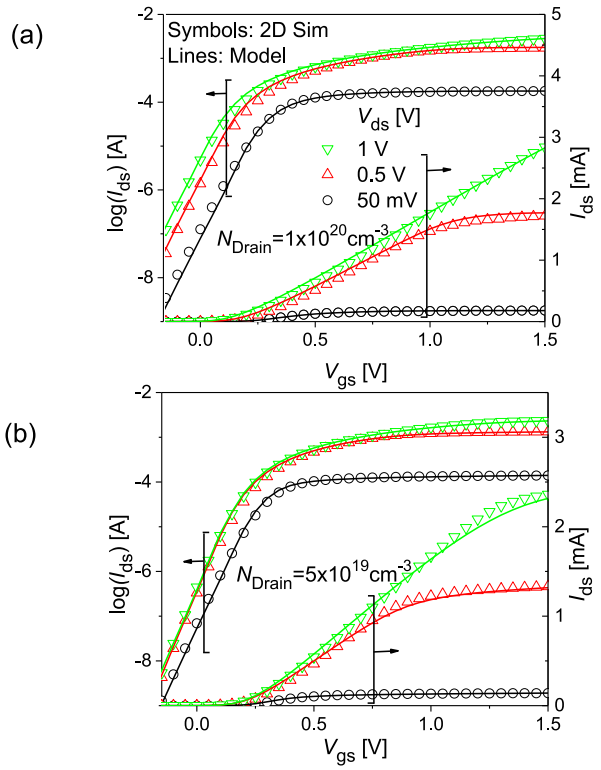

FIGURE 9. Comparison of model calculation results with those of 2D device simulation for transfer characteristics between devices with (a) N_{Drain} = 1 × 10^{20}cm^{-3} and (b) N_{Drain} = 5 × 10^{19}cm^{-3} at different V_{ds} cases. The studied device parameters are L = 10nm, t_S = 5nm, t_{ox} = 1.5nm and N_{sub} = 10^{15}cm^{-3}.

Fig. 11 shows the output characteristics and conductance of the same devices, where clear resistance effect is detected, namely the quasi-saturation effect is already observed for the $N_{\rm Drain} = 5 \times 10^{19}{\rm cm}^{-3}$ case. A Gummel Symmetry Test is performed to both devices when a set of symmetrical ($N_{\rm Drain} = N_{\rm Source}$) and asymmetrical ($N_{\rm Drain} < N_{\rm Source}$) device parameters are used. Fig. 12 shows the results, the model presents smoothness around the $V_{\rm ds} = 0$ and symmetry for a symmetrical device. On the case of the asymmetrical device, the test helps to show the continuity around the origin and asymmetry is expected due to the asymmetry of the device.

Fig. 13 compares the threshold-voltage shift $\Delta V_{\rm th}$ of the studied transistors in comparison to the long-channel $V_{\rm th}$ as a function of $V_{\rm ds}$, which gives a measure for the SC effects.

The threshold voltage is determined by the GLME method, which provides more reliable $V_{\rm th}$ values than the constant current method [36]. Since the $L/t_{\rm s}$ ratio for the $L = 10$nm case is smaller than that for the $L = 25$nm case, the $\Delta V_{\rm th}$ difference from small to large $V_{\rm ds}$ becomes larger in spite of the $t_{\rm s}$ reduction.The result with a reduced impurity concentration of the drain diffusion region $N_{\rm Drain}$ from 1×10^{20} cm^{-3} to 5×10^{19} cm^{-3} for the $L = 10$nm case is also depicted in Fig. 13, showing an obvious reduction of $V_{\rm ds}$ dependence,

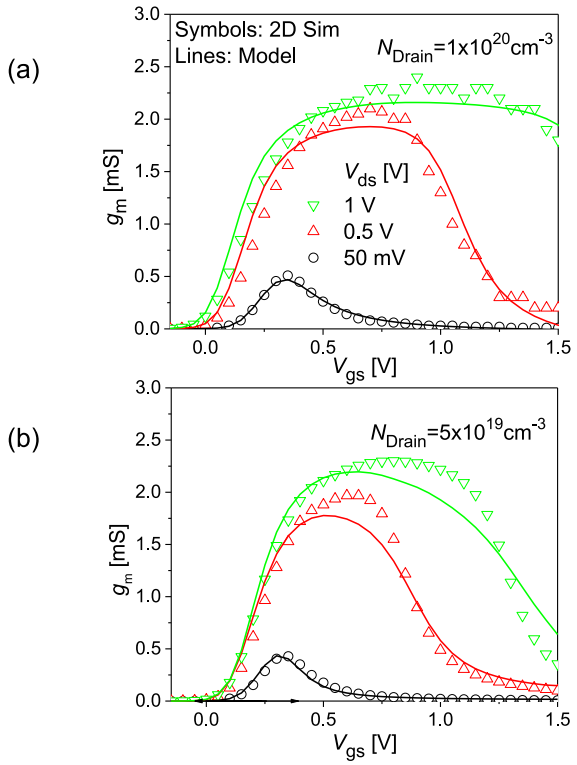

FIGURE 10. **Comparison of model calculation results with those of 2D device simulation for transconductance characteristics between devices with (a) $N_{Drain} = 1 \times 10^{20}$cm^{-3} and (b) $N_{Drain} = 5 \times 10^{19}$cm^{-3} at different V_{ds} cases. The studied device parameters are $L = 10$nm, $t_S = 5$nm, $t_{ox} = 1.5$nm and $N_{sub} = 10^{15}$cm^{-3}.**

i.e., the SC effect. The reason is attributed to the fact that the potential increase due to the increased V_{ds} is absorbed within the drain diffusion region as can be seen in Fig. 5, so that the potential minimum is decreased accordingly.

In order to observe the differences between the studied devices, model and simulation results of important parameters are compared in Table 3. High improvements in *SS* and *DIBL* are major achievements.

As the drain voltage increases, the potential drop occurs mostly in the resistive drain diffusion region, suppressing the lateral electric field increase in the channel region, and as a consequence the better V_{th} characteristics for high V_{ds} is achieved.

A specific attention has to be paid to the drain doping region, since a high resistive region affects negatively the ON state performance. The OFF/ON state current I_{OFF}/I_{ON} is presented in Table 3 as well. A ten times reduction in the OFF current is achieved, which reduces the leakage power consumption of the transistor. On the other hand, I_{ON} shows a very small difference between two devices, which results in no big penalties in the ON state by the slight reduction of N_{Drain}. The effective drain current I_{eff} is also compared. $g_{m,max}$ used for analog design presents similar values for the two presented cases.

TABLE 3. **Benchmarking for optimized/non-optimized device.**

Symbol	Quantity	Device I: Non-optimized L=10nm $N_{Drain}=10^{20}$ cm^{-3} [Sim/Model]	Device II: Optimized L=10nm $N_{Drain}=5\times10^{19}$ cm^{-3} [Sim / Model]
SS	Subthreshold slope [mV/dec]	93 / 95	83.7 / 86.5
DIBL	Drain Induced Barrier Lowering [mV· V^{-1}]	144.36 / 177.26	53.7 / 55.1
V_{th}	Threshold Voltage [V]	0.234 / 0.22	0.23 / 0.212
I_{OFF}	Off-current [μA] $I_{ds}(V_{gs}=0,V_{ds}=1V)$	4.78 / 5.3	0.446 / 0.290
I_{ON}	On-current [mA] $I_{ds}(V_{gs}=1V,V_{ds}=1V)$	1.76 / 1.78	1.67 / 1.63
I_{eff}	Effective current [mA]	1.05 / 1.11	0.886 / 0.895
$g_{m,max}$	Maximum transconductance at V_{ds}=1V [mS]	2.1 / 1.93	1.96 / 1.77
g_{ds}	Conductance at $V_{gs}=V_{ds}$=1V [mS]	0.798 / 0.66	1.62 / 1.54

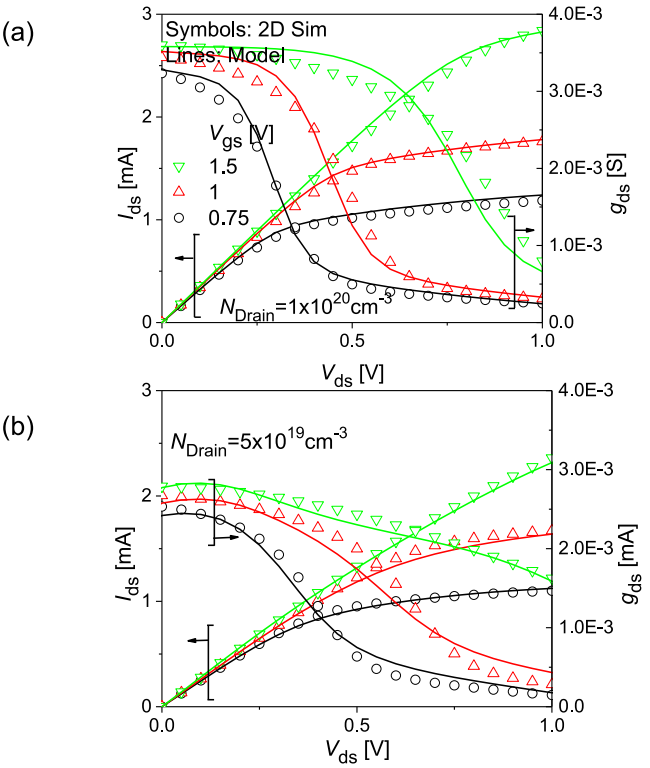

FIGURE 11. **Comparison of model calculation results with those of 2D device simulation for output characteristics between devices with (a) $N_{Drain} = 1 \times 10^{20}$cm^{-3} and (b) $N_{Drain} = 5 \times 10^{19}$cm^{-3} at different V_{ds} cases. The studied device parameters are $L = 10$nm, $t_S = 5$nm, $t_{ox} = 1.5$nm and $N_{sub} = 10^{15}$cm^{-3}.**

It is known that the SC effects cause the device-reliability reduction. Therefore, a lot of effort has been paid to reduce the SC effects [37], [38]. Since the drain resistance increase causes a degradation in device performances, the trade-off between the SCE reduction and the device-performance reduction must be investigated. Fig. 14 demonstrates the

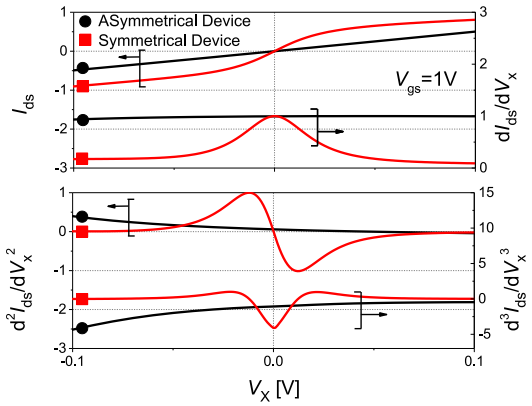

FIGURE 12. Normalized Gummel symmetry test for the drain current of the studied symmetrical ($N_{Drain} = N_{Source}$) and the asymmetrical ($N_{Drain} < N_{Source}$) device structures as a function of the voltage difference V_X = (Drain node voltage – Source node voltage)/2.

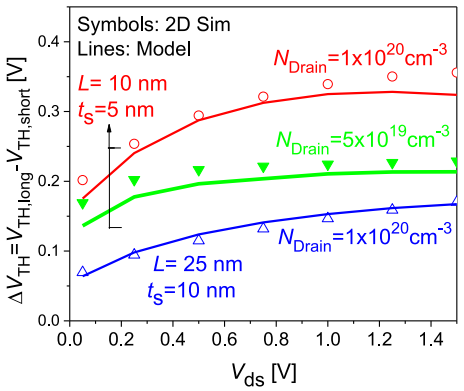

FIGURE 13. Threshold-voltage shift ΔV_{th} as a function of V_{ds} for three different transistors, demonstrating the SCE-reduction with reduced N_{Drain}. The studied device parameters are t_{ox} = 1.5nm and $N_{sub} = 10^{15}$cm^{-3}.

conduction loss of the two devices compared in Fig. 13 as a function of N_{Drain}. The circuit used for the simulation is depicted in Fig. 14b. The conduction loss is calculated by multiplying the current flowing under the on condition and the internal drain voltage as

$$Power = V_{\mathrm{ds}} \cdot I_{\mathrm{ds}} = V_{\mathrm{out}} \cdot I_{\mathrm{out}} \tag{7}$$

As can be expected the power loss decreases as N_{Drain} increases. However, it is also seen that the reduction characteristic saturates as N_{Drain} approaches $N_{\mathrm{Drain}} = 1 \times 10^{20}\mathrm{cm}^{-3}$. It is known that the value of $1\times10^{20}\mathrm{cm}^{-3}$ is already conductive and no potential drop occurs. Fig. 14 confirms that $N_{\mathrm{Drain}} = 5 \times 10^{19}\mathrm{cm}^{-3}$ causes a small power-loss increase.

V. DISCUSSION

We demonstrated that the developed model can be well applied for device optimization to realize high circuit performance. Here the model accuracy is a key to achieve reliable results, which are dependent on an accurate potential distribution along the channel. However, the impurity profile

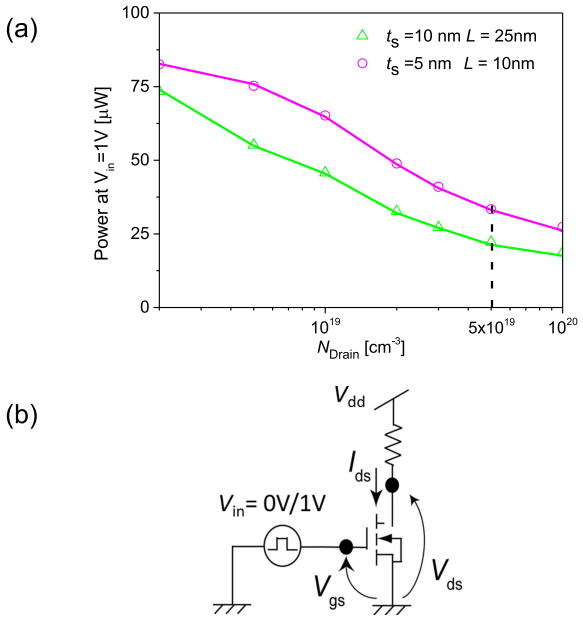

FIGURE 14. (a) Calculated power loss under the ON condition of a single N-MOS inverter with V_{in} = 1V as a function of N_{Drain}. V_{in} is the input voltage and V_{DD} is the power-supply voltage. (b) Circuit used for the power loss calculation. The studied device parameters are t_{ox} = 1.5nm and $N_{sub} = 10^{15}$cm^{-3}.

at the diffusion-region/channel junction must be known for this purpose, which is generally a very hard task and the same problematic situation as encountered for 2D device simulation.

In order to enable the modeling of the potential distribution, the magnitude of the fields E_{Source} and E_{Drain} at source/channel and channel/drain junctions are required (see Table 2), which are determined by the impurity profiles at junctions. These data for junction fields and impurity profiles then determine the potential-distribution modeling by a cubic function with model parameters A_0, B_0, and C_0. An advantage of such an analytical description for compact modeling in comparison to 2D-numerical device simulation is that measured SC effects, such as those shown in Fig. 13, allows to know the balance between the fields E_{Source} and E_{Drain}. This becomes possible, because the 2D impurity profile is reduced to just 1 dimension along the channel direction, where the device characteristic is mainly determined. In particular, the middle of the substrate is the most important position for determination of the device characteristics under the subthreshold condition.

The extension of the developed compact SCE-model for general MOSFETs can be done in a similar way by determining the position and path where the major current flow occurs, which, e.g., can be approximated by the diffusion region junction depth in case of the bulk MOSFET. For the DG-MOSFET with independent control by the two gate contacts, the position can be approximated by the ratio of the fields induced at the two independent gates. The proposed model approach is based on device-physics considering SC

effects for the subthreshold region and several effects above threshold, such as mobility degradation due to vertical and lateral electric fields, velocity saturation and also resistance effect. Performance of experimental devices is basically controlled by such effects.

VI. CONCLUSION

A new and complete compact model for short-channel effects is introduced and can be applied for device and circuit optimization of any technology node. The core improvements come from the developed potential-based modeling of the subthreshold region, which is verified with several structural and device variations. The reported compact SCE-model is suitable for multi-gate MOS devices. With the practical application of the proposed SCE-model it is verified that a slightly-resistive drain diffusion region can lead to a substantial suppression of SCEs without significantly sacrificing circuit and device performances.

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