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A T-Shaped SOI Tunneling Field-Effect Transistor With Novel Operation Modes

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ABSTRACT We present a novel T-shaped tunneling field-effect transistor (TFET) on Si-on-insulator (SOI). The asymmetric source-drain structure can effectively suppress the ambipolar switching. The on-current (I_{on})/off-current (I_{off}) ratio reaches very high value of $\sim 10^8$ at $V_{ds} = -0.5$ V with a smaller tunneling junction width at the drain. The innovative T-shape design allows integration of both TFET and metal-oxide semiconductor field-effect transistors (MOSFET) operation modes in one structure. Both TFET and MOSFET operation modes are experimentally demonstrated in this device structure, which provide the implementation of the selector function with the single device.

INDEX TERMS TFET, SOI, ambipolar, low power.

I. INTRODUCTION

Power consumption is becoming one of the major challenges as the scaling of traditional MOSFETs to adapt the rapid development of semiconductor industry [1]. Tunneling field-effect transistors (TFETs), due to the band to band tunneling (BTBT) carrier drift mechanism, have intrinsic advantages over standard MOSFETs in low power application by breaking through the limit of sub-threshold swing (SS) = 60 mV/dec at 300 K [2], [3]. However, application of TFETs is still limited by some challenges such as low on-current (I_{on}) [4]–[8], SS degradation caused by trap assisted tunneling (TAT) [9], [10], and ambipolar switching behavior resulted from the PIN structure. The low I_{on} TFET could be used in artificial organ especially as the replacement surgery makes great progress [11]–[15]. The ambipolar behavior in larger V_{ds} bias makes TFETs difficult for logic applications, causing the TFET circuit design more complicated than CMOS [16]–[18].

One intuitive method to suppress ambipolar behavior is to use a lightly doped drain. However, previous investigations didn't reveal expected results, especially for the ultrathin SOI and nanowire structure devices [19]–[21]. Another reported method is to use different materials for the source and drain. This is achieved by using a relatively narrow bandgap material at the source region and a wide bandgap material at the drain region [22]–[24]. Although this method can effectively suppress the ambipolar conduction effect, using of different materials will greatly increase the complexity of the fabrication process.

In order to reduce the off-state current and obtain a high-performance TFET device, we present a T-shaped SOI TFET with different widths of tunneling junction of source and drain. The preparation process was described in detail and the electrical characteristics of the device were measured and analyzed. In addition, the device of this special structure can also work in MOSFET operation mode at appropriate biases and the electrical results in this mode were also characterized. Thus, in this work we present our novel switch based device on this special structure that can work in the double operation mode.

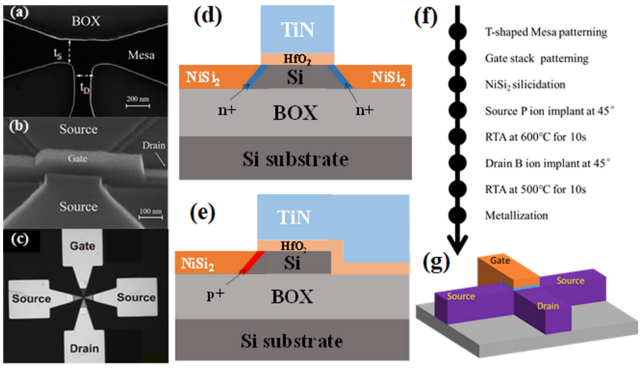

FIGURE 1. **SEM image of a T-shaped mesa (a), SEM image after gate formation (b) and Microscope image of the fabricated TFET structure (c). Cross-section views along the direction from source to source (d) and drain to gate (e). (f) Process flow of the device fabrication. (g) Schematic diagram of the T-shaped TFETs with unequal widths between source and drain.**

II. FABRICATION AND DEVICE STRUCTURE

The T-shaped transistor in which tunneling junction was formed by an ion implantation into $NiSi_2$ silicide was fabricated on SOI substrate. Fig. 1(f) shows the main process steps of the fabrication, including mesa patterning, gate stack patterning, $NiSi_2$ silicidation, ion implant, rapid thermal annealing (RTA) and metallization. The original SOI substrate has a top p-type lightly-doped silicon of 12 nm and a 145 nm-thick buried oxide (BOX) layer. E-beam lithography was used to pattern the T-mesa. Scanning electron microscope (SEM) image of a T-shaped mesa is shown in Fig. 1 (a). After RCA standard cleaning, a 3 nm-thick high-κ gate dielectric HfO_2 film was deposited by atomic layer deposition (ALD). Then a TiN film of 60 nm was deposited by atomic vapor deposition (AVD) method. After the gate formation as shown in the Fig. 1(b), a 3 nm-thick Ni film was deposited on the top Si surface by sputtering and followed by rapid thermal annealing at 700 °C for 30 seconds to form self-aligned $NiSi_2$ at source and drain region. Then phosphorus and boron ions were implanted under a tilt angle of 45 ° or 135 ° as shown in Fig. 1(d) and (e). The dopants were activated by using a 10 seconds RTP at 600 °C for phosphorus and at 500 °C for boron, respectively. During this process dopant segregated at the $NiSi_2$/Si channel interface to form the tunnel junction. Finally, the gate, source and drain contacts were formed with Pt/Cr (150 nm/5 nm) by lift-off process. The final device structure was shown in Fig. 1(c).

As showed in Fig. 1(g), unlike normal field-effect transistors, the mesa fabricated here is a T shape. The gate stack covers the intersection of the "T" to form the four-terminal devices. The two ends of the horizontal line of the "T" were defined as the sources and the bottom along the vertical line represents the drain for the TFET. For p-type TFET device, the source is n+ doped and the drain is p+ doped. The widths of the mesa where implanted by phosphorus and boron were defined as t_S and t_D, as shown in Fig. 1(a). Therefore, in this T-shaped structure, the width of the source/channel tunneling junction is $2t_S$ because there are two source regions, while the width of drain/channel tunneling junction is t_D. In this work, t_S is 200 nm whereas t_D is 100 nm/200 nm, respectively. Fig. 1(d) and Fig. 1(e) show the cross-section views along the direction from source to source and drain to gate.

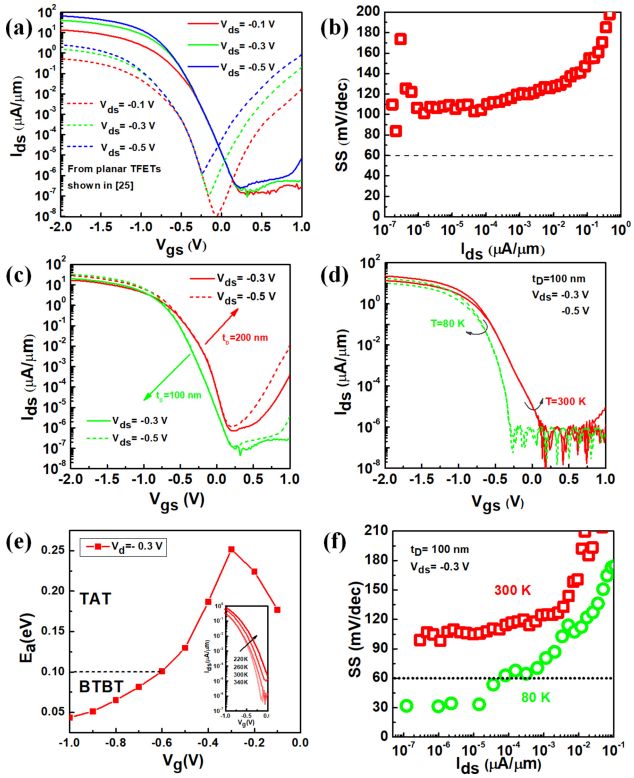

FIGURE 2. **Measured transfer characteristics (a) and SS-I_{ds} (b) of a T-shaped TFET. (c) Comparison of the transfer characteristics of T-shaped TFETs with different t_D. (d) Measured transfer characteristics of the device at 80 K and 300 K. (e) Extracted E_a as function of the gate voltages at $V_{ds} = -0.3$ V . (f) The SS-I_{ds} curves at 80 K and 300 K.**

III. RESULTS AND DISCUSSION

For TFET measurements, the both source contacts were grounded ($V_s = 0$ V), while the drain is biased with V_d. The solid lines in Fig. 2(a) shows the measured transfer characteristic of a T-shaped p-TFET with $t_S = 200$ nm and $t_D = 100$ nm. Compared with the transfer characteristic result from the planar TFET with symmetric source and drain shown in the dashed lines in Fig. 2(a) from [25], the device here exhibits good switching performance as the ambipolar turn-on current is significantly suppressed at $V_{gs} > 0$ V. Furthermore, with $|V_{ds}|$ increasing, the I_{off} still keeps at very low level. The I_{on}/I_{off} ratio remains very high with the largest I_{on}/I_{off} ratio as high as 10^8 at $V_{ds} = -0.5$ V. Due to the T-shaped structure, the width of the source/channel tunneling junction in our device is four times of the drain/channel tunneling junction. Then the n-type current was significantly suppressed in p-TFET at

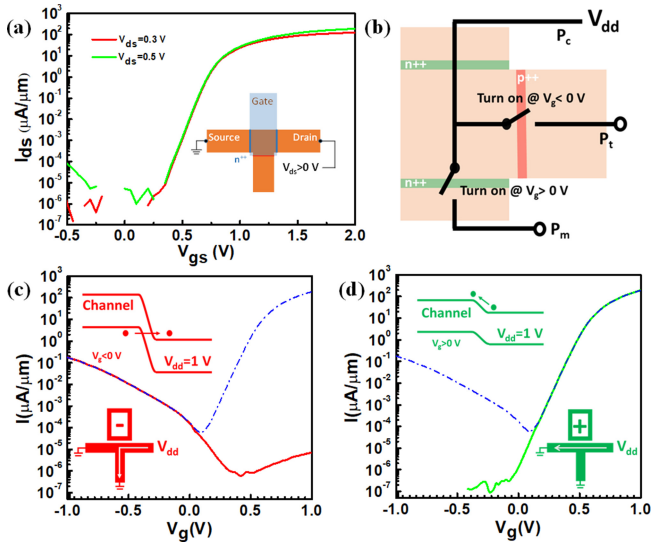

FIGURE 3. **(a)Transfer characteristic curves in MOSFET operating mode. (b) Schematic diagram of the T-shaped switch. V_g dependence of currents at P_t (c) and P_m (d).**

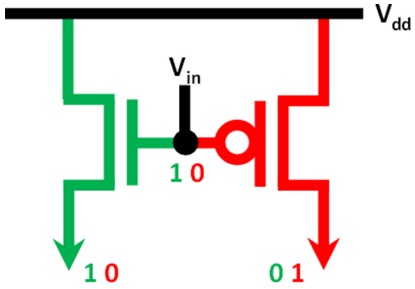

FIGURE 4. **Equivalent circuit of this single device works as a selector.**

$V_{gs} > 0$ V. Therefore, the T-shaped transistor basically avoid the ambipolar conduction.

The SS-I_{ds} was extracted from the transfer characteristic curve and shown in Fig. 2(b). The minimum sub-threshold swing (SS_{min}) is 95 mV/dec, while the average sub-threshold swing (SS_{avg}) is about 105 mV/dec at I_{ds} ranging from 10^{-7} to 10^{-4} μA/μm. The result also exhibits typical TFET device characteristics that SS increase with increasing I_{ds}. The larger SS value should be ascribed to the TAT process caused by the defects and traps in the device [9], [10].

Fig. 2(c) shows a comparison of the transfer characteristics of T-shaped TFET devices with various widths of t_D. Here, the currents were normalized with $2t_S$. The red lines represent the transfer characteristics for $t_D = 100$ nm, while the green lines represent the curves for $t_D = 200$ nm. In our device structure, when $t_S = 200$ nm and $t_D = 200$ nm, the ratio of source/channel tunneling junction width to drain/channel tunneling junction width is 2:1. While t_S is 200 nm and decreasing t_D to 100 nm the ratio is 4:1. A narrower drain tunneling junction decreases the tunneling currents at the drain side, thereby suppressing the ambipolar effect of the device. As can be seen from the figure, the device still exhibits a pronounced ambipolar turn-on current at n-type branch for $t_D = 200$ nm. The n-type I_{ds} at $V_{gs} > 0$ V increases with $|V_{ds}|$. However, for the device with $t_D = 100$ nm, the ambipolar n-type I_{ds} was significantly reduced by several orders of magnitude rather than by a factor of 2. This is because the tunneling currents distribution at the channel/drain tunneling junction is uneven. As shown in Fig. 1(c), the gate of this nanoscale device works like a Tri-gate to control the channel instead of a planner gate [26]. Therefore, the tunneling currents at the edge of channel/drain tunneling junction contributes more to the I_{off}. When reducing the width, the distance from the source to drain increases and the electric field strength from the source to the drain in the channel will drop more at the corner, which lead to futher reduction of I_{off}.

The transfer characteristics of the T-shaped TFET device were also measured at low temperature. The result was shown in Fig. 2(d). It can be clearly seen that the device exhibits a steeper SS at low temperature due to the suppressed TAT which is associated with a thermal emission process. In order to confirm that the TAT is the origin of SS degradation, the activation E_a was extracted from the inset of the Fig. 2 (e) which shows the subthreshold region of the device at temperature ranging from 220K to 340K and was plotted versus V_g as shown in the Fig. 2 (e). The E_a values reflect the contributions of TAT, Shockley-Read-Hall (SRH) recombination and BTBT [27]. The peak of E_a is 0.25 eV, which is less than half of the Si band-gap, indicating that the TAT current is the main contribution when V_g is small. E_a is lower than 0.1 eV at $V_g < -0.6$ V, indicating that the current is dominated by BTBT at on-state [28]. In addition, the transition of E_a from the TAT dominant area to the BTBT dominant area is relatively gentle, indicating that the TAT in the device has a greater impact when the device worked in the subthreshold region. And the Fig. 2 (f) reveals that the SS reached 30 mV/dec at 80K, consistent with the report in [25]. All the results indicate that the larger SS in room temperature should be attributed to defects in the preparation process rather than the T-shaped structure itself. The I_{on} at 80 K is lower than that at 300 K. This is because, at low temperature, the energy bandgap (E_g) increases slightly, resulting in a reduction of the tunneling probability. The result also proves that the on-state current of the T-shaped TFETs is mainly contributed by the BTBT process.

This special T-shaped four-terminal device can be operated not only in TFET mode, but also in MOSFET mode. In the T-shaped structure, one side of the "T-horizontal" is grounded as the source and the other side is applied by V_{ds} as the drain. As the both sides are heavily n+ doped, the device can be also operated as an n-type MOSFETs. Fig. 3(a) shows the transfer characteristic of this device. Thus, this device can be used as a combination of a MOSFET and a TFET.

Obviously, the device works in MOSFET operation mode with a positive gate voltage, while it works in TFET operation mode when the gate voltage turns negative. According

to this feature, the device can be used as a switch which has two paths to decide whether to turn on or off. As shown in Fig. 3 (b), one of the "T-horizontal" was bias by V_{dd} and the other two terminals are at lower potentials. And these three ports are named separately by P_c, P_t and P_m. When the gate voltages is either positive or negative, the N-type heavily doped region near P_c can be turned on. The barriers between the channel and the N-type heavily doped region near P_m and P-type heavily doped region near P_t are like two parallel resistors whose resistances are affected by the gate voltage.

The blue dash lines in Fig. 3(c) and Fig. 3(d) show the total currents measured at P_c, while the red solid line in Fig. 3(c) and the green solid line in Fig. 3(c) show the currents at P_t and P_m, respectively. This result shows excellent switching characteristics. When $V_g < 0$ V, the currents at P_c is almost entirely contributed by the current at P_t. And when $V_g >$ 0.2 V, basically all currents flow from P_c to P_m.

Fig. 4 shows the equivalent circuit model of the device. A common-gate P-type transistor and N-type transistor form a selector that implements the functionality with a single device rather than by two devices. In addition, the currents at P_c have two sub-threshold regions on both sides of 0.2 V. When the gate voltage changes slightly, not only the magnitude but also the direction of the currents will change accordingly. Therefore, this structure has the potential to be applied in voltage sensitivity sensors. While the large mismatch of on-state currents in both modes may cause some problems. It limits the direct application for digital logic circuits, because the performance of the device does not allow the series connection of TFETs and MOSFETs. Heterogeneous integration allows devices with various materials to be integrated on one chip, and the device has potential to meet the connection among different functional components.

IV. CONCLUSION

We have fabricated and characterized a T-shaped TFET device based on SOI technology. In the T-shaped mesa structure, asymmetric tunneling junctions at the source and drain were formed to suppress the intrinsic ambipolar switching of the TFET device. The experimental results show that the I_{on}/I_{off} ratio reaches 10^8 at $V_{ds} = -0.5$ V. Low temperature results explain the high SS and prove that the I_{on} of the T-shaped TFET are mainly resulted from the BTBT. Both TFET and MOSFET have been realized with the proposed T-shaped device structure. The equivalent circuit model shows that our device is qualified for the two work mode including TFET and MOSFET, which can be used as a selector. In addition, the two sub-threshold workspaces also make this device has potential for the application in voltage sensitivity sensors.

REFERENCES

[1] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014. doi: 10.1109/JEDS.2014.2326622.

[2] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010. doi: 10.1109/JPROC.2010.2070470.

[3] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011. doi: 10.1038/nature10679.

[4] K. K. Bhuwalka, M. Born, M. Schindler, T. Sulima, M. Schmidt, and I. Eisele, "P-channel tunnel field-effect transistors down to sub-50 nm channel lengths," *Jpn. J. Appl. Phys*, vol. 45, no. 4B, pp. 3106–3109, Apr. 2006. doi: 10.1143/JJAP.45.3106.

[5] K. K. Bhuwalka, J. Schulze, and I. Eisele, "A simulation approach to optimize the electrical parameters of a vertical tunnel FET," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1541–1547, Aug. 2005. doi: 10.1109/ted.2005.850618.

[6] M. Lee, J. Koo, E.-A. Chung, D.-Y. Jeong, Y.-S. Koo, and S. Kim, "Silicon nanowire-based tunneling field-effect transistors on flexible plastic substrates," *Nanotechnology*, vol. 20, no. 45, Oct. 2009, Art. no. 455201. doi: 10.1088/0957-4484/20/45/455201.

[7] H. G. Virani, R. B. R. Adari, and A. Kottantharayil, "Dual-*k* spacer device architecture for the improvement of performance of silicon n-channel tunnel FETs," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2410–2417, Oct. 2010. doi: 10.1109/TED.2010.2057195.

[8] M. Najmzadeh, K. Boucart, W. Riess, and A. M. Ionescu, "Asymmetrically strained all-silicon multi-gate *n*-Tunnel FETs," *Solid-State Electron.*, vol. 54, no. 9, pp. 935–941, Sep. 2010. doi: 10.1016/j.sse.2010.04.037.

[9] Q. Smets *et al.*, "Pulsed I-V on TFETs: Modeling and measurements," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1489–1497, Apr. 2017. doi: 10.1109/TED.2017.2670660.

[10] P. Singh, V. Asthana, R. Sithanandam, A. Bulusu, and S. D. Gupta, "Analytical modeling of sub-onset current of tunnel field effect transistor," in *Proc. 27th Int. Conf. VLSI Design 13th Int. Conf. Embedded Syst.*, Mumbai, India, 2014, pp. 411–414. doi: 10.1109/VLSID.2014.77.

[11] H. Chen, Z. Cao, S. Su, J. Liu, and Z. Wang, "Measurement System for attitude of anterior pelvic plane and implantation of prothesis in THR surgery," *IEEE Trans. Instrum. Meas.*, vol. 67, no. 8, pp. 1913–1921, Aug. 2018. doi: 10.1109/tim.2018.2809818.

[12] S. Su, Y. Zhou, Z. Wang, and H. Chen, "Monocular vision- and IMU-based system for prosthesis pose estimation during total hip replacement surgery," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 3, pp. 661–670, Jun. 2017. doi: 10.1109/TBCAS.2016.2643626.

[13] H. Tang, H. Chen, D. Yang, Y. Jiang, C. Zhang, and Y. Zhou, "Distinctions of introarticular force distribution between genesis-II posterior stabilized and cruciate retaining total knee arthroplasty: An intraoperative comparative study of 45 patients," *Clin. Biomech.*, vol. 42, pp. 1–8, Feb. 2017. doi: 10.1016/j.clinbiomech.2016.12.007.

[14] H. Chen, J. Gao, S. Su, X. Zhang, and Z. Wang, "A visual-aided wireless monitoring system design for total hip replacement surgery," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 2, pp. 227–236, Apr. 2015. doi: 10.1109/TBCAS.2015.2416253.

[15] Z. Cao, S. Su, Z. Wang, and H. Chen, "Live demonstration: A real-time measurement system for pose of anterior pelvic plane and implantation angles of prosthesis in THR surgeries," in *Proc. IEEE Biomed. Circuits Syst. Conf. (Biocas)*, Turin, Italy, 2017, p. 172.

[16] S. Richter *et al.*, "Tunnel-FET inverters for ultra-low power logic with supply voltage down to VDD = 0.2 V," in *Proc. Int. Conf. Ultimate Integr. Silicon (ULIS)*, Stockholm, Sweden, 2014, pp. 13–16.

[17] M. Lee, Y. Jeon, J.-C. Jung, S.-M. Koo, and S. Kim, "Multiple silicon nanowire complementary tunnel transistors for ultralow-power flexible logic applications," *Appl. Phys. Lett.*, vol. 100, no. 25, Jun. 2012, Art. no. 253506. doi: 10.1063/1.4729930.

[18] G. V. Luong *et al.*, "Experimental demonstration of strained Si nanowire GAA n-TFETs and inverter operation with complementary TFET logic at low supply voltages," *Solid-State Electron.*, vol. 115, pp. 152–159, Jan. 2016. doi: 10.1016/j.sse.2015.08.020.

[19] F. Settino, F. Crupi, S. Biswas, J. D. Holmes, and R. Duffy, "Modelling doping design in nanowire tunnel-FETs based on group-IV semiconductors," *Mater. Sci. Semicond. Process.*, vol. 62, pp. 201–204, May 2017. doi: 10.1016/j.mssp.2016.10.048.

[20] V. Vijayvargiya and S. Vishvakarma, "Effect of doping profile on tunneling field effect transistor performance," in *Proc. Spanish Conf. Electron Devices(CDE)*, Valladolid, Spain, 2013, pp. 195–197.

[21] S. Mantl *et al.*, "Si based tunnel field effect transistors: Recent achievements," in *Proc. Int. Conf. Ultimate Integr. Silicon (ULIS)*, Coventry, U.K., 2013, pp. 15–20.
[22] M. Schmidt *et al.*, "Line and point tunneling in scaled Si/SiGe heterostructure TFETs," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 699–701, Jul. 2014. doi: 10.1109/LED.2014.2320273.
[23] C.-H. Shih and N. D. Chien, "Physical operation and device design of short-channel tunnel field-effect transistors with graded silicon-germanium heterojunctions," *J. Appl. Phys.*, vol. 113, no. 13, Apr. 2013, Art. no. 134507. doi: 10.1063/1.4795777.
[24] S. Blaeser *et al.*, "Novel SiGe/Si line tunneling TFET with high Ion at low Vdd and constant SS," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2015, pp. 608–611.
[25] C. Liu *et al.*, "Experimental *I*-*V*(*T*) and *C*-*V* analysis of Si planar p-TFETs on Ultrathin body," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 5036–5040, Dec. 2016. doi: 10.1109/TED.2016.2619740.
[26] T. Baldauf *et al.*, "Simulation and optimization of tri-gates in a 22 nm hybrid tri-gate/planar process," in *Proc. Ulis Ultimate Integr. Silicon*, Cork, Ireland, Apr. 2011, pp. 3–6. doi: 10.1109/ULIS.2011.5757974.
[27] A. Vandooren *et al.*, "Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction tunnel-FETs," *Solid-State Electron*, vol. 83, pp. 50–55, May 2013. doi: 10.1016/j.sse.2013.01.026.
[28] C. Liu *et al.*, "Experimental investigation of *C*-*V* characteristics of Si tunnel FETs," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 818–821, Jun. 2017.