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Numerical Analysis of the LDMOS With Side Triangular Field Plate

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ABSTRACT A Lateral Double-diffused Metal Oxide Semiconductor (LDMOS) with side triangular field plate (STFP) is proposed for improving the breakdown voltage (BV) and reducing the specific on-resistance ($R_{on,sp}$). The main feature of the novel LDMOS is the STFPs at both ends of the drift region, and they are fabricated into the dielectric pillars. With the introduction of the STFPs, the electric field peaks at the P-well/N-drift and N+/N-drift junctions are reduced effectively. The STFPs together with the dielectric pillars modulate the surface and vertical electric field distributions, which enhances the BV. Meanwhile, the doping concentration of the silicon pillars in the drift region is optimized and thus reduces the $R_{on,sp}$. The simulation results indicate that the BV of 379 V and the $R_{on,sp}$ of 37.3 m$\Omega\cdot$cm^2 are achieved by the STFP-LDMOS. The figure of merits (FOM) of the STFP-LDMOS is 2.7 times compared with the conventional LDMOS without STFPs. The STFP-LDMOS demonstrates a great trade-off between the $R_{on,sp}$ and BV.

INDEX TERMS Side triangular field plate, LDMOS, breakdown voltage, specific on-resistance.

I. INTRODUCTION

With the rapid development of the power integrated circuit, Lateral Double-diffused Metal Oxide Semiconductor (LDMOS) has been widely applied into various power devices owing to its advantages such as the high speed and the low parasitical effect [1]–[3]. The trade-off between the specific on-resistance ($R_{on,sp}$) and the breakdown voltage (BV) is one of the concerns for the design of LDMOS [4]–[5]. The high electric field peaks at the P-well/N-drift junction and N+/N-drift junction limit the improvement of the BV in the LDMOS. For this issue, the field plate technology is one of the effective junction termination techniques to improve the BV by reducing the electric field peaks at junctions. The related concepts such as the striped trench electrodes [6], the split gate [7], the trigate [8], and the trench field plate [9] have been proposed to modulate the electric field from the sides of the drift region. However, these structures focus on the voltage class lower than 200V because higher BV requires the wider sidewall dielectric region to contain the large size field plate, which leads to high $R_{on,sp}$ [6].

In this paper, the LDMOS with side triangular field plates (STFP-LDMOS) is presented and investigated. The side field plates are fabricated into the dielectric pillars to isolate from the silicon region. The electric field and doping concentration of the proposed STFP-LDMOS have been modulated by not only the side triangular field plates, but also the dielectric pillars [10]–[12]. Therefore, the BV and $R_{on,sp}$ have been significantly improved. The results are obtained from the three-dimensional semiconductor device simulator DAVINCI. The physical models such as Shockley-Read-Hall recombination model (CONSRH), Auger recombination model (AUGER),

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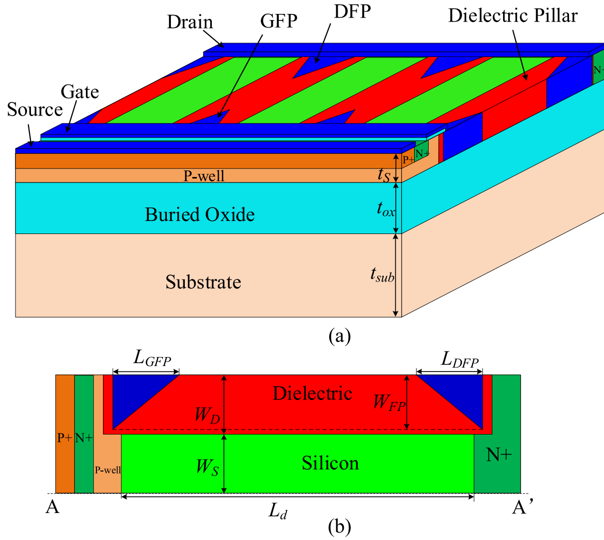

FIGURE 1. (a) The 3D structure of STFP-LDMOS, (b) top view of the basic unit for simulation.

carrier mobility model (FLDMOB) and impact ionization model (IMPACT.I) are used in the simulation.

II. DEVICE STRUCTURE AND MECHANISM

Fig. 1 shows the three-dimensional structure of the proposed STFP-LDMOS. To add the side triangular field plates into the drift region, dielectric pillars are introduced firstly, and thereby forming the composite drift region with silicon pillars and dielectric pillars. The side triangular field plates are fabricated into the dielectric pillars, and their depths are the same as the dielectric pillars and the top silicon layer. The field plates at the P-well/N-drift junction are connected to the gate electrode, named gate field plate (GFP). The field plates at the N-drift/N+ junction are connected to the drain electrode, named drain field plate (DFP). By employing the side triangular field plates, the surface electric field peaks at the ends of the drift region have been reduced. Meanwhile, the vertical electric field has been improved due to the DFP, avoiding the premature breakdown under the drain. Both result in the improvement of breakdown voltage. The doping concentration of the silicon pillars is also increased by the modulation of the STFPs and dielectric pillars, leading to the low $R_{on,sp}$. The thickness of the top silicon layer, the buried oxide layer, and the substrate layer are t_S, t_{ox}, and t_{sub}, respectively. Based on the symmetry of the structure, the basic unit is used to simplify the simulation, its top view is shown in Fig. 1(b). The width of the silicon pillar and the dielectric pillar are W_S and W_D. The length of the GFP and DFP are L_{GFP} and L_{DFP}, respectively. The widths of the GFP and DFP are the same and both are defined as W_{FP}. The L_d and N_d are the length and doping concentration of the drift region. The values of the device parameters used in this paper are presented in Table 1.

To explore the mechanism of the proposed STFP-LDMOS. Fig. 2 illustrates the equipotential contours of

TABLE 1. Device parameters used in the simulation.

Parameters	Value
Thickness of the top silicon layer, t_s (μm)	1
Thickness of buried oxide layer, t_{ox} (μm)	3
Thickness of substrate, t_{sub} (μm)	5
Width of the silicon pillar, W_S (μm)	1
Width of the dielectric pillar, W_D (μm)	1
Width of the field plate, W_{FP} (μm)	0.8
Length of the drift region, L_d (μm)	20
Length of the gate field plate GFP, L_{GFP} (μm)	Optimized
Length of the drain field plate DFP, L_{DFP} (μm)	Optimized

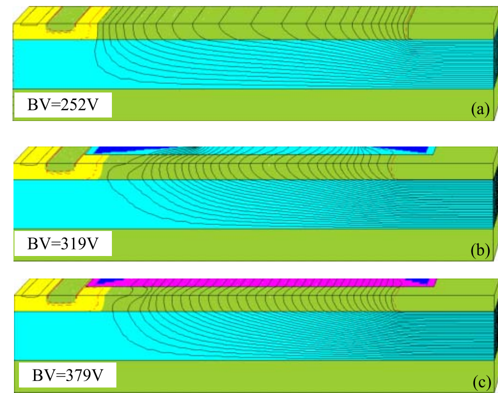

FIGURE 2. Equipotential contour plots at own optimal *BV* for (a) CONV-LDMOS, (b) STFP-OX-LDMOS, (c) STFP-HK-LDMOS.

the STFP-LDMOS and the conventional LDMOS without side triangular field plate (CONV-LDMOS). Since the field plate length also depends on the dielectric materials, the STFP-OX-LDMOS with oxide dielectric ($\varepsilon_D = 3.9$) and the STFP-HK-LDMOS with a high-k dielectric ($\varepsilon_D = 200$) are both given to make the comparison. The comparison is under the condition when the three LDMOSs obtain their own optimal *BV*. As shown in Fig. 2(a), the equipotential contours of the CONV-LDMOS device is mainly concentrated at both ends of the drift region, and the middle part is sparse. Compared with the CONV-LDMOS, the equipotential contours in the STFP-OX-LDMOS and STFP-HK-LDMOS are concentrated at both ends of two triangular trench field plate, and the middle part STFP-HK-LDMOS is more uniform. Therefore, the voltage sustaining characteristics of the LDMOS can be improved. Note that, the STFP-OX-LDMOS has the L_{GFP} of 6μm and L_{DFP} of 4μm, while the STFP-HK-LDMOS has the L_{GFP} of 2μm and L_{DFP} of 2μm. Because the dielectric material also modulates the equipotential contours [10], the length of the field plate needs to be optimized according to the dielectric material.

Fig. 3 shows the surface electric field distributions along AA' line for the CONV-LDMOS, STFP-OX-LDMOS, and STFP-HK-LDMOS. It can be seen from the figure that the electric field peak P1 at the P-well/N-drift junction is

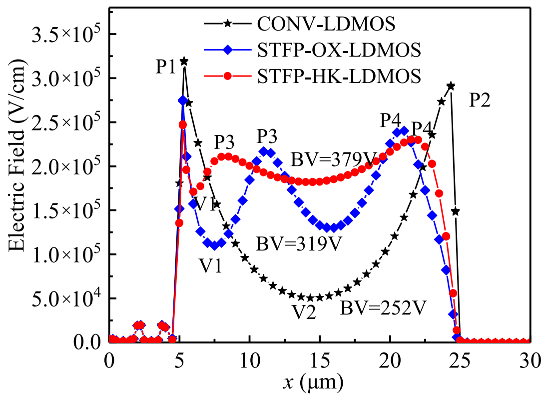

FIGURE 3. Surface electric field distributions at optimal *BV* for the different LDMOS.

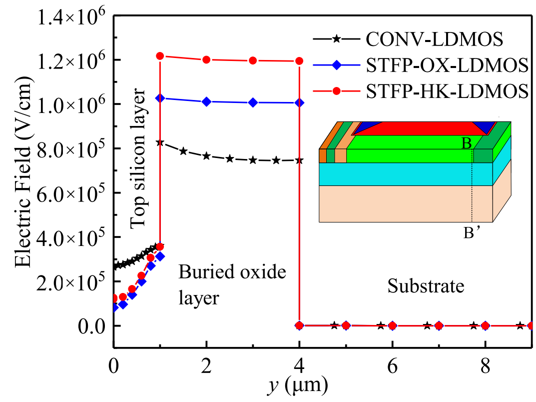

FIGURE 4. Vertical electric field distribution at the drain at optimal *BV* for the different LDMOS.

reduced by the GFP, the STFP-HK-LDMOS has the lowest P1 because of the high permittivity of the dielectric pillar. Meanwhile, the electric field peak P3 is formed at the edge of the GFP because of the accumulation of equipotential contours shown in Fig. 2. The electric field peak P2 at the N+/N-drift junction is almost eliminated due to the applied voltage on the DFP which makes the peak move to the edge of the DFP, marked as P4. On the other hand, the high-k dielectric improves the electric field valley V2 significantly. Therefore, the *BV* of 379V in STPF-HK-LDMOS is increased by 50% when comparing to the *BV* of 252V in CONV-LDMOS.

Fig. 4 shows the vertical electric fields at the drain end (along BB' line) under the optimal *BV* for the three LDMOSs. The electric field in the buried oxide layer is only 0.8×10^{6} V/cm for the CONV-LDMOS, while it is 1.06×10^{6} V/cm for the STFP-OX-LDMOS, and 1.26×10^{6} V/cm for the STFP-HK-LDMOS. Obviously, the vertical breakdown voltage has been improved by the STPFs.

Fig. 5 depicts the switching characteristic for the CONV-LDMOS, STFP-OX-LDMOS, and STFP-HK-LDMOS. The Vdd applied to the drain is 200V through the load resistor of 2×10^{6} Ω, the 10-V input pulse is applied to the gate through a resistor of 30 Ω. The rise time of the STFP-HK-LDMOS is about 0.4ns while the rise times of the CONV-LDMOS and STFP-OX-LDMOS are 0.5ns and 0.55ns. The fall time is about 6ns for the three LDMOSs. Therefore, the novel LDMOS maintains the excellent switching characteristic compared with that of the CONV-LDMOS.

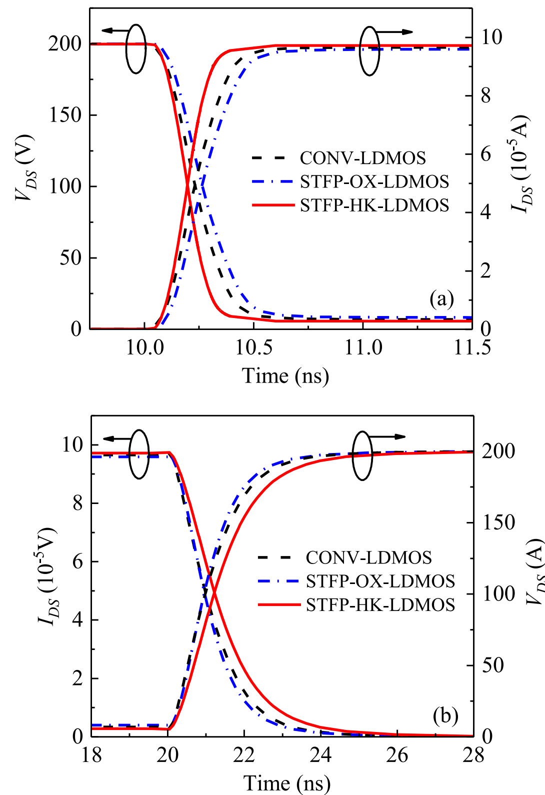

FIGURE 5. Switching characteristic for the different LDMOS. (a) Turn-on. (b) Turn-off.

III. RESULTS AND DISCUSSIONS

The STFP-LDMOS with different L_{GFP} and L_{DFP} are simulated to investigate the influence of the side triangular field plate on the characteristics of the proposed LDMOS. Fig. 6 shows the *BV* versus the N_d of the STFP-OX-LDMOS and STFP-HK-LDMOS with different L_{GFP} and L_{DFP}. It can be seen from the figure that the *BV* increases first and then reduces with the increasing of N_d. The maximum *BV* and the corresponding N_d are obtained. For the STFP-OX-LDMOS, the field plate can improve the maximum *BV* significantly when comparing the LDMOS without field plate and the CONV-LDMOS. The L_{GFP} has a large influence on the maximum *BV* as shown in Fig. 6(a), while the L_{DFP} has less influence on the maximum *BV* as shown in Fig. 6(b). The optimal *BV* can be obtained when $L_{GFP} = 6\mu$m and $L_{DFP} = 4\mu$m. For the STFP-HK-LDMOS, the maximum *BV* reaches 379V when $L_{GFP} = 2\mu$m and $L_{DFP} = 2\mu$m. As illustrated in Fig. 6(c) and (d), with the increasing of L_{GFP} and L_{DFP}, the maximum *BV* decreases

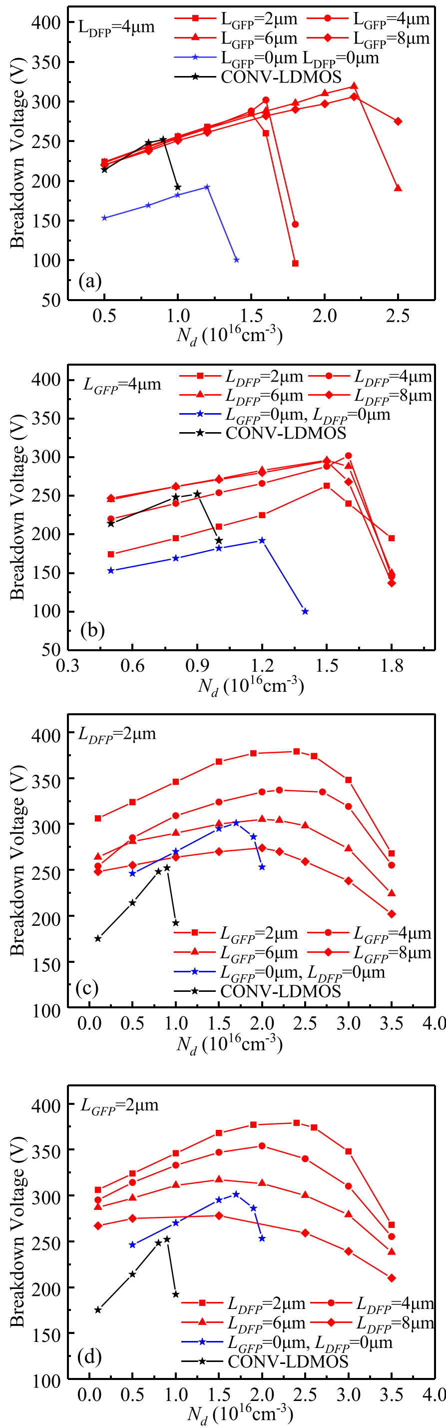

FIGURE 6. ***BV* versus N_d of the (a) STFP-OX-LDMOS with different L_{GFP}, (b) STFP-OX-LDMOS with different LDFP, (c) STFP-HK-LDMOS with different L_{GFP}, (d) STFP-HK-LDMOS with different L_{DFP}.**

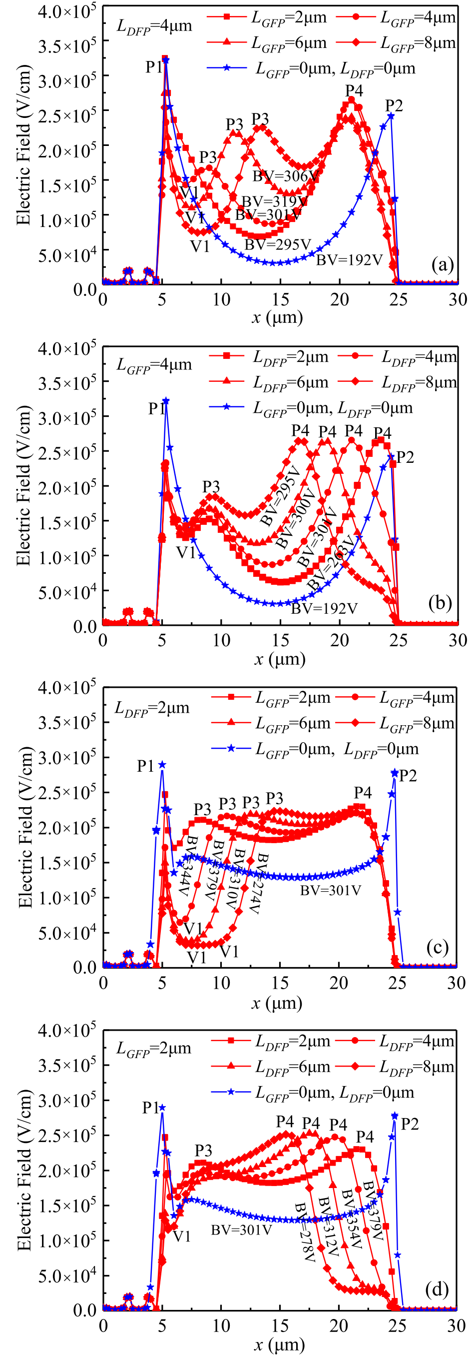

FIGURE 7. Surface electric field distributions for the (a) STFP-OX-LDMOS with different L_{GFP}, (b) STFP-OX-LDMOS with different L_{DFP}, (c) STFP-HK-LDMOS with different L_{GFP}, (d) STFP-HK-LDMOS with different L_{DFP}.

and even lower than that of the LDMOS without side trench field plates. The longer L_{GFP} or L_{DFP} makes the shorter effective length of the drift region, leading to the lower *BV*.

To reveal the reason of the maximum *BV* changes with the length of the field plates, Fig. 7 illustrates the electric field distribution for the STFP-OX-LDMOS and STFP-HK-LDMOS with different L_{GFP} and L_{DFP} when they reach their maximum *BV* shown in Fig. 6. As can be seen from the figure, the electric field peaks P1 and P2 at the junction of P-well/N-drift and N+/N-drift can be reduced by the STFPs. At the same time, new electric field peaks P3 and P4 are introduced at the GFP edge and DFP edge.

Therefore, the electric field distributions have been modulated and the breakdown voltage is changed. As shown in Fig. 7(a), the new electric field peak P3 produced by GFP increases and shifts to right with L_{GFP} increasing, which increases the BV. However, the electric field valley V1 reduces with the increasing of L_{GFP}, leading to decrease of BV. Therefore, the L_{GFP} needs to be optimized to obtain the optimal BV. The electric field peak P4 produced by DFP shifts to left with the same peak value when L_{DFP} increasing as shown in Fig. 7(b). The electric field at the left of P4 increases but the electric field at the right of P4 decreases, hence, the BV is almost the same. For the results of STFP-HK-LDMOS shown in Fig. 7(c) and (d), the STFPs can further improve the electric field although the high-k dielectric has modulation on the electric field. However, with the increasing of the L_{GFP} and L_{DFP}, the valley of the electric field became larger and the effective drift length to sustain the applied voltage became shorter, which results in the decreasing of BV.

Fig. 8 shows the on-state output characteristic curves of the STFP-OX-LDMOS and STFP-HK-LDMOS with different L_{GFP} and L_{DFP}. Obviously, the saturation current of the STFP-LDMOS is higher than the CONV-LDMOS, the STFP-HK-LDMOS has a very high saturation current because of the saturation voltage has been increased by the modulation effect of the high-k dielectric. The current in the linear region of the STFP-LDMOS is almost the same as that of the CONV-LDMOS, which means their on-resistance are nearly the same. The reason is that although the increased doping concentration of the STFP can reduce the on-resistance, but the reduced current path increases the on-resistance. With the modulation effect of high-k dielectric on the doping concentration, the specific on-resistance of the STFP-HK-LDMOS has been improved. The specific on-resistance is calculated by extracting the data from the deep linear region of the IV curves. The calculated $R_{on,sp}$ of the STFP-OX-LDMOS and STFP-HK-LDMOS is 40.2 m$\Omega\cdot$cm^2 and 37.3 m$\Omega\cdot$cm^2, respectively. Compared to 44.3 m$\Omega\cdot$cm^2 of the CONV-LDMOS, the $R_{on,sp}$ has be reduced by 9.25% and 13.5%, respectively.

According to the discussions above, Fig. 9 directly illustrates the dependence of the BV, $R_{on,sp}$, and Figure Of Merit (FOM) on the L_{GFP} and L_{DFP} of the STFP-OX-LDMOS and STFP-HK-LDMOS. The BV of the two LDMOSs all increase with the increasing of L_{GFP} and L_{DFP}, and then decreases. The $R_{on,sp}$ decreases with the increase of L_{GFP}, and it decreases first and then increases with the increasing of L_{DFP}. The FOM has been widely employed to evaluate the trade-off between the $R_{on,sp}$ and BV of power devices,expresses as $BV^2/R_{on,sp}$. As shown in the subgraphs, the FOM has a maximum value for the different L_{GFP} and L_{DFP}. The simulation results indicate that the STFP-OX-LDMOS and STFP-HK-LDMOS has the maximum FOM of 2.53 MW/cm^2 and 3.85 MW/cm^2, which is 1.8 and 2.7 times in compared with the $FOM = 1.43$ MW/cm^2 of the CONV-LDMOS. Therefore, the trade-off between the $R_{on,sp}$, and BV of STFP-LDMOS is significantly improved by employing the side triangular field plates.

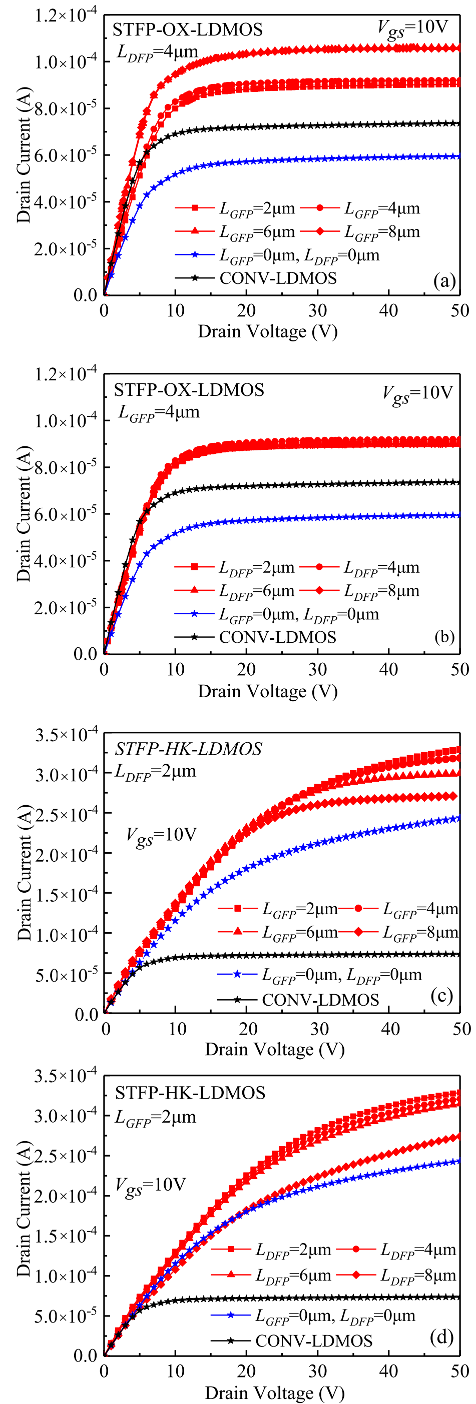

FIGURE 8. Output characteristics for the (a) STFP-OX-LDMOS with different L_{GFP}, (b) STFP-OX-LDMOS with different L_{DFP}, (c) STFP-HK-LDMOS with different L_{GFP}, (d) STFP-HK-LDMOS with different L_{DFP}.

The permittivity ε_D of the trench dielectric is also the key parameter for the performance of the STFP-LDMOS. Fig. 10 gives the simulation results about the influence of ε_D on the BV, $R_{on,sp}$, and FOM of the STFP-LDMOS. The permittivity value of 3.9, 50, 100, and 200 are

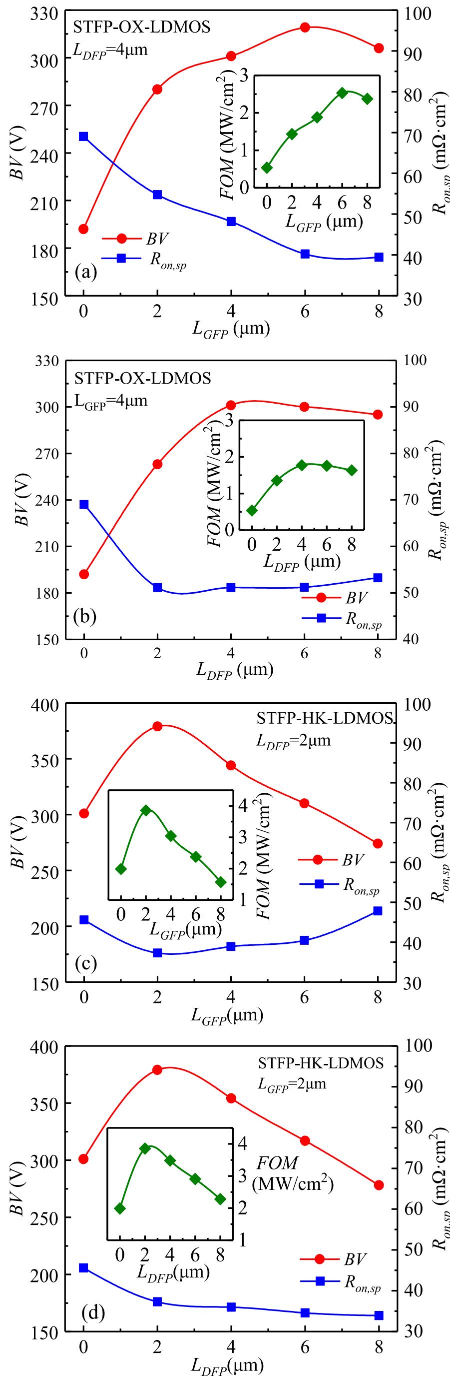

FIGURE 9. Dependences of *BV* and $R_{on,sp}$ for (a) STFP-OX-LDMOS with different L_{GFP}, (b) STFP-OX-LDMOS with different L_{DFP}, (c) STFP-HK-LDMOS with different L_{GFP}, (d) STFP-HK-LDMOS with different L_{DFP}.

corresponding to the high-k materials of SiO_2, $ZrTiO_4$ [13], $SrTiO_3$ [14], and PZT [15]. According to the simulation results, the optimal L_{GFP} and L_{DFP} are 6μm and 4μm for the STFP-LDMOS with $\varepsilon_D = 3.9$, while the optimal L_{GFP} and L_{DFP} are 2μm and 2μm of the STFP-LDMOS with $\varepsilon_D = 50$, 100, and 200. As shown in this figure, the permittivity ε_D mainly influences the *BV* while has less impact on the $R_{on,sp}$. Therefore, the *FOM* is increased with the heightening of ε_D.

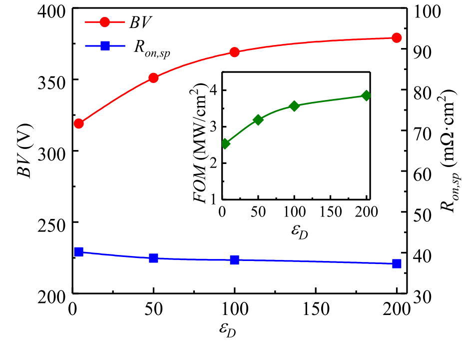

FIGURE 10. Influence of the permittivity ε_D on the *BV*, $R_{on,sp}$, *FOM* of the STFP LDMOS.

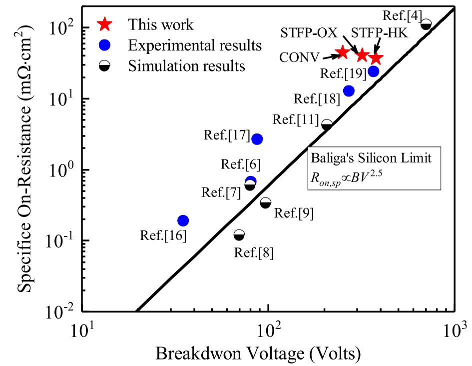

FIGURE 11. $R_{on,sp}$ versus *BV* for different LDMOSs.

The Ron,sp versus BV for the STFP-LDMOS together with some experimental [6], [16]–[19] and simulated data reported previously are shown in Fig. 11. The simulation results of this work are compared with the Baliga's ideal silicon limit curve [20] and other LDMOS structures. We can see that the results of STFP-HK-LDMOS is much closer to the silicon limit than the STFP-OX-LDMOS and CONV-LDMOS. Thus, the STFP-HK-LDMOS exhibits a higher performance and has a better trade-off between the $R_{on,sp}$ and *BV*.

IV. PROCESS REALIZATION

The feasible process steps for fabricating the prototype of the STFP-LDMOS is shown in Fig. 12. The process starts from forming the trenches by etching as shown in Fig. 12(a). Then, the trenches are compactly filled with dielectric material by the chemical vapor deposition technique, as shown in Fig. 12(b). The dielectric isolation technology can be used to form the oxide dielectric pillars without additional masks. Therefore, the STPF-OX-LDMOS has fewer process steps than STFP-HK-LDMOS. In Fig. 12(c), the triangular trenches are etched, which needs much accurate control. The following steps are the deposition of metal into the field plate

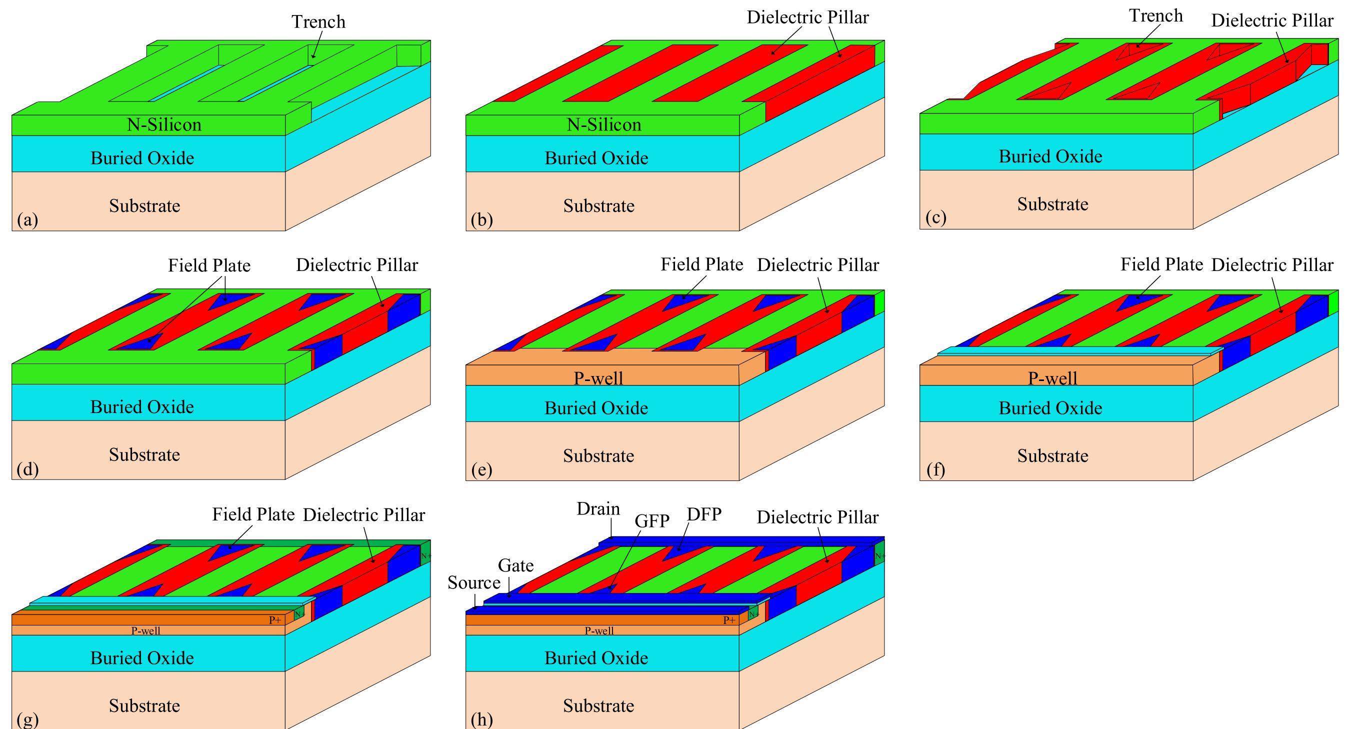

FIGURE 12. Key process steps for fabricating the STFPLDMOS. (a) Etching the trenches. (b) Filling the trenches with dielectric. (c) Etching the field plate trenches. (d) Filling the field plate trenches with metal. (e) Forming the P-well. (f)Forming the gate oxide. (g) Forming N+ and P+ regions. (h) Electrodes fabrication.

trenches and planarization, the STFPs are formed as seen in Fig. 12(d). In Fig. 12(e), the P-well is implemented by the ion implantation method. The ion implantation procedure stands after trench fabrication, the reason is that high temperature generated by etching and deposition process may cause secondary diffusion of impurities. The gate oxide is formed as seen in Fig. 12(f). The N+ and P+ regions are also formed by the ion implantation and annealing as shown in Fig. 12(g). Finally, the metal electrodes are formed as shown in Fig. 12(h). The technological challenges in realizing such a structure mainly consist of the accurate etching and deposition of the side triangular field plate, which needs the special masks to deposit symmetrical plates.

V. CONCLUSION

A novel LDMOS with side triangular field plate has been proposed and investigated in this paper. The gate field plate and drain field plate are introduced to reduce the electric field peak at the P-well/N-drift and N+/N-drift junctions. The field plates together with the dielectric pillars improve the surface electric field and vertical electric field, which results in the incensement of the *BV*. Meanwhile, the doping concentration is also optimized to reduce the $R_{on,sp}$. The influence of the structure parameters, especially the length of the field plates on the device performance is discussed based on the simulation results from the semiconductor device simulator in the TCAD tool. The simulation results show that STFP-LDMOS with a high-k dielectric of $\varepsilon_D = 200$ has the *BV* of 379V, $R_{on,sp}$ of 37.3 mΩ·cm^2, and *FOM* of 3.85 MW/cm^2. Compared to the CONV-LDMOS with the same geometric parameters, the *BV* can be increased by 50%, the $R_{on,sp}$ can be reduced by 13.5%. The *FOM* of the STFP LDMOS is 2.7 times compared with the *FOM* of CONV-LDMOS, which indicates that the STFP device has a great trade-off between the $R_{on,sp}$ and *BV*.

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