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Fault-Tolerant Architecture for Reliable Integrated Gate Drivers

JONGBIN KIM [1], HOON-JU CHUNG [2], AND SEUNG-WOO LEE [1] (Senior Member, IEEE)

1 Department of Information Display and Advanced Display Research Center, Kyung Hee University, Seoul 02447, South Korea
2 School of Electronic Engineering, Kumoh National Institute of Technology, Gumi 39177, South Korea

CORRESPONDING AUTHOR: S.-W. LEE (e-mail: seungwoolee@khu.ac.kr)

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ABSTRACT This paper proposes fault-tolerant (FT) architecture for integrated gate drivers. It can automatically detect faults in the gate driver caused by external physical stress and then immediately repair them as well. As a result, it can contribute to highly reliable display products. The proposed architecture uses redundant circuit structure with fault detection circuit. The detailed algorithm for the proposed method is presented in this paper. Simulation and measurement results verify that the proposed circuit and its driving algorithm operates successfully. Finally, the display system architecture is also suggested for realization of our FT method.

INDEX TERMS Fault tolerance, flexible displays, integrated gate drivers.

I. INTRODUCTION

Current displays have faced much harsher environments than before, since consumers are looking for displays that are bendable and rollable. Also, a stretchable display is being considered as a future display due to its high flexibility and various application [1]–[6]. In order to realize the stretchable display, it is very important to have high reliability against external physical stress [7]–[8]. Moreover, most of display products require the gate driver integrated on a glass substrate to meet the demand for narrow bezel, and cost reduction [9]–[11]. Recently, the gate drivers are even formed on flexible material. For this reason, many failures of current display products are due to the integrated gate drivers. The fault of one stage can breakdown the whole gate driver, since it has a special property that the previous stage affects the next stage [12]. As display operating environment becomes harsher, reliability of the gate driver is getting more important. Thus, if the fault of the gate driver is clearly detected and repaired, it can make a great contribution to improving yield of flexible display products.

Fault-tolerant (FT) technology has been widely used to prevent fatal outcome in computer systems requiring high reliability such as industrial control systems, aircraft control systems, bank transaction systems, etc. It can maintain the functionality of the system against sudden failures at harsh condition. As a result, it helps lifetime improvement of the system. FT technologies for display applications were studied in the past [13], [14]. They adopt redundant circuits commonly used for FT architecture. However, they have not been actively utilized so far. Recently, as the research on flexible displays has just started, the need for related research is emerging.

In this paper, we propose a FT gate driver that can automatically repair the fault when it happens at a specific stage of gate driver due to physical stress during display driving. The proposed circuit uses redundant circuit structure with fault detection circuit [15]. Although this architecture brings increase in circuit area, it is much less expensive than destroying a whole display panel with fault and also improves lifetime of display products. When a scan signal occurs at each stage, it can detect faults such as line disconnection (LD), low voltage stuck (LVS), and high voltage stuck (HVS) by using the detection circuit. Then, it can fix the fault stage automatically with redundant circuit. Consequently, it prevents the fault stage from affecting the whole gate driver and enables continuous operation. In the next section, the fault detection circuit is reviewed. Our proposed FT circuit and its driving algorithm are explained.

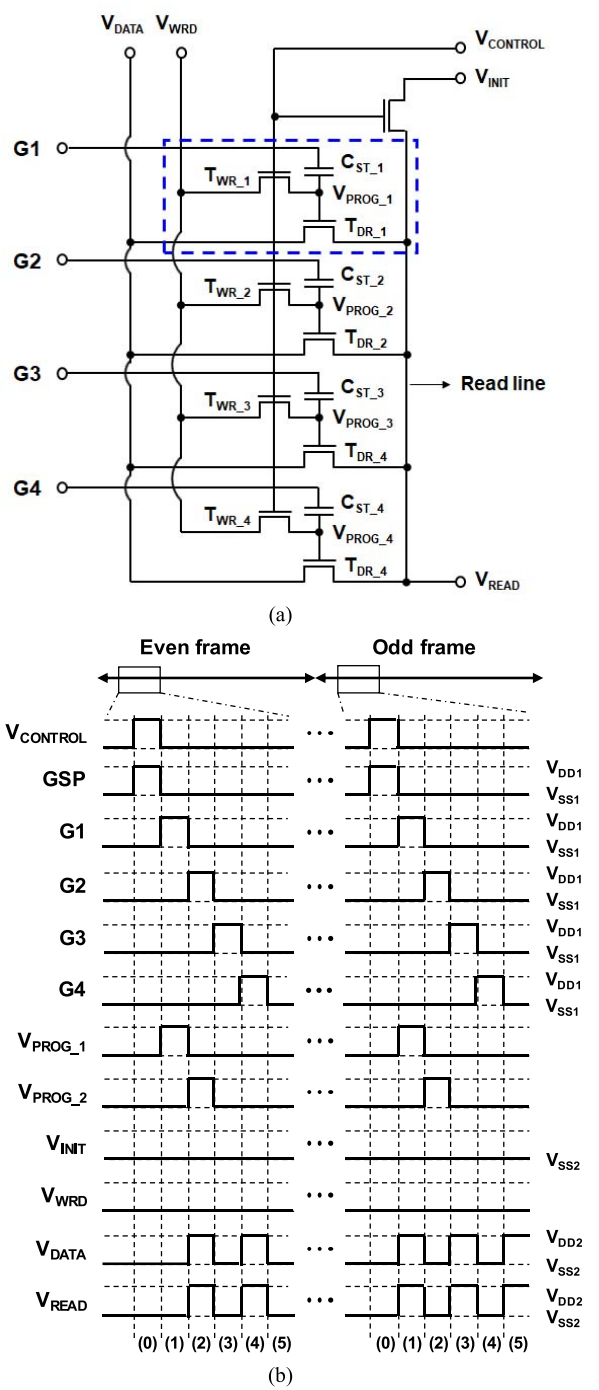


FIGURE 1. (a) The fault detection circuit and (b) its timing diagram [15].

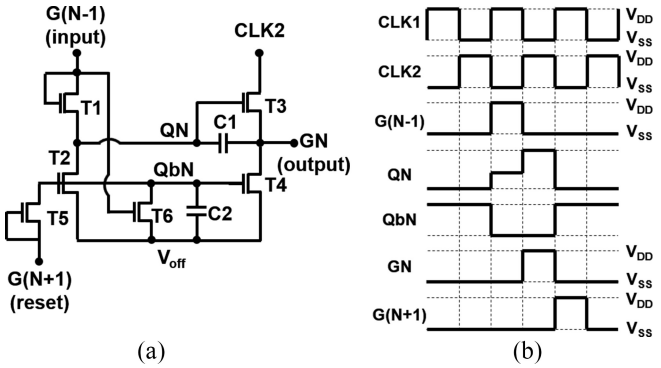


FIGURE 2. (a) Schematic of the gate driver circuit [16]. (b) Corresponding control signals and outputs.

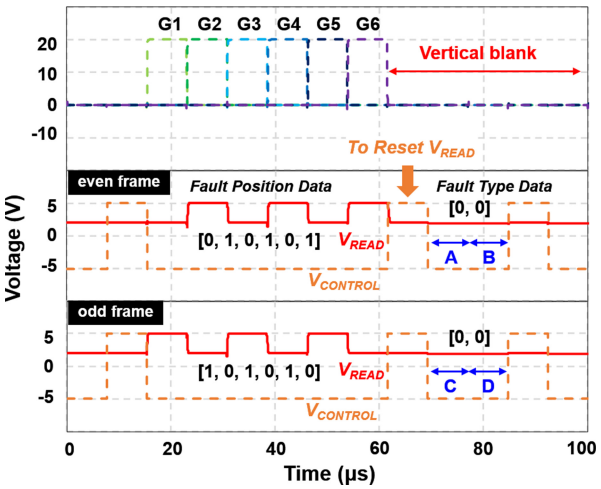


FIGURE 3. Simulated results when a gate driver operates normally [15].

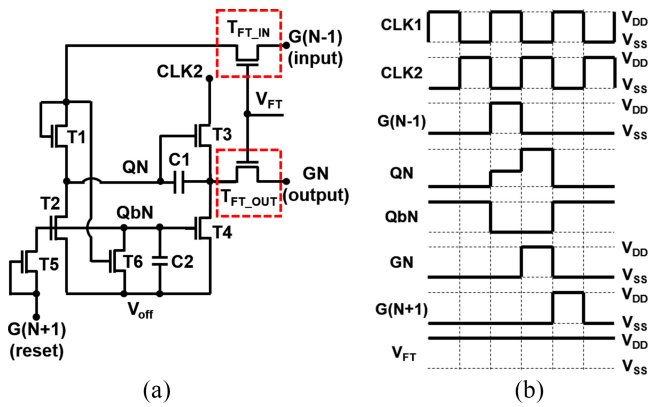


FIGURE 4. (a) Fault-tolerant gate driver circuit and (b) its driving signals.

They are verified with simulation and measurement results as well. Finally, display system architecture with FT architecture is proposed for practical implementation of our proposed technology.

II. REVIEW OF FAULT DETECTION CIRCUIT

A. FAULT DETECTION CIRCUIT

Our proposed FT gate driver uses the fault detection circuit which we proposed in the previous study [15]. Fig. 1 shows the fault detection circuit and its timing diagram. A unit cell enclosed by a dashed line contains one capacitor (C_{ST}) and two thin-film transistors (TFTs), T_{WR} and T_{DR}. The driving TFT (T_{DR}) is used to charge or discharge V_{READ} node; the writing TFT (T_{WR}) to write data; and the storage capacitor (C_{ST}) to bootstrap the node V_{PROG} depending on GN. The operation of the fault detection circuit is divided

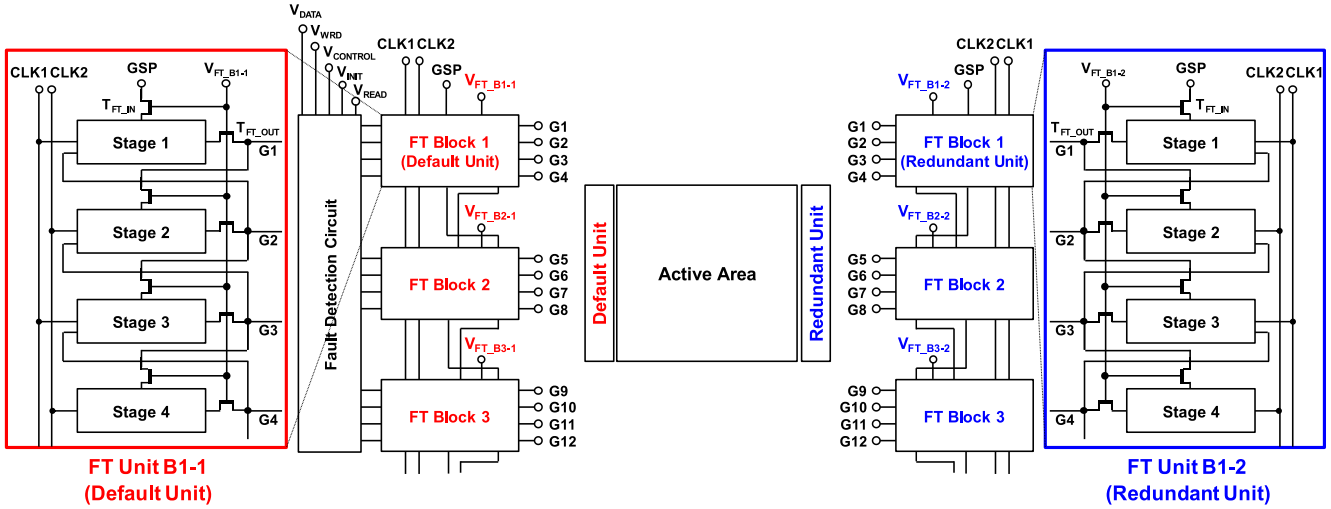


FIGURE 5. Block diagram of fault-tolerant gate driver and fault detection circuit.

into two steps: initializing and programming; charging and discharging.

Initializing and Programming: During period (0) as shown in Fig. 1(b), $V_{CONTROL}$ rises to high and every T_{WR} turns on and every V_{PROG} node ischarged to V_{WRD}. At the same time, the read line (V_{READ}) is initialized to a DC voltage of V_{INIT}.

Charging and Discharging: When the N-th scan signal, GN goes high, GN bootstraps V_{PROG_N} by a capacitor C_{ST_N}. Thus, T_{DR_N} is turned on. Then, the read line can be charged or discharged depending on V_{DATA}. As shown in Fig. 1(b), V_{DATA} is an alternating signal. Let's assume that V_{DATA} with high voltage is applied to odd lines during odd frames and low V_{DATA} to even lines during even frames. Then, during even frames, V_{DATA} becomes high for even time steps such as (2), (4), and so on. During odd frames, V_{DATA} becomes high for odd time steps such as (1), (3), and so on. Since the V_{DATA} waveforms of two consecutive frames are completely reversed, the waveforms of V_{READ} of even and odd frames are reversed. Therefore, when a gate driver normally operates, the waveform of the node V_{READ} is the same as the V_{DATA}. In this way, it is possible to detect whether the scan signal is properly applied to the display panel by checking the difference between V_{DATA} and V_{READ}.

B. FAULTS OF GATE DRIVER

Here, we briefly review how to detect faults with a gate driver shown in Fig. 2 [16]. The fault detection circuit can detect three types of faults of a gate driver such as LD, LVS and HVS. Fig. 3 shows simulated results when a gate driver operated normally in the previous study [15]. We can distinguish the types of faults when we carefully investigate V_{READ} during vertical blank. During the vertical blank, the two values of V_{READ} right after resetting V_{READ} in even frame are assigned to A and B. The counterparts in odd frame are assigned to C and D. Let's define A, B, C, and

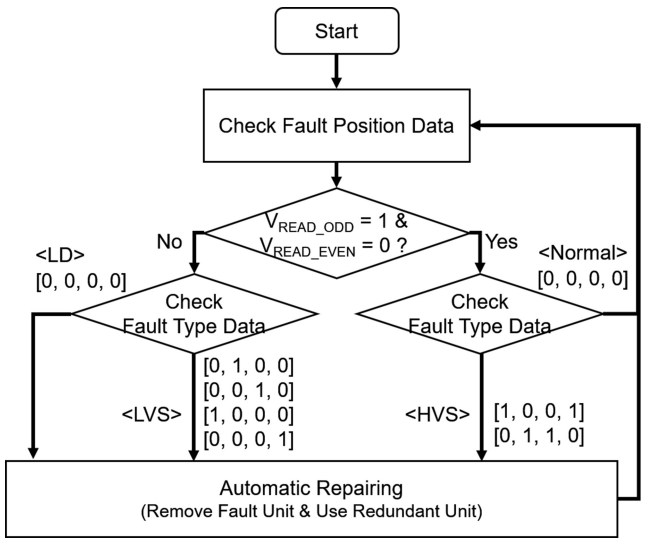
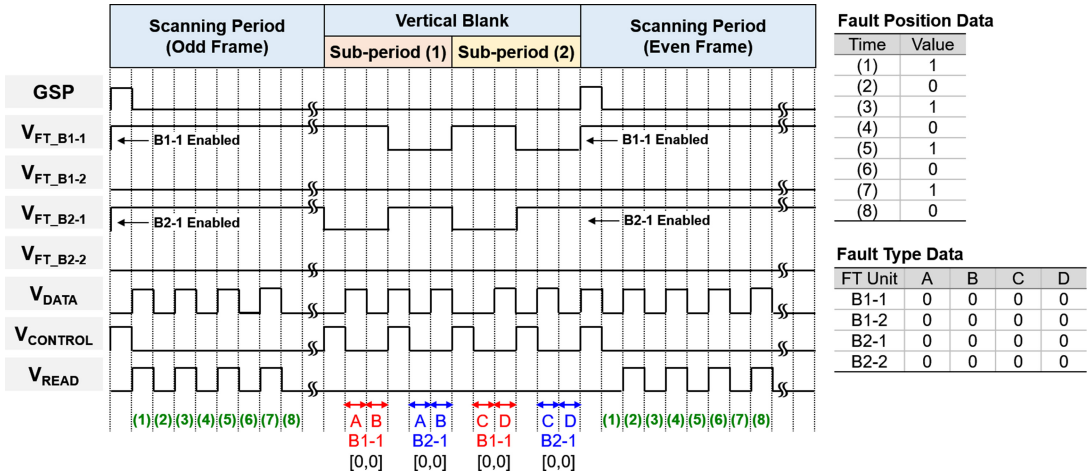


FIGURE 6. Flow chart of our fault-tolerant algorithm for odd frames.

D as *fault type data*. Then, we can find that the fault type data [A, B, C, D] are [0, 0, 0, 0] if there is no error in the circuit as shown in Fig. 3. In this way, the fault type data can determine the types of the faults. During our study, we found that fault type data of LVS and HVS in the previous work [15] were incorrect. Thus, we have fixed the fault type data and summarized as shown in Table 1. When the LVS occurs at the second stage, G1 repeatedly generates high pulses corresponding to the clock signal and G3 remains low. In this case, the fault type data are [0, 1, 0, 0]. When G3 is stuck at high (HVS), G1 and G4 generate the same repetitive output. Thus, the fault type data become [1, 0, 0, 1].Finally, when a certain line of a gate driver is disconnected (LD), the fault type data become [0, 0, 0, 0] which is the same as the fault type data of normal operation. However, it is possible to distinguish LD from normal operation by checking the



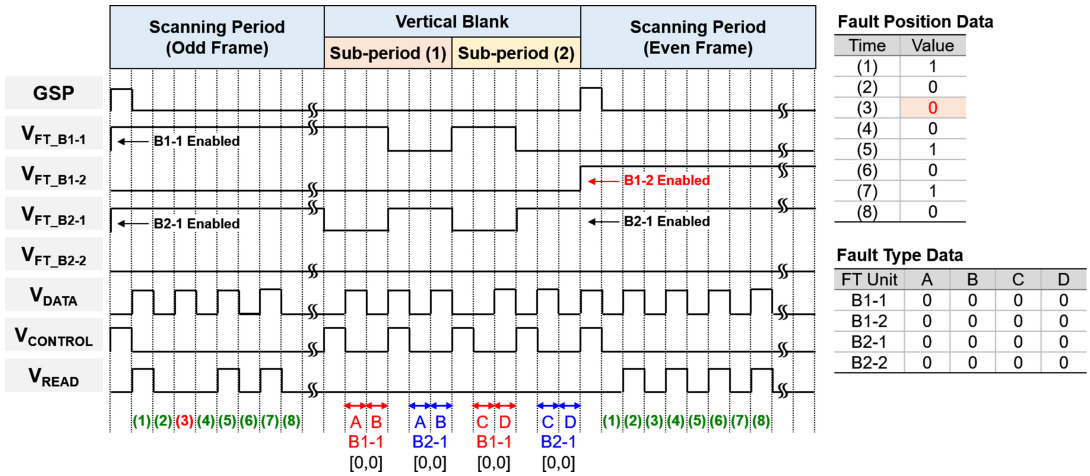
Fault Position Data

Time	Value
(1)	1
(2)	0
(3)	1
(4)	0
(5)	1
(6)	0
(7)	1
(8)	0

Fault Type Data

FT Unit	A	B	C	D
B1-1	0	0	0	0
B1-2	0	0	0	0
B2-1	0	0	0	0
B2-2	0	0	0	0

FIGURE 7. Timing chart of fault-tolerant operation when gate driver operating normally.



Fault Position Data

Time	Value
(1)	1
(2)	0
(3)	0
(4)	0
(5)	1
(6)	0
(7)	1
(8)	0

Fault Type Data

FT Unit	A	B	C	D
B1-1	0	0	0	0
B1-2	0	0	0	0
B2-1	0	0	0	0
B2-2	0	0	0	0

FIGURE 8. Timing chart of fault-tolerant operation when line disconnection (LD) occurs at the FT unit of B1-1.

TABLE 1. Fault type data.

A	B	C	D	Type of Fault
0	0	0	0	Normal Operation or Line Disconnection (LD)
0	1	0	0	Low Voltage Stuck (LVS)
0	0	1	0	
1	0	0	0	
0	0	0	1	
1	0	0	1	High Voltage Stuck (HVS)
0	1	1	0	

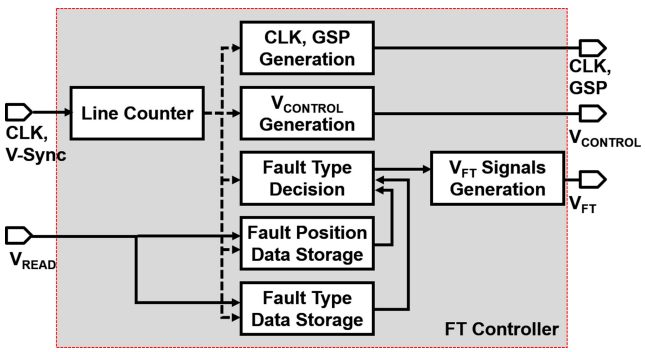
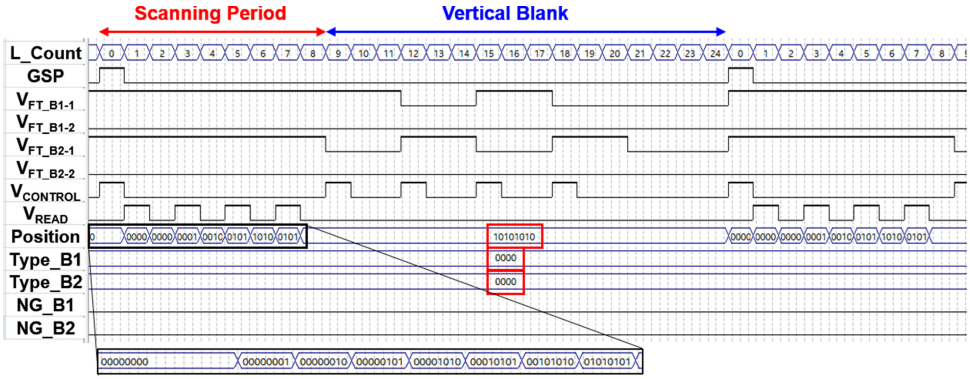


FIGURE 9. Block diagram of FT controller to detect faults and repair them.

V_{READ} signal during the scanning period. Here, we define the states of V_{READ} during the scanning period as *fault position data*. If there are no errors in the gate driver, V_{READ} should be equal to V_{DATA} during the scanning period. When a frame number is odd, fault position data during odd frame are [1, 0, 1, 0, 1, 0] as shown in Fig. 3. In the next section, we describe the FT architecture and how it detects and repairs faults based on fault type data and fault position data.

III. FAULT-TOLERANT ARCHITECTURE FOR GATE DRIVERS

Our proposed FT architecture uses redundant circuit structure which can replace fault parts in a gate driver. The fault

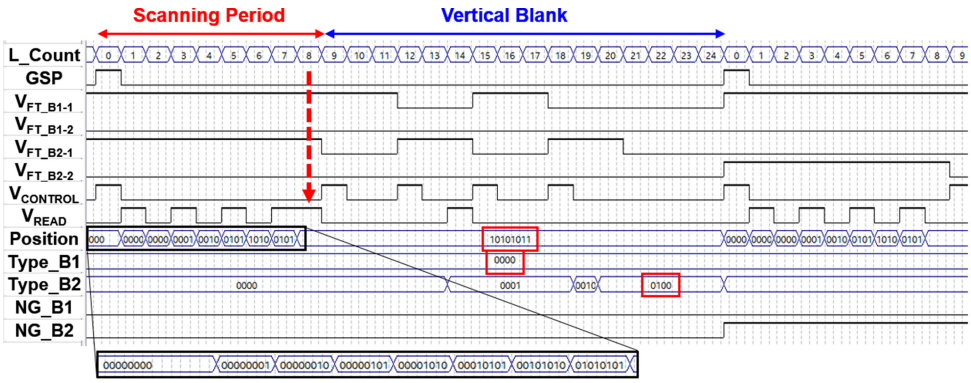


(a)

Fault position data		Fault type data	
Time	Value	Unit	[A,B,C,D]
(1)	1	B1-1	[0,0,0,0]
(2)	0		
(3)	1		
(4)	0		
(5)	1	B2-1	[0,0,0,0]
(6)	0		
(7)	1		
(8)	0		

(b)

FIGURE 10. (a) Simulated results and (b) summarized data when gate driver operating properly.

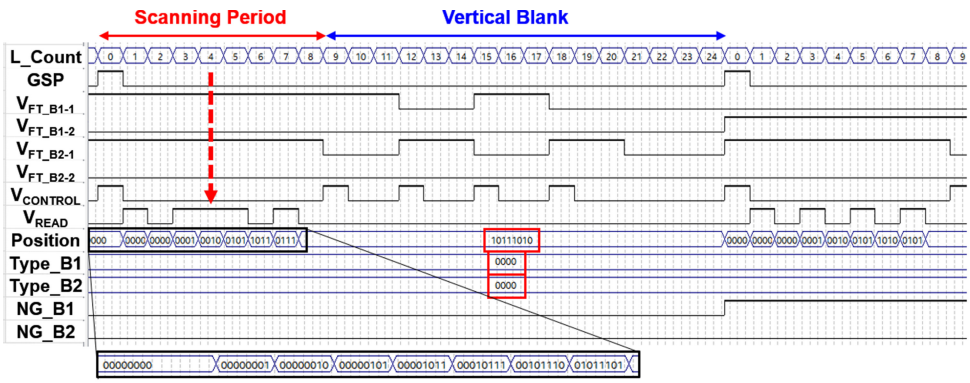


(a)

Fault position data		Fault type data	
Time	Value	Unit	[A,B,C,D]
(1)	1	B1-1	[0,0,0,0]
(2)	0		
(3)	1		
(4)	0		
(5)	1	B2-1	[0,1,0,0]
(6)	0		
(7)	1		
(8)	1		

(b)

FIGURE 11. (a) Simulated results and (b) summarized data when low voltage stuck (LVS) occurs at B2-1.



(a)

Fault position data		Fault type data	
Time	Value	Unit	[A,B,C,D]
(1)	1	B1-1	[0,0,0,0]
(2)	0		
(3)	1		
(4)	1		
(5)	1	B2-1	[0,0,0,0]
(6)	0		
(7)	1		
(8)	0		

(b)

FIGURE 12. (a) Simulated results and (b) summarized data when line disconnection (LD) occurs at B1-1.

tolerance of a gate driver is implemented by turning the fault parts off and redundant counterparts on. Fig. 4 shows FT gate driver circuit and its driving scheme used in this paper. Based on the gate driver shown in Fig. 2, T_{FT_IN} and T_{FT_OUT} are added to control the input and output of a stage as shown in Fig. 4(a). The input and output of a single stage of the gate driver are enabled at the same time by controlling V_{FT} signal. If the V_{FT} is high, the stage works normally. The V_{FT} with a low voltage turns off T_{FT_IN} and T_{FT_OUT} and disables the operation of the stage. If we control each stage, it needs a lot of V_{FT} signals. In the case of the resolution of full high definition (FHD), 2160 lines are totally required because two signals with opposite levels per stage disable the fault part and enable the redundant counterpart, which occupies huge area. Thus, the gate driver is divided into several blocks of FT circuits in this paper to reduce circuit area while maintaining the number of individually controllable stages. For example, assuming there are 10 FT

blocks in the gate driver, the fault tolerance can be achieved with 20 signal lines for FHD resolution. In addition, if TFTs feature improved reliability against external physical stress, it is expected that the number of FT blocks can be decreased, and thus corresponding signal lines are also further reduced as well.

Fig. 5 shows a block diagram of our proposed FT gate driver. One FT block contains two kinds of FT units, default and redundant units. The default and redundant units are placed on the both bezels of a display panel, respectively. In Fig. 5, B1-1 is the default unit for normal operation and B1-2 is the redundant unit for repairing. These FT units in a single FT block are controlled by two V_{FT} signals, V_{FT_B1-1} and V_{FT_B1-2} for the default and redundant units, respectively. One FT block can cover several scan lines. As shown in Fig. 5, for example, FT block 1 is responsible for scan lines of G1 to G4. In this way, FT block N is for G(4N-3) to G(4N) lines.

Our proposed FT gate driver is combined with the fault detection circuit shown in the previous section. If a fault is detected by the fault detection circuit, the default unit containing the fault stage is disabled and the corresponding redundant unit is enabled. The fault detection circuit is composed of only two transistor and one capacitor per scan line. Thus, this circuit does not greatly increase the overall circuit area. The size of T_{WR} is small since it only charges the storage capacitor C_{ST}. Also, C_{ST} requires a little area to bootstrap the node V_{PROG}. The driving TFT, T_{DR} should charge V_{READ} line which has a similar electrical load as a clock signal line. When we model the electrical load of V_{READ} line as 5 kΩ and 120 pF for FHD resolution, the width and length of T_{DR} are determined to be 20 μm and 5 μm, respectively, to charge V_{READ} line. Thus, the area of the fault detection circuit is estimated to be under 100 μm $\times$ 100 μm. Considering a 55-inch FHD display, it only occupies 0.0008 % of the whole display panel area. If the fault detection circuit has errors, there is no way to discover faults of gate drivers. However, the break-down probability of the fault detection circuit is very low because its area occupies only 0.0008% of the whole circuit. If only one FT unit is activated for a long time, T_{FT_IN} and T_{FT_OUT} in the unit can suffer from gate bias stress due to constant voltages of V_{FT} signals. To prevent the degradation of the both transistors, it is necessary for the default and redundant units to be alternately active to alleviate the continuous stress.

Fig. 6 shows a flow chart of our FT algorithm. The algorithm consists of detecting faults of a gate driver and repairing the detected faults automatically. To detect the faults, fault position data are checked during scanning period. If there are no errors in the gate driver, V_{READ} should be equal to V_{DATA} during the scanning period. If a frame number is odd, for example, V_{READ} is high for odd time steps such as (1), (3), and so on as shown in Fig. 1. It is represented by $Vc = 1$ as shown in Fig. 6. In the same way, $V_{READ\_EVEN} = 0$ since V_{READ} is low for even time steps. In addition to the case of no errors, the case of HVS also satisfies that $V_{READ\_ODD} = 1$ and $V_{READ\_EVEN} = 0$, simultaneously. On the contrary, the cases of LD and LVS do not satisfy this condition. Thus, in order to determine the types of faults clearly, fault type data are also checked during the vertical blank as shown in Fig. 6. The fault type data can finally narrow down the types of faults. After fault detection, automatic repairing is performed except the case of the normal operation. The detected fault stage of the gate driver is automatically repaired by replacing it with the corresponding redundant FT-unit.

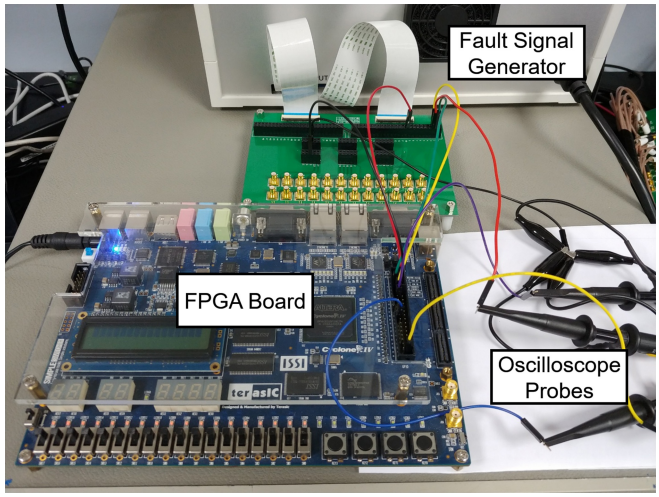
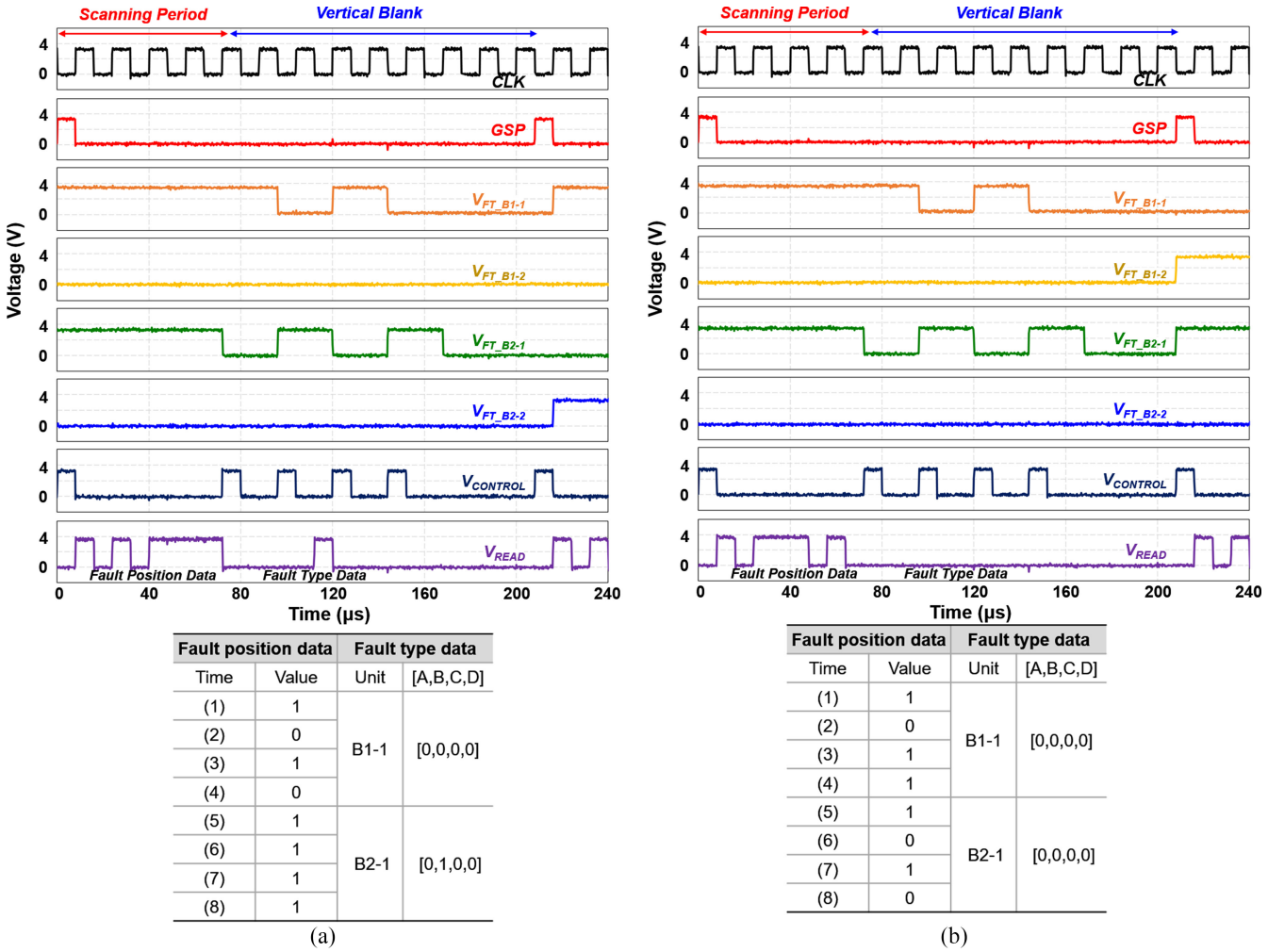


FIGURE 13. Photo of measurement setup for FPGA verification.

Fig. 7 shows a timing chart of our FT operation when a gate driver works normally to describe detailed operation of the algorithm, based on the FT blocks of Fig. 5. One FT block is responsible for four scan lines. During the scanning period, fault position data are checked. If HVS happens or there are no errors in the gate driver, $V_{READ\_ODD} = 1$ and $V_{READ\_EVEN} = 0$. Thus, the fault position data shown in Fig. 7 are [1, 0, 1, 0, 1, 0, 1, 0]. Next, the fault type data are checked during the vertical blank. $V_{CONTROL}$ signal resets V_{READ} in the fault detection circuit so that we can check states of each FT unit during the vertical blank. The vertical blank is divided into two periods. The only difference between them is that V_{DATA} signals at each sub-period are opposite in polarity to each other. FT units are sequentially scanned by corresponding V_{FT} signal, to detect fault of each FT unit. Thus, we can obtain the fault type data, [A, B, C, D] of all the FT units by reading out V_{READ} as shown in Fig. 7. We can observe that the gate driver has no errors, where the fault type data are [0, 0, 0, 0]. As a result, repairing is not needed after the vertical blank: The fault unit is enabled, and redundant counterpart is disabled. As shown in Fig. 7, V_{FT_B1-1} signal goes high to activate B1-1 unit again. B2-1 unit also has no fault, thus V_{FT_B2-1} signal becomes high to maintain the unit.

Fig. 8 shows a timing chart when LD occurs at B1-1 unit. The fault position data are [1, 0, 0, 0, 1, 0, 1, 0] where V_{READ} at the third stage is low. Thus, $V_{READ\_ODD} = 0$ during (3)



Fault position data		Fault type data	
Time	Value	Unit	[A,B,C,D]
(1)	1	B1-1	[0,0,0,0]
(2)	0		
(3)	1		
(4)	0		
(5)	1	B2-1	[0,1,0,0]
(6)	1		
(7)	1		
(8)	1		

(a)

Fault position data		Fault type data	
Time	Value	Unit	[A,B,C,D]
(1)	1	B1-1	[0,0,0,0]
(2)	0		
(3)	1		
(4)	1		
(5)	1	B2-1	[0,0,0,0]
(6)	0		
(7)	1		
(8)	0		

(b)

FIGURE 14. **Measured results when (a) low voltage stuck (LVS) and (b) line disconnection (LD) occur.**

as shown in Fig. 8. The fault of the FT unit is either LVS or LD. It is easy to identify the fault by checking the fault type data during the vertical blank. As shown in Fig. 8, the fault type data are [0, 0, 0, 0]. As a result, we can see that the LD occurs, and B1-2 unit is activated right after the vertical blank since the fault stage belongs to B1-1 unit.

IV. RESULTS AND DISCUSSION

The operation of the proposed architecture was verified by digital simulation using a hardware description language, Verilog HDL. Fig. 9 shows a block diagram of FT controller. The FT controller module generates clocks and a gate start pulse (GSP) of an integrated gate driver. It transfers $V_{CONTROL}$ signal to control the fault detection circuit. Also, if the fault detection circuit transfers V_{READ} signals to the FT controller module, it can decide whether there are faults or not, and generate appropriate V_{FT} signals. In this simulation, we assumed an integrated gate driver with eight stages. Each FT block was composed of four stages. Thus, there were two FT blocks and the total number of FT units was four including default and redundant units. Fig. 10(a) shows simulated waveforms when the gate driver operated normally. After a GSP signal went high for the first time, $V_{FT\_B1\text{-}1}$ and $V_{FT_B2\text{-}1}$were high voltage to enable FT units of B1-1 and B2-1, respectively. During the scanning period, V_{READ} were stored to lease significant bit (LSB) of fault position data. Then, a bit shift operation is performed toward most significant bit (MSB) at every line time. In this way, the fault position data were determined to be [1, 0, 1, 0, 1, 0, 1, 0], and the fault type data were [0, 0, 0, 0] as shown in Fig. 10(b). Thus, we concluded that the gate driver was normal according to the FT algorithm shown in Fig. 6. Note that NG_B1 and NG_B2 are defined as *block data* to provide information of whether FT units have faults or not. When a fault occurs at a FT unit, its block data become '1', whereas those of normal FT unit are '0'. Therefore, the fault units can be automatically repaired by checking the block data right after the vertical blank.

Fig. 11(a) shows simulation results when LVS occurs. During the scanning period, V_{READ} at even numbers of L_count should be '0' for normal operation. However, the fault position data of (8) was '1' (denoted by an arrow).

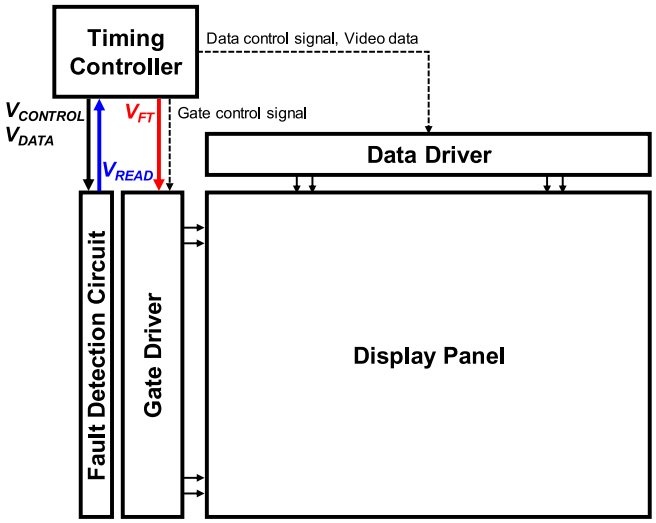


FIGURE 15. Schematic diagram of our proposed display architecture with the fault-tolerant gate driver and fault detection circuits.

Thus, the type of fault may be either LD or LVS in the FT unit. The fault type data of the unit were [0, 1, 0, 0] as shown in Fig. 11(b). As a result, we could determine that LVS occurred at B2-1 unit. Note that NG_B2 became '1' which means B2-1 has the fault. We could see a redundant unit B2-2 was enabled instead of B2-1, in order to repair the fault unit automatically right after the vertical blank. Based on the block data, V_{FT} signals control the default and redundant FT units. The block data are stored in a memory.

Fig. 12(a) shows simulation results when LD occurs. During the scanning period, the fault position data were [1, 0, 1, 1, 1, 0, 1, 0], where the fault position data of (4) was '1' (denoted by an arrow). During the vertical blank, the fault type data were [0, 0, 0, 0], which were different from the data of LVS. We could determine that LD occurs at B1-1 unit. The block data NG_B1 became '1' after the vertical blank. Therefore, the redundant unit B1-2 was activated by $V_{FT\_B1\text{-}2}$, whereas B1-1 was disabled.

The operation of the FT architecture was also verified with measurement results using a field programmable gate array (FPGA) board and a fault signal generator. Fig. 13 shows a measurement setup for the verification. The FPGA board and the fault signal generator act as a timing controller (T-CON) of display system and the fault detection circuit, respectively. All input and output signals of them were measured with an oscilloscope. The FPGA board generated clocks and control signals of an integrated gate driver. It also created $V_{CONTROL}$ signal used in the fault detection circuit. When the fault signal generator transferred V_{READ} signals to the FPGA board, it generated V_{FT} signals depending on the types of the faults.

Fig. 14(a) shows measured results when LVS occurred. We assumed that the gate driver consisted of eight stages for the measurement. One line time was set to be 8 μs. Fault position data of (7) was '1', which means V_{READ_ODD} was not '0'. Thus, the type of fault may be either LD or LVS. Fault type data of B1-1 and B2-1 were [0, 0, 0, 0] and [0, 1, 0, 0], respectively, which indicates that LVS occurred at B2-1. We could observe that $V_{FT\_B2\text{-}2}$ became high after the vertical blank to enable a redundant unit, B2-2. On the other hand, $V_{FT\_B2\text{-}1}$ got low to disable B2-1. Fig. 14(b) shows measured results when LD happened. Fault position data of (3) was '1', and fault type data of B1-1 and B2-1 were both [0, 0, 0, 0]. As a result, the FPGA board determined the type of fault to be LD. We can see the FPGA board made $V_{FT\_B1\text{-}2}$ high to enable redundant unit B1-2 instead of B1-1. From the measured results, we have verified that the proposed FT architecture operates well.

Fig. 15 shows a schematic diagram of our proposed display architecture with the FT gate driver and fault detection circuits. A T-CON supplies V_{FT} signals to the FT gate driver to turn on each FT unit. At the same time, $V_{CONTROL}$ and V_{DATA} are sent to the fault detection circuit. Then, the T-CON reads out V_{READ} signals from the fault detection circuit in order to obtain fault position data and fault type data. Based on them, the T-CON transmits V_{FT} signals again to automatically repair the detected fault units.

V. CONCLUSION

In this paper, we have proposed FT gate driver circuits which can repair the fault stage automatically. Our proposed circuits have the fault detection circuit where the types of faults can be determined during the display driving. In addition, the detected faults are immediately repaired by redundant circuit architecture. The detailed algorithm for various faults was proposed. Also, it was verified with simulated and measured results. Finally, this paper showed that the proposed FT circuit and its driving scheme can be directly applied to current display system architecture. We think our proposed circuit and architecture can be applied to the integrated gate driver of scalable display which is vulnerable to physical stress. Therefore, we believe that our proposed technology will contribute to a yield and reliability of the stretchable display.

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JONGBIN KIM received the B.S. and M.S. degrees in information display from Kyung Hee University, Seoul, South Korea, in 2010 and 2012, respectively, where he is currently pursuing the Ph.D. degree with the Department of Information Display. His research interests include driving methods and circuits for various types of displays, including LCD and OLED displays.

HOON-JU CHUNG received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea, in 1994, and the M.S. and Ph.D. degrees from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 1997 and 2002, respectively. He is currently a Full Professor with the School of Electronic Engineering, Kumoh National Institute of Technology.

SEUNG-WOO LEE (SM'10) received the B.S. and M.S. degrees in electrical engineering and the Ph.D. degree from the Korea Advanced Institute of Science and Technology in 1993, 1995, and 2000, respectively, where he conducted research on integrated driver circuits for poly-Si TFT-LCDs.

In 2000, he joined Samsung, where his research has focused on the development of key driving technologies for active-matrix liquid-crystal displays. He has played a key role in image quality enhancement, high-end LCD timing-controller design, FPGA evaluation of new driving schemes, next-generation LCD interface technologies, and advanced LCD driving schemes for large-size TV applications. He was also in charge of the development of analog–digital mixed-signal ICs for TFT-LCDs. After joining Kyung Hee University, he has been studying novel display systems and visual perception. He is currently a Full Professor with the Department of Information Display, Kyung Hee University, Seoul, South Korea.

Prof. Lee was a recipient of the 2008 Chester Sall Award from IEEE Consumer Electronics Society in 2010. He has been active as a Senior Member of Society for Information Display since 2010.