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A Low-Energy High-Density Capacitor-Less I&F Neuron Circuit Using Feedback FET Co-Integrated With CMOS

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ABSTRACT We have developed a capacitor-less I&F neuron circuit with a dual gate positive feedback field-effect transistor (FBFET) and successfully co-integrated FBFET and CMOS in a wafer. By implementing the neuron circuit with FBFET, we can overcome the limits of conventional CMOS, reduce energy consumption, and imitate the biological neuron. The floating body of the FBFET can replace the membrane capacitor that occupies a large area and performs leaky integration of the neuron. Due to the extremely low sub-threshold swing of the FBFET (less than 0.528mv/dc), energy consumption of the neuron is significantly reduced by suppressing sub-threshold current. Finally, we analyzed the fabricated neuron circuit operation, retention time of the integrated charges and energy consumption compare to conventional CMOS neuron circuit.

INDEX TERMS Integrate-and-fire neuron circuit, positive feedback FET, low energy consumption, floating body effect.

I. INTRODUCTION

Recently, various types of the artificial neural model such as I&F neuron, H-H neuron, log domain neuron and tau-cell neuron have been presented [1]–[7]. One of them, integrate-and-fire (I&F) neuron model was introduced to implement basic property of biological neuron behavior such as integration, action potential, threshold and refractory. However, conventional CMOS based neuron circuits for these biological functions require a large membrane capacitor (C_{mem}) for integration as well as a number of transistors that result in large cell size and high energy consumption. Besides, the first inverter (INV1) that is connected to C_{mem} is responsible for the largest portion of the energy consumption, because short-circuit current (I_{SC}), that is called crowbar current also, flows through the INV1 from the power supply voltage (V_{DD}) to ground, while the C_{mem} is charged to the switching voltage of the INV1 (Fig. 1). This problem is more serious, especially for artificial neuron circuits because the membrane potential is increased very slowly only when the post synaptic signal is applied. So the INV1 has been called as starved inverter in analog neuron circuit [8], [9]. In order to realize high density and low energy, the neuron citcuit using non-volatile memory such as RRAM, phase change material, spin-transfer torque devices, floating body MOSFET, NEMS devices and insulator to metal transition device are reported [10]–[22]. But these devices have low endurance, stochastic switching problems for use in neuron circuits and most of the materials that construct the device are not compatible with CMOS process. In previous works, we have analyzed the energy consumption caused by the I_{SC} in conventional neuron circuit and developed low-energy neuron circuit with positive feedback FET (FBFET) that perfectly suppressed the I_{SC} and investigated operation mechanism and electrical characteristics of the FBFET by TCAD and

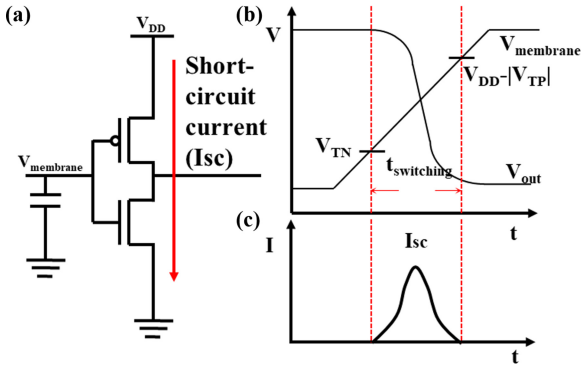

FIGURE 1. **(a) Circuit diagram of membrane capacitor and first inverter stage. (b) Output voltage of INV1 curve when Vmembrane slowly increases. (c) Short-circuit current during inverter switching.**

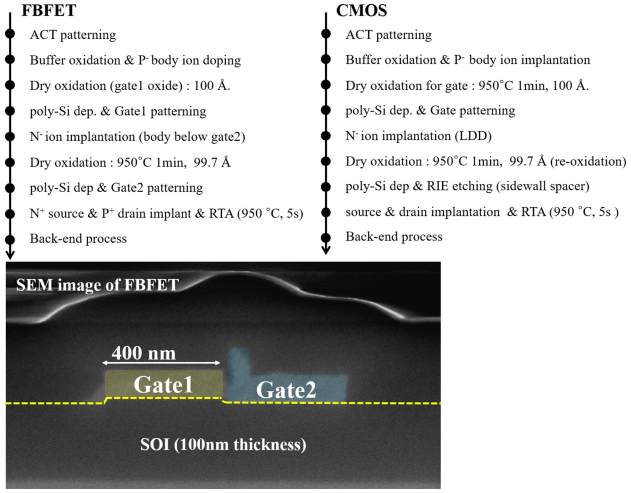

FIGURE 2. **Fabrication flow of FBFET, CMOS and SEM image of FBFET. Thanks to the process of FBFET is almost same with standard CMOS process, the FBFET can be co-integrated with CMOS, adding only a mask for gate2 patterning.**

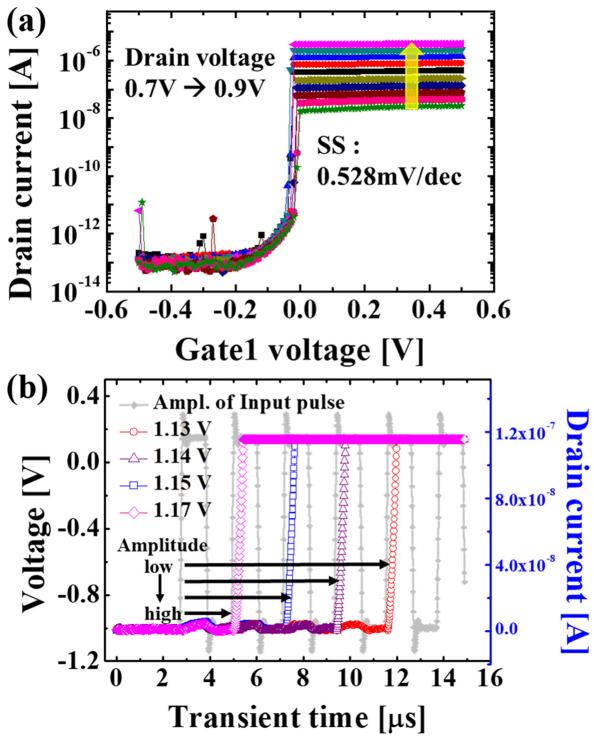

FIGURE 3. **Measurement result of (a) I_d-V_{G1} curves according to the drain voltage with the SS less than 0.53 mV/dec, and (b) when input pulse is applied to various amplitude of the V_{G1}.**

SPICE simulation work [23]. But, in previous works the neuron circuit used membrane capacitor to integrate input signals.

In this work, we propose a capacitor-less neuron circuit using floating body of the FBFET to integrate and reduce the energy consumption by suppressing the I_{SC}. And we have co-integrated the FBFET and CMOS circuit in a chip, by adding only one supplement mask for second gate patterning. The proposed circuit is an important milestone for artificial neuron circuit with new device and application of FBFET as logic device. Using CMOS alone cannot prevent the I_{sc}, which is the biggest problem of analog circuits. In addition, although the FBFET has excellent switching characteristics [24]–[32], there is a serious disadvantage that it cannot simply replace the CMOS. For this reason, FBFET has been studied as a memory device only, but there are few applications as logic devices. By implementing the neuron circuit with co-integrating the CMOS and FBFET in a chip, we can overcome the disadvantages of each device, dramatically reduce energy consumption and area, and imitate the biological characteristics of the neuron.

II. FABRICATION METHOD

The fabrication process of proposed neuron circuit and FBFET is shown in Fig. 2. As the fabrication method is based on standard CMOS procedure, only a mask for gate2 patterning was supplemented, the devices are co-integrated in a chip. First, active patterning and p-type body doping (BF_2 with a dose of 1×10^{13} cm^{-2}) is performed to adjust the threshold voltage. So NMOS and FBFET has equal body concentration. Then, 10nm-thick SiO_2 is grown by dry oxidation at 950°C and n^+-doped poly-Si (for first gate of FBFET and CMOS gate) is deposited. After the first gate patterning, n-type dopants (As with a dose of 2×10^{13} cm^{-2}) are implanted for the potential well below the gate2 and lightly doped drain of NMOS, and buffer oxide for implantation is removed by HF wet etching. The second gate oxidation is performed to 10 nm to separate gate1 and gate2. Then n^+-doped poly-Si is deposited for gate2 of the FBFET and sidewall spacer of NMOS, then the second gate etching is carried out both FBFET and CMOS. After source & drain implantation (BF_2 for p-type, as for n-type with a dose of 5×10^{15} cm^{-2}), rapid thermal annealing (RTA) is performed at 950°C with 5 s. Finally, the TEOS for inter-layer dielectric (ILD) is deposited, and contact hole etching and pre-metal cleaning (dHF, 10s) is performed. The metal stack (Ti / TiN / Al / TiN, 300 / 300 / 4000 / 300A) are deposited using metal

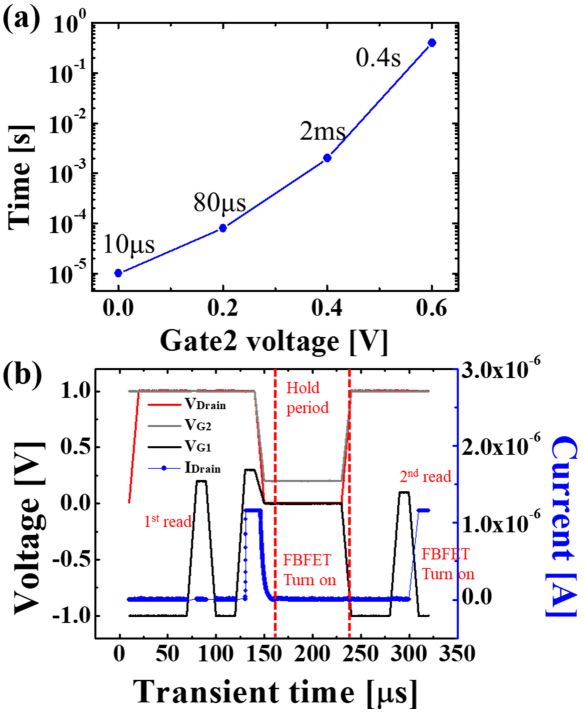

FIGURE 4. (a) Measurement result of retention time of the accumulated electrons in the floating body according to V_{G2}. (b) Voltage scheme (1st read: V_{drain} = 1V, V_{G1} = 0.2V, V_{G2} = 1V, FBFET turn on: V_{drain} = 1V, V_{G1} = 0.4V, V_{G2} = 1V, Hold period: V_{drain} = 0, V_{G1} = 0, V_{G2} = hold voltage, 2nd read: V_{drain} = 1V, V_{G1} = 0.15V, V_{G2} = 1V).

sputter. Metal patterning and ICP metal etching is performed. Finally, back-end metal process is performed.

III. DEVICE MEASUREMENT RESULTS

In our previous work, we analyzed operation mechanism and electrical characteristics of the FBFET [23]. In this fabrication, we improved sub-threshold slop (SS) and on/off current ratio by reducing gate length, rapid thermal annealing time and increasing annealing temperature. The measurement result of drain current (I_d)-gate1 voltage (V_{G1}) curves according to the drain voltage is shown in Fig. 3(a). The FBFET has super steep switching characteristics with a SS of less than 0.528 mV/dec. As the input pulse is applied to gate1, injected electrons are integrated in the floating body below gate2. If the electron concentration exceed the threshold for feedback, the FBFET is turned on by the positive feedback between the electrons and potential barrier. By using this charge accumulation property, the FBFET substitutes membrane capacitor. The smaller the amplitude of the pulse, the fewer electrons are accumulated in the floating body, so a larger number of pulses are required to turn on the FBFET (Fig. 3 (b)). The measurement result of the retention time of the accumulated electrons in the floating body according to V_{G2} is shown in Fig. 4 (a) and Fig. 4 (b) shows measurement voltage scheme. The 1st read voltage that is lower than V_T of the FBFET is applied to gate1. Then the FBFET is turned on by applying a voltage higher than V_T, and the electrons are accumulated in the floating body. During hold time, gate1 and drain are grounded, and hold voltage is applied to gate2. After the hold time, the 2nd read voltage is applied. If the FBFET is turned on, the electrons remain in the floating body, but if the FBFET does not turn on, most of the electrons are removed by recombination. The retention time was defined as the hold period that the FBFET was able to turn on again. As the V_{G2} is increased, retention time is increased exponentially. If the 0.6 V hold voltage is applied to gate2, the retention time is increased to 0.4s. So we can control the charge retention time by applying V_{G2}, and implement adjustable leaky integration.

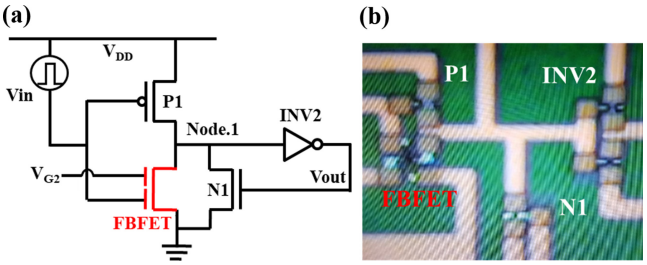

FIGURE 5. (a) Proposed capacitor-less I&F neuron circuit diagram and (b) microscopy image of fabricated circuit.

IV. CAPACITOR-LESS NEURON CIRCUIT

Fig. 5 illustrates the proposed capacitor-less neuron circuit diagram and microscopy image of fabricated circuit. The first inverter consists of the FBFET and a p-type MOSFET (P1), and the FBFET performs temporal integration function. To verify the circuit operation, circuit simulation was performed by the SILVACO TCAD and SPICE mixed mode simulation (Fig. 6). Fig. 6(a) shows input pluses, node1 and output voltage according to transient time. When the input pulse is applied, the electron concentration in the floating body of the FBFET is increased by the electrons injected from source (Fig. 6(b)). So, the input pulses are integrated by the injected electrons that accumulated in the floating body of the FBFET. And leaky integration is implemented by electron recombination. If the number of electrons exceeds the threshold point, the hole concentration in the floating body below the gate1 increases abruptly, and the FBFET is turned on very rapidly. During the accumulation period, V_{node1} is maintained at V_{dd} because the I_{SC} is suppressed by the FBFET. The drain current flows only in short moments when the first inverter switching occurs (Fig. 6(c)). In conventional CMOS neuron circuit, during the membrane capacitor is charged, the I_{SC} continues to flow and most of the energy is consumed at this period (Fig. 6(d)). The conventional CMOS neuron circuit is described in previous works [23].

Measurement results of the neuron circuit are shown in Fig. 7. The input pulses are applied by Keithley and node1 and output voltage is observed by oscilloscope. Due to the super steep characteristics and low off-current of the FBFET, I_{SC} of the inverter are perfectly suppressed before the inverter

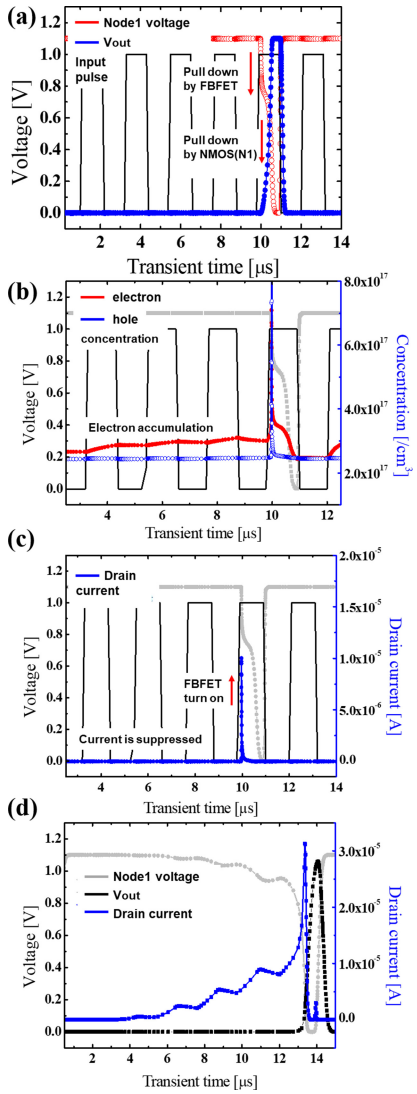

FIGURE 6. **Spice simulation results (a) each node bias, (b) charge concentration in the floating body (electron concentration in n-type body below the gate2, hole concentration is in p-type body below gate1), (c) drain current of FBFET, and (d) current of the 1st inverter in conventional CMOS neuron without FBFET.**

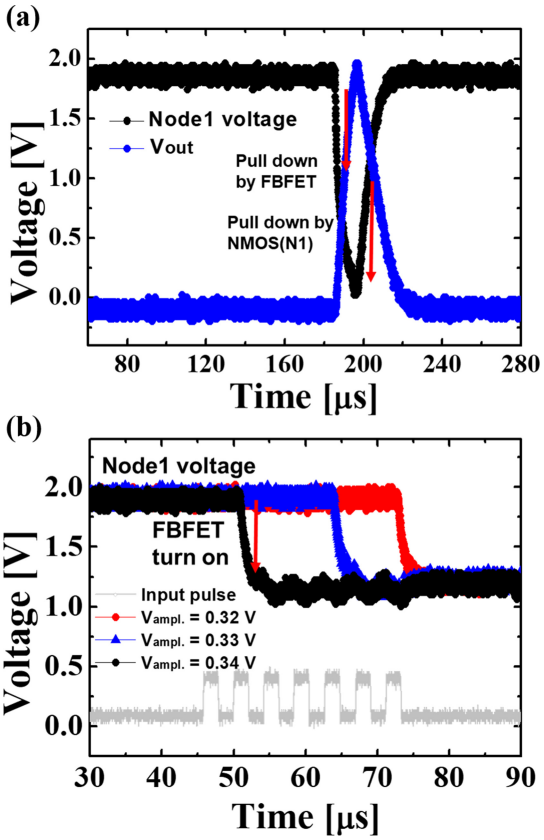

FIGURE 7. **(a) Measurement result of the capacitor-less neuron circuit with FBFET. After the FBFET initially turns on and pulls down the node1 abruptly, then continuously the N1 fully discharges node1 to the ground. (b) Measurement result of integration property. The number of pulses to turn on the FBFET depends on the amplitude of the input voltage.**

switching, and the node1 voltage drops rapidly due to the FBFET. However, the FBFET cannot simply replace the NMOS. The FBFET cannot pull down the node1 voltage to the ground because the FBFET shuts off rapidly as the drain voltage decreases before the node1 voltage is discharged to ground (Fig. 7(b)). To pull down the node1 to ground, we used second positive feedback loop circuit between inverter (INV2) and NMOS (N1). After the FBFET initially turns on and pulls down the node1 abruptly, the N1 is turned on by INV2 and fully discharges node1 to the ground as shown in Fig. 7 (a). Finally, the output spike is generated and accumulated charges in FBFET are removed by recombination. And during the accumulation period, V_{node1} is maintained V_{dd} since the I_{SC} is suppressed by the FBFET. Fig. 7 (b) show the measurement result according to the amplitude of the input pulse. When the amplitude of the input is low, the injected electrons are deceased and more pulses are required to turn on the FBFET. As the amplitude of the input is 0.32V, the FBFET is turned on after accumulating electrons for 7 pulses. Conversely, when a higher voltage pulse is applied, a large number of electrons are accumulated in the floating body during the only 2 pulses, causing the device to turn on and node1 voltage to drop. Therefore, the temporal integration is performed by the floating body effect and the FBFET can substitute the membrane capacitor effectively, reducing area and energy consumption.

V. CONCLUSION

In this work, we developed a capacitor-less I&F neuron circuit with FBFET that replace the membrane capacitor, resulting in reduced cell area and power consumption. And we successfully co-integrated FBFET and CMOS in a wafer using standard CMOS process. By incorporating FBFET to the neuron circuit, we can overcome the limits of conventional CMOS, suppress short-circuit current, and imitate integration property. And we demonstrate a method to utilize FBFET as a logic application.

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