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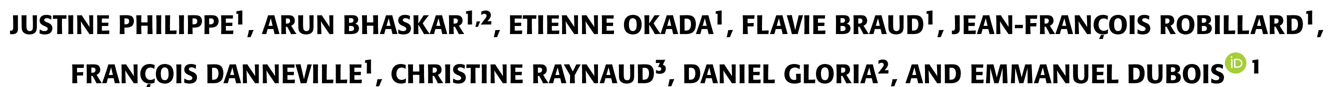
# Thermal Analysis of Ultimately-Thinned-and-Transfer-Bonded CMOS on Mechanically Flexible Foils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**ABSTRACT** Thinned CMOS chips transfer-bonded onto a compliant host substrate remain to date the technology of choice for applications requiring both mechanical flexibility and high frequency operation. However, the use of poorly thermally conductive host substrates raises the problem of thermal management of flexible electronics, a topic poorly addressed in literature. In this letter, we report the analysis of flexible SOI-CMOS chips ultimately-thinned-and-transfer-bonded (UTTB) onto polyimide and copper substrates. While the temperature remains limited to ∼68°C on the native silicon substrate or after transfer onto a copper host substrate, infrared thermography reveals temperature peaks of up to 118°C on polyimide. The impact of self-heating in flexible SOI-CMOS is correlated with electrical performance for the three types of substrates. Beyond the property of mechanical flexibility it provides, a copper substrate is shown to slightly strengthen electrostatic integrity while maintaining a thermal landscape close to that of silicon.

**INDEX TERMS** CMOS, SOI, thin film, flexible electronics, thermal management.

## I. INTRODUCTION

The field of flexible electronics has been the subject of considerable interest in recent years due to the prospects it offers for applications requiring mechanical flexibility, multiple form factors, weight and space savings [1]. While organic electronics has made remarkable progress, many challenges still persist, such as the low mobility of carriers, which make this technology inappropriate for high frequency applications [2]. On the other hand, flexible electronics based on an ultra-thin CMOS substrate has demonstrated great promise to meet application demands requiring high frequency, mechanical compliance and even optical transparency [3], [4], [5], [6], [7], [8]. Because silicon remains a brittle material, the transfer and bonding of the thinned chips onto a flexible host substrate is necessary to increase the toughness of the resulting bilayer system by stratification [9]. The choice of the host substrate is particularly important because it also determines the ability to dissipate heat. It is worth noting that plastic substrates have a relatively low thermal conductivity ($< 1$ W·m$^{-1}$·K$^{-1}$), especially compared with silicon (150 W·m$^{-1}$·K$^{-1}$). As a result, the transfer of thinned silicon chips on an organic substrate considerably increases the self-heating effect in MOS transistors. This effect, well known to affect carriers mobility and maximum drain saturation current in SOI-CMOS technology [10], [11], [12], [13], [14], is further exacerbated in transfer-bonded devices and circuits. Although, the influence of various plastic and metal-based host substrates on the radio-frequency (RF) performance on CMOS transistors has been covered in previous work [1], [4], the impact of thermal effects induced by the nature of the host substrate is poorly addressed in the literature [15], [16]. In this letter, we compare DC performance of transistors transferred on flexible copper (Cu) and polyimide (PI) substrates with those of the native CMOS technology. This is achieved with the objective to clarify

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the impact of self-induced thermal effects on markedly different host substrates, namely, metallic or plastic. For this comparison exercise, the choice of a Cu metal substrate is naturally justified by its very high thermal conductivity (400 $Wm^{-1}K^{-1}$), which is 2.7 times more than silicon as shown by the data compiled in Table 1. This characteristic of Cu is coupled with greater ductility, making it an interesting option of flexible substrate. The choice of copper was therefore guided by the objective of comparing the initial silicon substrate with a caricatural case where both thermal conductivity and mechanical flexibility are theoretically improved compared to silicon. Indium as a thin bonding layer (2 μm) is used here in an opportunistic way for its metallic character in order to minimize any thermal barrier. The other extreme caricatured situation is embodied by the use of a PI substrate with a relatively thick organic bonding layer extremely unfavorable to heat dissipation. Polyimide is here representative of many other organic films such as Polyethylene naphthalate (PEN), polydimethylsiloxane (PDMS), polymethyl methacrylate (PMMA), polycarbonate (PC). Although RF operation is not the subject of this study, the choice of either material can potentially be guided by a low dielectric loss requirement. In the following, the fabrication process is described in a first part. In Section III, thermal characterization will be presented through the implementation of two-dimensional thermography. Finally, Section IV discusses electrical performance and correlation with thermal characterization.

**TABLE 1. Bulk thermal parameters of transistor layers.**

| | Si handler | $SiO_2$ BOX | Cu substrate | In bond | PI substrate | Ordyl bond |
|---|---|---|---|---|---|---|
| Layer thickness (μm) | 800 | 0.145 | 250 | 2 | 50 | 17 |
| κ ($W.m^{-1}.K^{-1}$) | 150 | 1 | 400 | 82 | 0.12 | 0.2 |
| $R_{ths}$ ($K.m^2.W^{-1}$) × $10^{-6}$ | 5.33 | 0.4 | 0.625 | 0.024 | 417 | 85 |
| Ref. κ | [27] | [28] | [29][30] | [26] | [31] | [20] |

## II. FABRICATION PROCESS

The chip comprises RF-CMOS transistors fully processed on high-resistivity (HR) SOI wafers using a conventional route of 65nm partially-depleted PDSOI technology [17]. The post-processing principle is to use back-side etching techniques to completely eliminate the silicon (Si) handler down to the buried oxide (BOX) before transfer-bonding onto a bendable host substrate [1], [4]. For a comparison purpose, thinned chips are transferred onto markedly different flexible host substrates, namely, a 250 μm thick Cu foil and a 50 μm thick PI film, using an appropriate bonding technique (Fig. 1). Post-processing starts with chip singulation using pulsed laser ablation to prevent incipient fracture points that could cause breakage during the thinning steps. The front side of the chip is bonded onto a sapphire carrier using a temporary double-sided

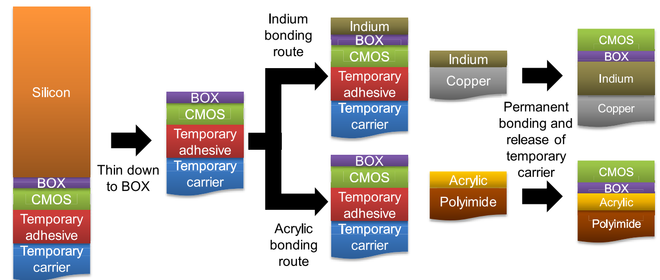


**FIGURE 1. Fabrication sequences of the ultimate-thinning-and-transfer-bonding (UTTB) process distinguishing integration routes on a metal (Cu) or a polymer (PI) host substrate.**

thermally releasable adhesive film (Revalpha 3195M from Nitto Denko). Grinding and chemical mechanical polishing are subsequently used to thin the 780-μm-thick silicon handler down to 30 μm. A selective dry etching based on xenon difluoride ($XeF_2$) is implemented to remove the remaining silicon layer using the BOX as a stop layer. It is important to note that silicon etching in $XeF_2$ gaseous phase is highly selective [18], [19] with respect to the silicon oxide of the BOX layer. This step results in an extremely flat and clean surface without alteration or cracking of the BOX as testified by scanning electron microcopy (SEM) and transmission electron microscopy (TEM) pictures on the same CMOS technology [1], [4], [8].

At this stage, the die is reduced to its ultimate thickness of about 7 μm that corresponds to the BOX and SOI layers topped by the interconnect network. For this reason, this process is referred to as ultimate-thinning-and-transfer-bonding (UTTB). The following step of this fabrication process is the transfer and bonding of the ultrathin chip onto a mechanically flexible host substrate. In the case of transfer on a Cu foil, a 1-μm-thick layer of indium (In) is vacuum deposited on both the chip back-side and the Cu foil before joining the two part in normal atmosphere using a roller lamination technique. The bonding is realized at a temperature of 100°C with a roller pressure of 4 $kg.cm^{-2}$ and a speed of 0.2 $m.min^{-1}$. Finally, the chip is released from the temporary adhesive layer through the application of a thermal budget of 120°C. In the case of transfer to a PI film, bonding is carried out by lamination of a 17 μm thick dry polymer film featuring a mixed acrylic/epoxy composition (Ordyl SY 317 from Elga) [20]. A lamination temperature of 120°C allows the bonding/release chain to be controlled in a single step using the same roller pressure and speed as above. The final result of the fabrication process is presented in Fig. 2(b) and 2(c) for the Cu and PI flexible substrates, respectively, while the original chip with its full 800 μm thick silicon handler is shown in Fig. 2(a).

The transfer-bonding of a thinned silicon chip on a host substrate is potentially subject to stress build-up resulting from the assembly of layers with dissimilar expansion coefficients, also known as thermal expansion mismatch. A simplified analysis can be performed by assuming a bilayer system where the upper layer represents a thinned all-silicon

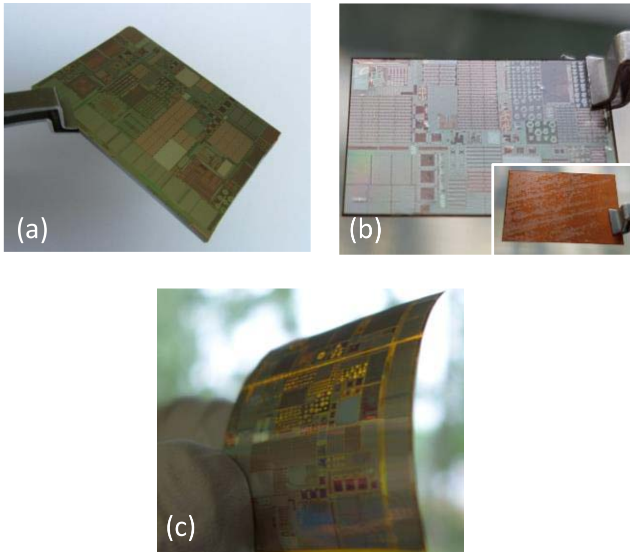


**FIGURE 2. Pictures showing (a) the original chip on its silicon substrate (Si), (b) after UTTB onto a 250 μm thick copper (Cu) foil with the back face in inset and (c) after UTTB onto a 50 μm thick polyimide (PI) film.**

chip and the lower layer, the host substrate. In this case, the strain required to fit the chip on the host substrate is expressed by [21]:

$$\varepsilon_{Sichip} = -(\alpha_{Sichip} - \alpha_{host}) \cdot \Delta T \quad (1)$$

where $\alpha_{\mathrm{Sichip}} = 2.6 \times 10^{-6}\ \mathrm{K}^{-1}$ [22] and $\alpha_{\mathrm{host}}$ are the linear thermal expansion coefficients of the thinned chip and host substrate, respectively. ΔT is the temperature difference describing the return to room temperature after bonding by roller lamination at 100°C. In the present case, ΔT∼-80K and is therefore negative. PI features a higher thermal expansion coefficient, typically $\alpha_{\mathrm{host}} \sim 30\times10^{-6}\mathrm{K}^{-1}$ [23]. It therefore ensues a negative strain $\epsilon_{\mathrm{Sichip}} \sim -2.19\times10^{-3}$ corresponding to a top silicon chip that shrinks less than the PI substrate, resulting in compressive stress in the chip and a tensile stress in PI. It is interesting to note that Fig. 2(c) shows a convex bowing after transfer-bonding of the thinned chip onto PI consistently with the above analysis. In reality, the rigorous mechanical analysis of UTTB chips is highly complex due to the variety of materials and the geometry of the interconnect layers in the silicon chip. Lecavelier des Etangs-Levallois *et al.* [1], [23] proposed a comprehensive modeling of the thickness-dependent strain and stress distributions when transfer-bonding is performed on a 50 μm thick PI host substrate, as it is the case in the present paper. It was shown that both the longitudinal and transversal components of the Cauchy stress tensor remain below 40 MPa, well below the fracture strength of silicon of 120 MPa [24]. Complementarily, the transfer of a thinned silicon chip onto the copper substrate mediated by an indium layer deserves special analysis because this case is supposed to represent the caricatured situation where heat dissipation is best, as explained in the introduction. It is important to note that the bonding of surfaces intended to facilitate heat flow removal is generally carried out by a thermal interface material (TIM). The first function of TIM is to fill microscale voids and grooves between mating surfaces. To this end, a sufficiently thick bondline is expected to play the role of gap filler, thus requiring a low bulk thermal resistivity for the TIM [25]. The second equally important function of the TIM is to absorb strain resulting from the mismatch of thermal expansion (CTE) between the circuit die and the host substrate. In that respect, indium exhibits outstanding attributes with a high thermal conductivity of 82 $\mathrm{W{\cdot}m^{-1}{\cdot}K^{-1}}$, low tensile and shear strengths of 1.9 MPa and 6.1 MPa, respectively, which makes it a material prone to absorb deformation resulting from thermal mismatch [26].

## III. THERMAL ANALYSIS

The first step of analysis focuses on the thermal behavior according to the nature of the host substrate. The analyzed device is an n-type MOSFETs transistor featuring a 60 nm gate length and a total width of 64 μm obtained from the parallel association of 128 gate fingers with a 0.5 μm unitary width. Temperature measurements are performed by infrared thermography using a camera with a lateral resolution of 3 μm. Measured samples are placed on a 45°C thermostatically-controlled chuck that facilitates the calibration of surface emissivity. In order to determine how electrical operation is affected by thermal behavior, transistors are biased identically at $V_{GS} = 0.7$ V and $V_{DS} = 1.5$ V regardless of the host substrate. From a methodological standpoint, the thermographic maps were recorded after a hold time during which the static electrical bias of the transistor was maintained and the current measured until complete stabilization, thus ensuring that the thermal steady-state regime was established. Under these conditions, the essence of the thermal problem can be captured by the time-independent Fourier equation and a lumped element modeling approach can be adopted with one thermal resistance associated to each material layer or interface. Fig. 3(a), 3(b) and 3(c) provides the 2D temperature distributions of the considered transistor on its original silicon handler and after transfer onto the Cu and PI film, respectively. To evaluate the ability of each substrate to dissipate heat, Table 1 summarizes parameters governing the thermal behavior in steady-state regime, namely, the material intrinsic thermal conductivity $\kappa$ ($\mathrm{W{\cdot}m^{-1}{\cdot}K^{-1}}$) as well as the insulance $R_{ths} = t/\kappa$ ($\mathrm{K{\cdot}m^2{\cdot}W^{-1}}$) that reflects the unit area thermal resistance for a layer of thickness t. The total series insulance can therefore be evaluated by adding the contribution of each layer. Taking into account the stacking of layers, the insulance of each configuration gives $5.7\times10^{-6}$, $1.1\times10^{-6}$ and $502\times10^{-6}\ \mathrm{K{\cdot}m^2{\cdot}W^{-1}}$ for the original silicon substrate, the Cu and PI host substrates, respectively. Not surprisingly, a significant temperature increase can be observed for the transistor transferred onto the PI sheet as expected from the high insulance theoretically evaluated hereinbefore.

In Fig. 4, this observation is confirmed by the one-dimensional horizontal (A-A') and vertical (B-B') profiles

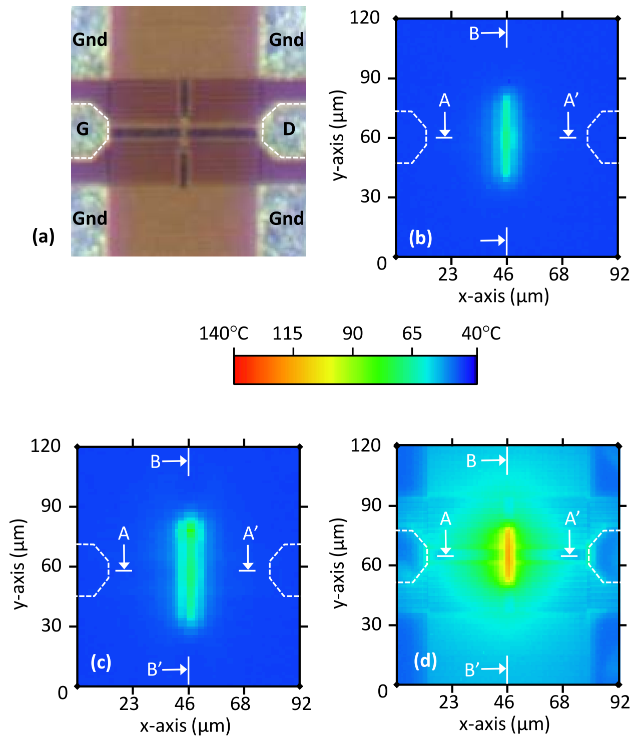


**FIGURE 3.** (a) Optical microscopy image of the measured RF n-MOS transistor showing the gate (G) and drain (D) coplanar access pads. Infrared thermography temperature maps of: (b) the original chip on its silicon substrate (Si), (c) after UTTB onto a 250 $\mu$m thick copper (Cu) foil and (d) after UTTB onto a 50 $\mu$m thick polyimide (PI) film. The n-MOSFET is biased at $V_{GS} = 0.7$ V and $V_{DS} = 1.5$ V for the three flavors of substrates. The dotted line delineates the central contact of the gate and drain coplanar accesses.

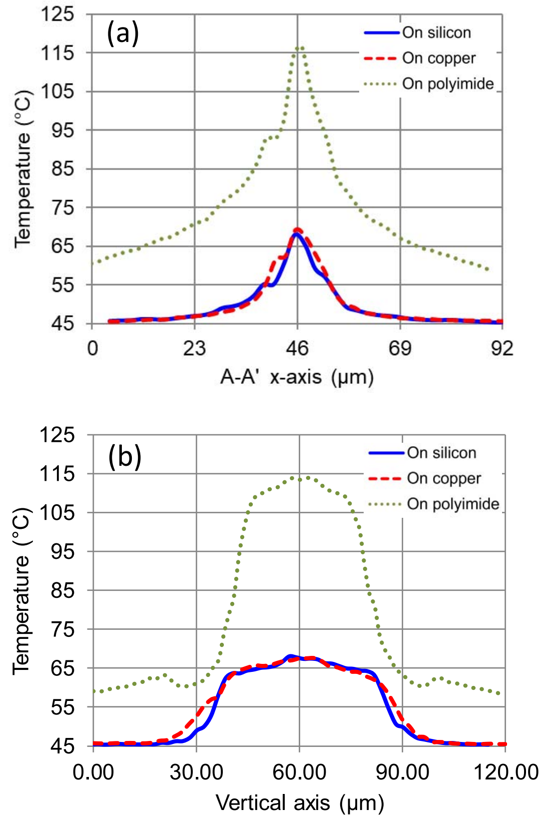


**FIGURE 4.** One-dimensional temperature profiles along horizontal (A-A') and vertical (B-B') directions corresponding to the thermal imaging maps shown in Fig. 3. The temperature profiles of the three flavors of substrates Si, Cu and PI are displayed for the same n-MOSFET biased at $V_{GS} = 0.7$ V and $V_{DS} = 1.5$ V.

crossing the transistor center for each of the host substrate configurations. The peak temperature along the vertical (B-B') profile corresponding to the longitudinal dimension along the MOSFET channel length amounts to 68, 67.7 and 114°C for the Si, Cu and PI substrates, respectively. Consistently, the peak temperature along the horizontal (A-A') profile corresponding to the transversal dimension along the MOSFET channel width reaches 67.8, 69.2 and 116.7°C for the three types of substrates in the same order as above. Fig. 3 and 4 also demonstrate that transistors on the original Si handler and after transfer bonding on Cu exhibit similar thermal behavior. Although the stack with the copper host substrate theoretically holds the lowest total insulance, the transistor on its native Si handler nevertheless demonstrates a slight advantage in terms of thermal dissipation.

This observation can be explained by the lack of consideration of the Kapitza interfacial resistance in the first order analysis developed hereinbefore. For the insertion of a TIM layer consisting of indium between oxidized silicon and copper substrates, the literature reports interface thermal resistance values varying in the range $5\times10^{-6}$-$2\times10^{-5}$ $K{\cdot}m^2{\cdot}W^{-1}$ depending on the assembly pressure applied to the stack [26]. In contrast, the Kapitza resistance of the $Si/SiO_2$ interface is considerably lower with a value of $2.3\times10^{-9}$ $K{\cdot}m^2{\cdot}W^{-1}$ which is considered as an upper limit that integrates all sources of uncertainties [32], [33]. By now including in the thermal analysis, the effect of the Kapitza resistance associated with the bottom bonding interface for the three types of substrates, the following conclusions can be drawn: i) the interface thermal resistance of the $Si/SiO_2$ interface is negligible when compared with the insulance of the various layers summarized in Table 1, ii) the total insulance of the system transferred onto a Cu host substrate is increased by typically $10^{-5}$ $K{\cdot}m^2{\cdot}W^{-1}$ which is representative of the Kapitza resistance associated to the indium TIM inserted between $SiO_2$ and Cu [26], iii) given the high thermal resistance of organic layers reported in Table 1, the total insulance of the system transferred on the PI film is more likely to be governed by the bulk thermal conductivity than the interface one. Summarizing the considerations outlined above, the total insulance corresponding to the Cu host substrate can be re-evaluated at $11\times10^{-6}$ $K{\cdot}m^2{\cdot}W^{-1}$, making the native silicon handler a slightly more efficient substrate for heat dissipation as experimentally observed in Fig. 3 and 4.

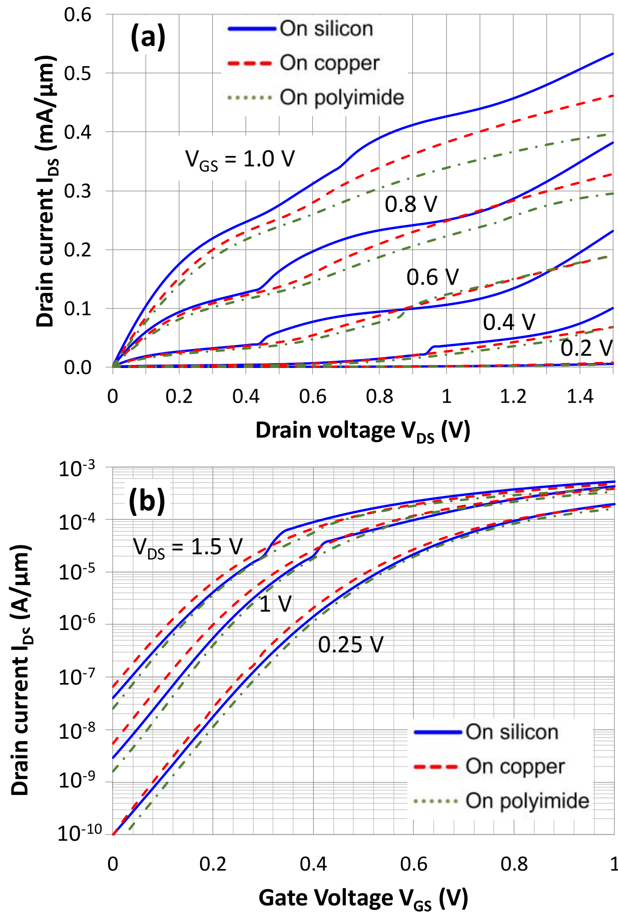


**FIGURE 5.** n-MOSFET current-voltage characteristics for the original chip on its silicon substrate (Si), after UTTB onto a 250 µm thick copper (Cu) foil and after UTTB onto a 50 µm thick polyimide (PI) film: (a) $I_{DS}$-$V_{DS}$ characteristics for $V_{GS}$ varied from 0.2 to 1 V in 0.2 V steps (b) $I_{DS}$-$V_{GS}$ characteristics for $V_{DS} = 0.25$, 1 and 1.5 V.

## IV. ELECTRICAL CHARACTERIZATION

Thermal dissipation in both DC and high-frequency small-signal operation is essentially governed by the quiescent bias state of the transistor. The impact of the host substrate on the DC performance is shown in Fig. 5 for n-MOSFETs thermally characterized in the previous section. The obvious observation is the significant attenuation of the kink effect for the transistor bonded on the PI film. The reduced kink effect is also observed to a lesser degree on the Cu host substrate. This phenomenon can be explained by the enhanced self-heating and the well-established reduction, at higher temperature, of impact ionization that governs the kink effect [34], [35]. In Table 2, six indicators have been selected to clearly identify the impact of each substrate on the overall static performance of the considered PDSOI technology.

The main effect introduced by host substrates is the decrease of the maximum saturation drain current ($I_{ON}$) which is ascribed to mobility reduction with the slightly higher temperature measured on Cu and more significantly on PI. It is worth noting that the Cu host substrate behaves like a metal back gate that reinforces the electrostatic control through the BOX. It visibly improves the subthreshold swing (SS) and decreases the threshold voltage ($V_{TH}$) by ~20 mV when compared to the Si case. Little variations of the off-state current ($I_{OFF}$) is obtained and explained by the $V_{TH}$ shifts. Overall, the electrostatic integrity of the transistor is preserved and the main effect of UTTB on Cu and PI is limited to a reduced current drive resulting from self-heating.

**TABLE 2.** Static parameters of n-MOSFETs on their initial rigid silicon (Si) substrate and after transfer onto a Cu and PI flexible film.

| MOSFET DC parameters | on native Si | on Cu | on PI |
|---|---|---|---|
| $I_{ON}\|_{V_{GS}=1V,V_{DS}=1.5V}$ (µA.µm$^{-1}$) | 534 | 462 | 397 |
| $I_{OFF}\|_{V_{GS}=0V,V_{DS}=1.5V}$ (nA.µm$^{-1}$) | 40.4 | 69.1 | 25.2 |
| $I_{ON}/I_{OFF}$ ($\times 10^4$) | 1.32 | 0.67 | 1.57 |
| $V_{TH}$ (mV) | 405 | 384 | 417 |
| DIBL (mV) | 254 | 255 | 259 |
| SS (mV/dec) | 89 | 82 | 85 |

## V. CONCLUSION

In this letter, we have analyzed the self-heating effect resulting from ultimate-thinning-and-transfer-bonding of SOI-MOS transistors onto low and high thermal conductivity substrates like PI and Cu, respectively. Measured thermal maps confirm the high temperature rise for PI that results in a current decrease and mitigation of the kink effect. Interestingly, a Cu host substrate experiences a smaller current reduction than the PI substrate and generates a beneficial effect in strengthening electrostatic integrity. It is therefore an excellent substrate for enhancing MOS technologies with additional properties of mechanical flexibility while preserving high frequency operation as previously shown in [1], [4], [7], [8], [36]. In addition, this work demonstrates that UTTB performed on a thin Cu substrate is effective in maintaining heat dissipation at a level very close to that of the native thick silicon substrate despite the introduction of Kaptiza resistances associated to the $Si/SiO_2/In/Cu$ interfaces substantially higher than that of the native $Si/SiO_2/Si$ interfaces.

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