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Comprehensive Study of Stacked Nanosheet-Type Channel Based on Junctionless Gate-All-Around Thin-Film Transistors

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ABSTRACT As technology develops, the stacked nanosheet (NS) structure demonstrates promise for use in future technology nodes. This study demonstrated the excellent performance of stacked-NS channels with junctionless gate-all-around thin-film transistors and compared the electrical characteristics of single-NS and stacked-NS structures. The performance of the multi-gate and gate-all-around transistors was then further analyzed. The stacked gate-all-around thin-film transistor exhibited superior performance and excellent temperature design flexibility. In brief, the stacked gate-all-around structure for thin-film transistors structure has the potential to overcome the challenges associated with downscaling.

INDEX TERMS Gate-all-around (GAA), junctionless (JL), nanosheet (NS), stacked structure, thin-film transistor (TFT).

I. INTRODUCTION

Stacked nanosheet (NS) devices have been proposed with the aim of improving device performance and serving as a substitute for fin structure devices in future technology nodes [1]–[8]. The NS channel structure is preferable in terms of 1) effective channel width, 2) process simplicity, and 3) design flexibility [1]–[3]. Additionally, the junctionless thin-film transistor (JL-TFT) has the advantages of low thermal budget, long effective channel length, and a simple source and drain engineering [9]–[11]. Accordingly, this study compared the electrical characteristics of the single-NS and stacked-NS JL structures and subsequently investigated the electrical behavior of the stacked-NS JL channel with multi-gate and gate-all-around (GAA) TFTs. This study proposes that stacked-NS channels for JL GAA TFTs are a promising structure in future technology nodes.

II. EXPERIMENTAL DETAILS

The proposed stacked-NS structures were fabricated by first growing a 400-nm-thick SiO_2 layer with a 50-nm-thick undoped amorphous Si (a-Si) layer which was deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C. Subsequently, a poly-Si layer was formed through the solid-phase crystallization (SPC) method at 600°C for 24 hrs in a nitrogen ambient atmosphere to serve as the bottom channel. The poly-Si layer was then implanted with BF_2 ions at a dose of 2×10^{14} cm^{-2} by 30 keV and activated through furnace annealing at 600°C for 4 hrs. Thermal oxide with 30 nm thickness was grown to separate the two stacked channels and thin down the thickness of the bottom channel. It is worth mentioning that the thickness of oxide interlayer is designed according to the trimmed thickness of the bottom channel. The 50-nm-thick poly-Si layer was deposited through SPC method as top channel, and then was implanted with BF_2 ions at a dose of 2×10^{14} cm^{-2} by 30 keV and activated through furnace annealing at 600°C for 4 hrs. Then, oxidation trimming was applied to thin down the thickness of the top channel. The NS structure was patterned through e-beam lithography (EBL) and transferred through reactive-ion etching (RIE). To form the GAA structure, the device was dipped in a buffered oxide etch (BOE) solution for suspending the NSs. Next, the thermal oxide (SiO_2) with 10 nm thickness and *in situ* doped n^+ poly-Si with 200 nm thickness were grown to serve as the gate oxide and gate,

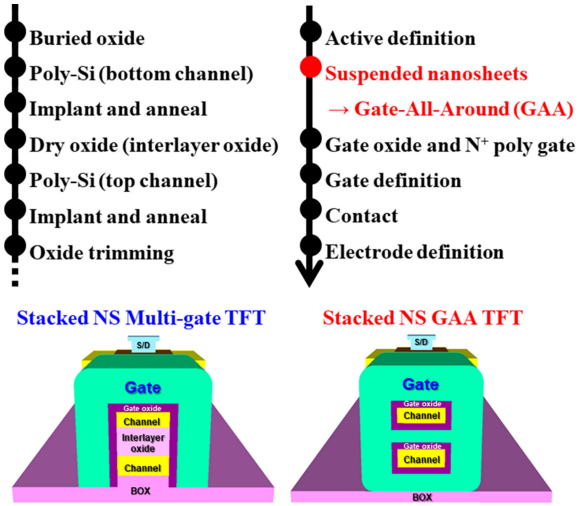

FIGURE 1. Process flow and channel cross-section of stacked nanosheets multi-gate and gate-all-around thin-film transistors.

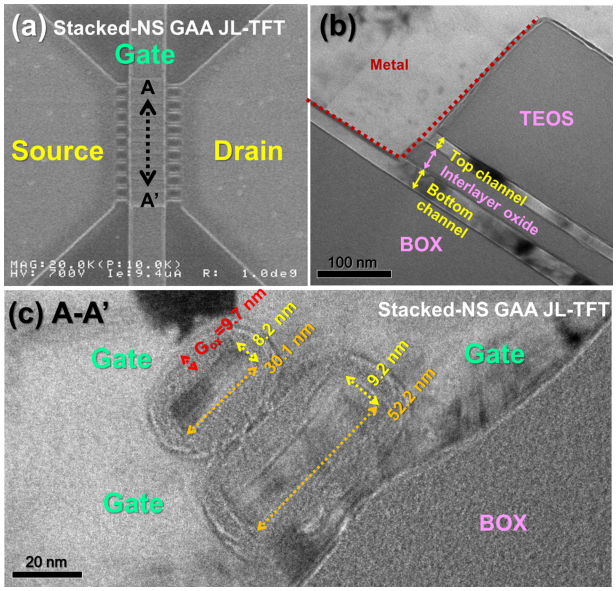

FIGURE 2. Top-view SEM images of the (a) stacked-NS GAA JL-TFT with ten nanosheets. TEM images for the (b) contact region and (c) cross-section of the stacked-NS GAA JL-TFT along the gate direction (A–A').

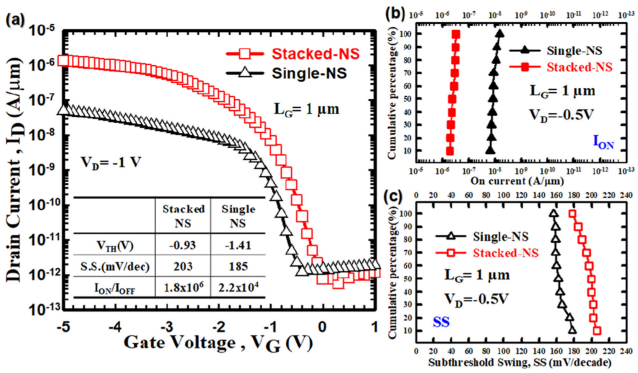

FIGURE 3. (a) Normalized I_D–V_G curves of the single-NS and stacked-NS JL devices. (b-c) Cumulative distribution of I_{on} and SS.

respectively. After growing the gate oxide, the top and bottom channels were thinned down again. Therefore, the final thickness of the top and bottom channels were around 8.2 nm and 9.2 nm, respectively (Fig. 2 [c]). Next, the gate electrode was patterned through EBL and RIE. The tetraethoxysilane with 200 nm thickness was deposited as a passivation layer. Finally, Al–Si–Cu with 300 nm thickness was served as the electrode and connected to the top and bottom channels (Fig. 2 [b]).

III. RESULTS AND DISCUSSION

The 3D stacked-NS channels structure has been proposed as a potential candidate for future technology nodes. Therefore, this work presents the stacked-NS channels GAA JL-TFT. In Fig. 2 (a), the top-view scanning electron microscopy images of the stacked-NS GAA JL-TFT with gate length of 1 μm. Fig. 2 (b) presents the transmission electron microscopy (TEM) image of the source/drain contact region. Fig. 2 (c) presents the TEM image of a nanosheet of the stacked-NS GAA JL-TFT with a height of 8.2 nm and width of 30.1 nm for the top channel. The bottom channel had a height of 9.2 nm and a width of 52.2 nm. The gate oxide thickness of the stacked-NS GAA JL-TFTs was approximately 9.7 nm. For comparing with the stacked-NS GAA JL-TFT, the stacked-NS multi-gate JL-TFT was also fabricated with a width of 39.5 nm for the top channel and a width of 65.6 nm for the bottom channel.

A. SINGLE AND STACKED NANOSHEETS CHANNEL TFT

This work compared single-NS and stacked-NS based on JL devices (presented in Fig. 3) at first. Fig. 3 (a) displays the normalized I_D–V_G curves of single-NS and stacked-NS JL-TFTs with a multi-gate structure. These I_D–V_G curves were normalized by total top width of each device. Each nanosheet top width of the single-NS and stacked-NS devices were around 110 nm and 100 nm, respectively. The subthreshold slopes (SS) of the single-NS and stacked-NS devices were 185 mV/dec and 203 mV/dec, respectively. Notably, the stacked-NS device had superior on-current because of its double-stacked structure. Fig. 3 (b-c) displays the cumulative distribution of the on-current and SS, respectively. The results were obtained from 20 devices operating under the same conditions. As a result, the stacked-NS structure could effectively increase the on-current that remedy for the problem of low on-current due to impurity scattering.

B. STACKED NANOSHEETS MULTI-GATE AND GAA TFT

To improve the performance of the stacked-NS structure comprehensively, this study further presents stacked-NS devices with a GAA structure. Fig. 4 (a) plots the I_D–V_G curves of the stacked-NS GAA JL-TFTs and stacked-NS multi-gate JL-TFTs at V_D of −0.5 and −3 V. The SS

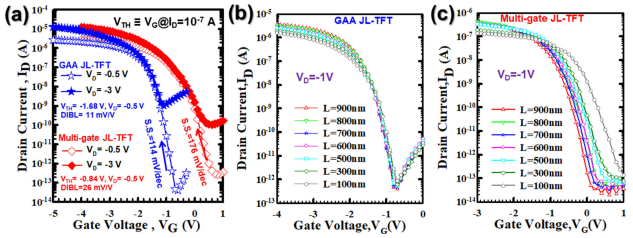

FIGURE 4. (a) Comparison of I_D–V_G curves at $V_D = -0.5$ V and $V_D = -3$ V. L_G comparison of I_D–V_G curves at $V_D = -1$ V of (b) the stacked-NS GAA JL-TFTs and (c) the stacked-NS multi-gate JL-TFTs.

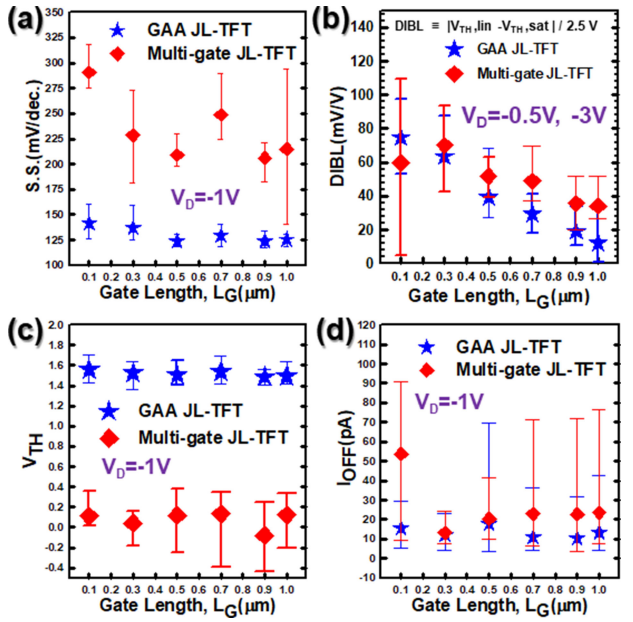

FIGURE 5. L_G comparison of *SS*, DIBL, V_{TH}, and I_{OFF} various plots of the stacked-NS GAA JL-TFTs and stacked-NS multi-gate JL-TFTs.

of the stacked-NS GAA JL-TFTs and stacked-NS multi-gate JL-TFTs were 114 mV/dec and 176 mV/dec at V_D of −0.5 V, respectively. Drain-induced barrier lowering (DIBL) in the stacked-NS GAA JL-TFTs (11 mVV^{-1}) was superior to that in the stacked-NS multi-gate devices (26 mVV^{-1}). Fig. 4 (b-c) presents the I_D–V_G characteristics with different gate lengths of the stacked-NS GAA JL-TFTs and stacked-NS multi-gate JL-TFTs. The SS of the stacked-NS GAA JL-TFTs and stacked-NS multi-gate JL-TFTs on gate length from 0.9 to 0.1 μm were 119 mV/dec, 119 mV/dec, 120 mV/dec, 121 mV/dec, 125 mV/dec, 126 mV/dec, 126 mV/dec, and 171 mV/dec, 175 mV/dec, 178 mV/dec, 179 mV/dec, 188 mV/dec, 206 mV/dec, 207mV/dec, respectively. These could be used to investigate further the effects of the downscaling gate length. Fig. 4 reveals that the stacked-NS GAA JL-TFTs exhibited less variation when the gate length was scaled down; this was a result of their excellent gate control ability.

Moreover, the *SS*, DIBL, V_{TH}, and I_{OFF} for different gate lengths were also considered. The mean and variance in Fig. 5 (a-d) were obtained from the results of 20 devices.

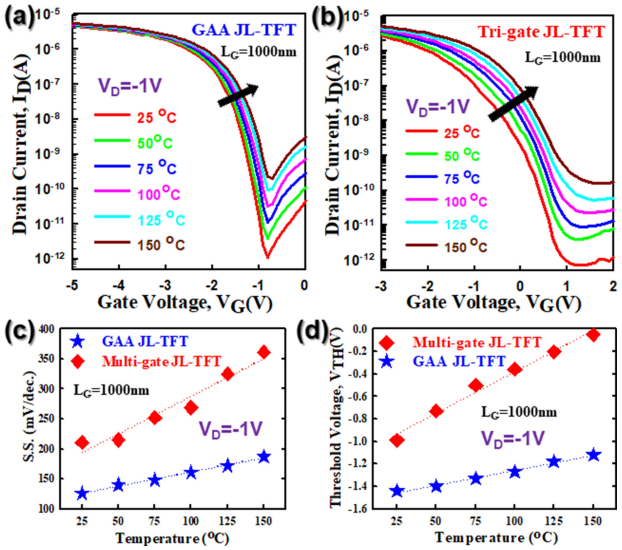

FIGURE 6. Effect of temperature variation on (a-b) I_D–V_G curves and (c-d) SS and V_{TH} values of the stacked-NS GAA JL-TFTs and stacked-NS multi-gate JL-TFTs.

The results presented in Fig. 5 demonstrate that the stacked-NS GAA JL-TFTs had small mean and variance because of their excellent gate control ability. Fig. 6 (a-b) demonstrates the effect of temperature variation on the I_D–V_G curves of the stacked-NS GAA JL-TFTs and stacked-NS multi-gate JL-TFTs. Fig. 6 (c-d) plots the temperature dependence of SS and V_{TH} of both stacked-NS JL devices. The stacked-NS GAA JL-TFTs were less sensitive to temperature. The temperature coefficients for S.S. and V_{TH} of the stacked-NS GAA JL-TFTs and the stacked-NS multi-gate JL-TFT are around 0.472 mV/dec. and 2.56 mV per degree C and 1.25 mV/dec. and 7.44 mV per degree C, respectively. In brief, the GAA structure has the potential to overcome challenges of scale and presents exceptional thermal design flexibility.

IV. CONCLUSION

These stacked-NS channels in GAA JL-TFTs demonstrated the simplicity of the process and high performance. The stacked-NS GAA JL-TFTs exhibited less variation with gate length and temperature. Overall, stacked-NS JL-TFTs have potential for use in 3D stacked integrated-circuit applications in future technology nodes.

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