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Investigation of TSV Liner Interface With Multiwell Structured TSV to Suppress Noise Propagation in Mixed-Signal 3D-IC

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ABSTRACT Mixed-signal 3D-ICs have a stacked structure of digital and analog circuit chips. In this study, the effect of noise propagation from a digital circuit on an analog circuit was evaluated using an actual mixed-signal 3D-IC. The noise propagation via through-silicon vias (TSVs) was measured, with a ring-oscillator as a noise source. For a comprehensive investigation, TSV-liner interface states were evaluated along the depth direction using unique multiwell-structured TSVs and a charge-pumping method. It was considered that the interface traps and nonconformal thickness of the TSV liner increased the noise propagation among stacked chips.

INDEX TERMS 3D IC, through-silicon vias, charge pumping method, interface trap.

I. INTRODUCTION

Three-dimensional integrated circuits (3D-IC) have received significant attention because they have the potential to improve IC performances beyond those offered by the scaling of transistors [1]. 3D-ICs consist of several vertically stacked chips, electrically connected by through-Si vias (TSVs) and metal microbumps; they have been developed for several applications, such as memory storage and processors [2]–[5]. RF applications, which consist of mixed-signal ICs, are a class of applications that benefit greatly from 3D integration [6]–[8]. This is because noise propagation can be effectively suppressed by the 3D integration technique, because of the complete isolation between the analog and digital circuits in mixed-signal 3D-ICs [9]–[10]. To demonstrate the benefit of 3D integration for mixed-signal applications, we must evaluate the noise issues due to the one-chip integration of a noisy digital circuit along with the sensitive analog circuit. For example, we may have to consider the effect of the interface trap generated by Cu diffusion from TSVs [11]. This trap can cause noise propagation from the digital circuit to the analog circuit in the mixed-signal 3D-IC.

In this study, we fabricated a mixed-signal 3D-IC and evaluated the noise propagation. Then, we evaluated the state of the interface between the Si substrate and the TSV liner by measuring the charge-pumping current. For this purpose, we proposed the multiwell-structured TSV, which can evaluate the depth-direction-dependent interface state.

II. NOISE PROPAGATION IN MIXED-SIGNAL 3D-IC

A. FABRICATION

We fabricated a mixed-signal 3D-IC integrated with Cu-TSVs, as shown in Fig. 1. This mixed-signal 3D-IC consists of an analog circuit chip and a digital circuit chip. Each chip was fabricated by the standard 180-nm CMOS process. Fig. 2 shows the circuit diagrams of the low-noise amplifiers (LNA) and the ring-oscillator (RO) in the analog and digital circuit chip, respectively, that were used in this study. The LNA consists of instrumentation amplifier (IA) and programmable amplifier (PGA) circuits. All the circuits were fabricated by the triple-well-structure process; in addition, a guard ring surrounded the LNA. The gain and cut-off frequencies were 20 dB and 200 Hz, respectively. On the

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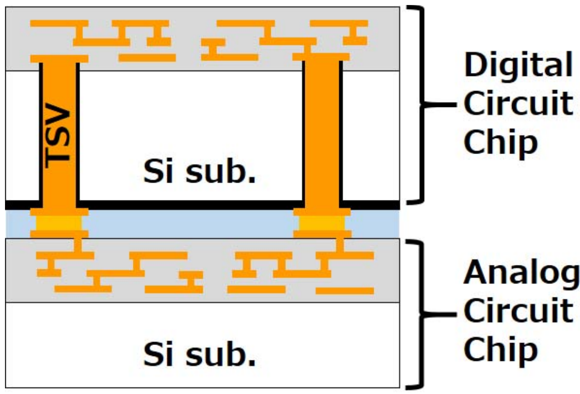

FIGURE 1. Cross-sectional schematic image of the fabricated mixed-signal 3D-IC.

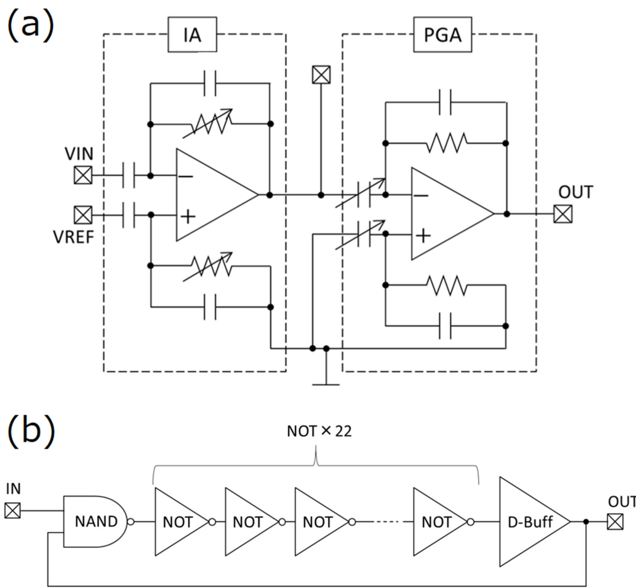

FIGURE 2. Circuit diagram of (a) LNA in an analog circuit chip and (b) RO in a digital circuit chip.

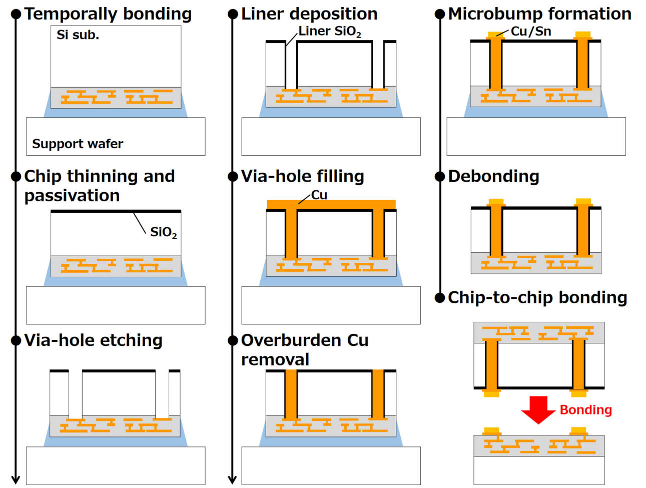

FIGURE 3. Process flow of the mixed-signal 3D-IC with via-last/backside-via TSV process.

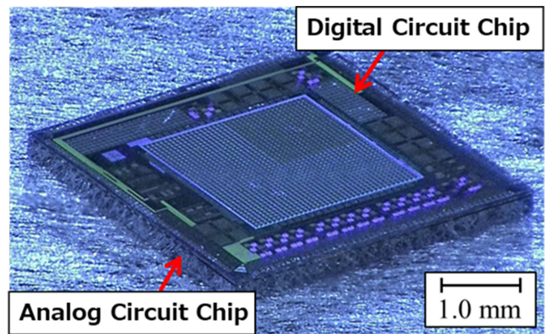

FIGURE 4. Photograph of the mixed-signal 3D-IC fabricated by via-last/backside-via TSV process.

other hand, the digital circuit chip had a 23-stage RO as the digital noise source. The oscillation frequency of the RO was 228 MHz.

The mixed-signal 3D-IC was fabricated with the via-last/back-side Cu-TSV process, as shown in Fig. 3. First, a digital circuit chip was bonded on a support wafer using a temporary adhesive. Then, the chip was thinned by mechanical grinding and chemical mechanical polishing (CMP). After the passivation process, via-holes were formed to contact the wiring layer of the digital circuit chip. Following this, the SiO_2 liner was deposited by plasma-enhanced chemical vapor deposition (PE-CVD). Here, the deposition gases and temperature were O_2, TEOS, and 200 °C, respectively. After the Ti barrier and Cu seed layer deposition, the via-holes were filled with Cu with electroless and electrolytic plating. The overburdened Cu was removed by CMP. Then, the redistribution layer and Cu/Sn metal microbumps were formed. Cu/Sn metal microbumps were also formed on the analog circuit chip. Finally, the digital circuit chip was bonded on the analog circuit chip and underfill was injected between the bonded digital and analog circuit chips. Fig. 4 is a photograph of the fabricated mixed-signal 3D-IC. The top chip consisted of digital circuits including the RO, and the bottom chip consisted of analog circuits including the LNA.

B. MEASUREMENT RESULTS AND DISCUSSION

First, the ring oscillator was operated at 228 MHz in the top digital circuit chip. Then, the LNA fabricated in the bottom analog circuit chip was measured. Fig. 5 shows the fast Fourier transformation (FFT) results of the measurements of the LNA with the ring oscillator operation in the top chip. The LNA input signal was a sine wave which had a frequency and amplitude of 1-kHz and 10-mV, respectively. We also measured the LNA in 2D-IC and 3D-IC, with and without RO operation, respectively, as shown in Fig. 5. We observed a strong signal in the vicinity of 225 and 228 MHz during the RO operation. In these measurements, we impressed the digital and the analog circuits with the isolated power-supply voltages (1.8 V) and the ground. Therefore, it is assumed that the strong signals are induced by RO operation and propagated through the substrate. There was a slight delay

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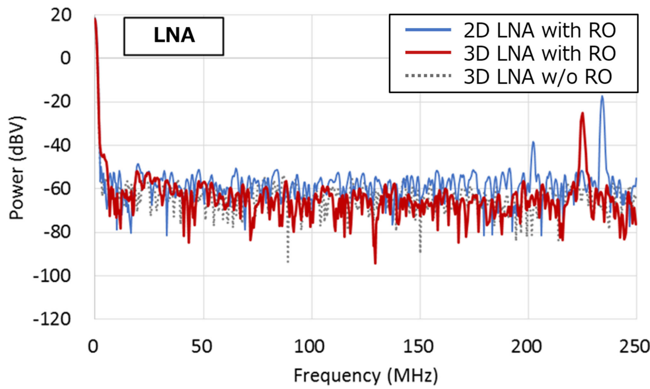

FIGURE 5. FFT results of the measured output of the LNA in mixed-signal 3D-IC with 228-MHz ring oscillator operation in the digital circuit.

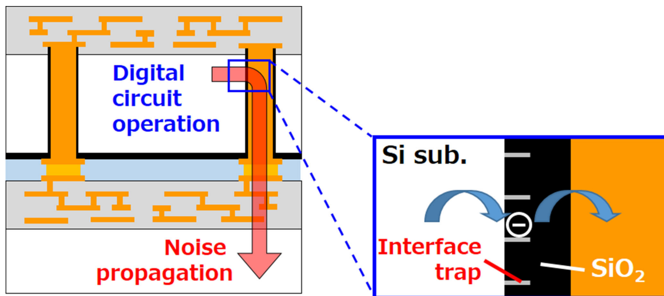

FIGURE 6. Schematic image of noise propagation through TSVs and Si substrate due to TSV-liner interface trap.

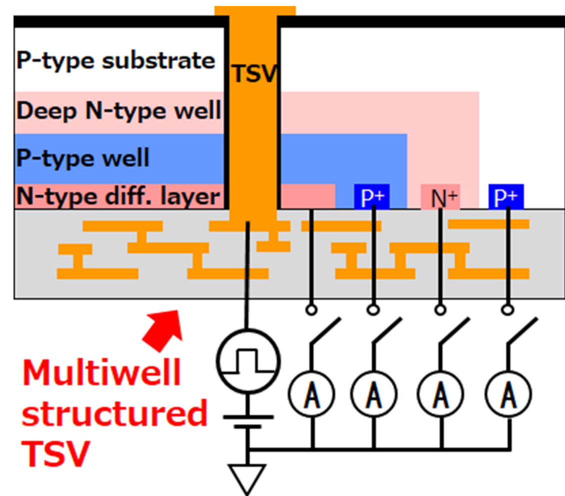

FIGURE 7. Cross-sectional image of TSV with multiwell structure and measurement setup of charge-pumping currents to evaluate the dependence of TSV liner interface on depth direction.

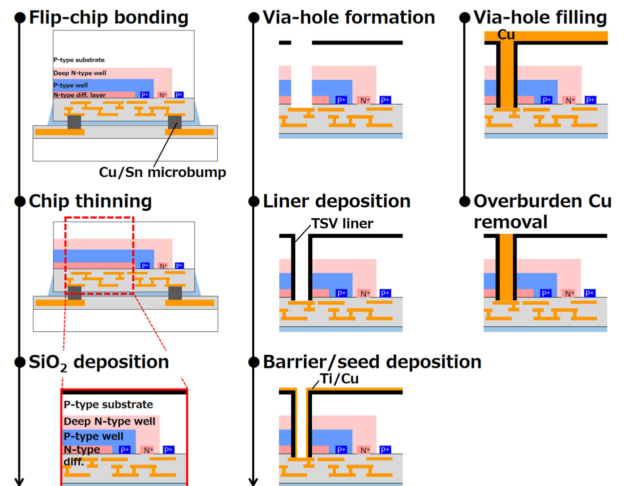

FIGURE 8. Process flow of the mixed-signal 3D-IC with via-last/backside-via TSV process.

between the RO-induced digital noises in the 2D- and 3D-ICs, induced by the parasitic resistance and capacitance in the noise path, such as the Si-substrate and the TSV liner. We observed that the RO-induced digital noise is suppressed by the 3D-stacked structure. However, these results indicate that it is difficult to fully remove the noise induced by the digital circuit operation in the mixed-signal 3D-IC with the TSV liner deposited by PE-CVD. These noise propagations are induced by high trap density and large parasitic capacitance that depend on the state of the TSV liner, as shown in Fig. 6. Therefore, we have to evaluate the interface state of the TSV liner to further suppress the effect of the noise propagation.

III. EVALUATION OF THE LINER INTERFACE WITH MULTIWELL-STRUCTURED TSV

Recently, several studies have been conducted on the properties of the TSV liner using various methods, such as *C-t* measurements and charge-pumping current measurements [12]–[13]. A characteristic variation of the TSV liner can be observed along the depth direction; however, there has been no prior attempt to evaluate the dependence of the interface state on the depth direction. In a previous study, we proposed a multiwell-structured TSV to characterize the dependence of the TSV-liner interface on the depth direction, as shown in Fig. 7. Reference [14]. In this study, for the first time, we have successfully quantitatively confirmed the dependence of interface trap density on the depth direction using multiwell-structured TSV. The test sample consists of TSVs and the multiwell, made of the N-type diffusion layer, P-type well, and deep N-type well. As shown in Fig. 7, by connecting an ammeter to each well, we can measure the charge-pumping current, which can assess the interface state of the TSV liner at each depth. We can evaluate the dependence of the interface characteristics of the liner on the depth direction with charge-pumping current measured by multiwell-structured TSVs.

A. FABRICATION

Fig. 8 shows the process flow of multiwell-structured TSVs. In this test structure, the TSVs were formed in the IC chip with the multiwall structure. Fig. 9 shows a cross-sectional scanning capacitance microscopy (SCM) image of the fabricated IC chip with the multiwall structure to evaluate the interface of the liner; it can also be seen here that the IC chip

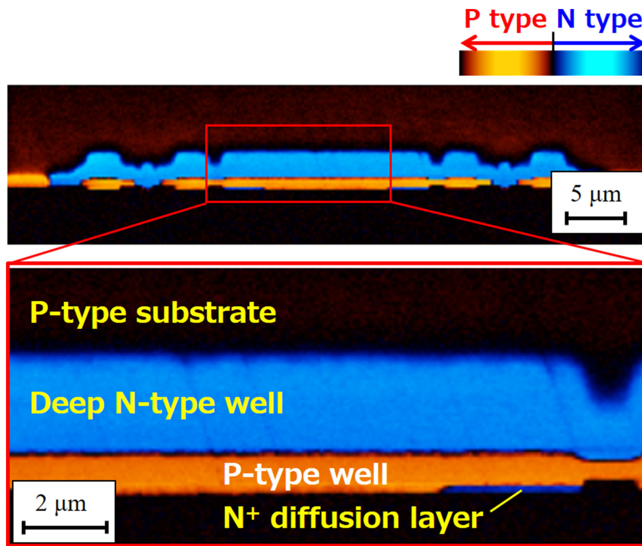

FIGURE 9. Cross-sectional scanning capacitance microscopy (SCM) image of the multiwell structure.

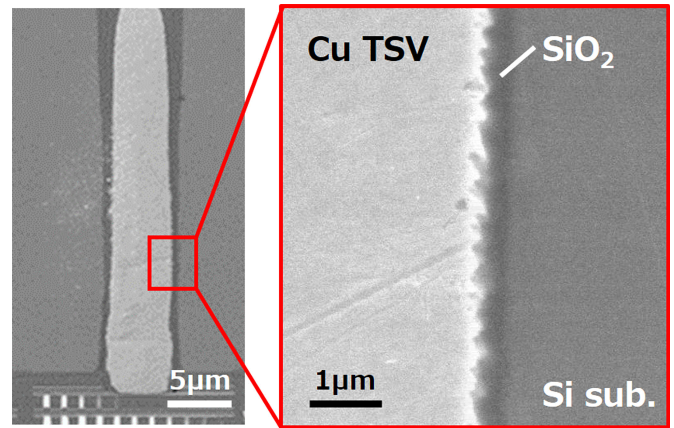

FIGURE 10. Cross-sectional SEM image of the fabricated multiwell-structured TSV.

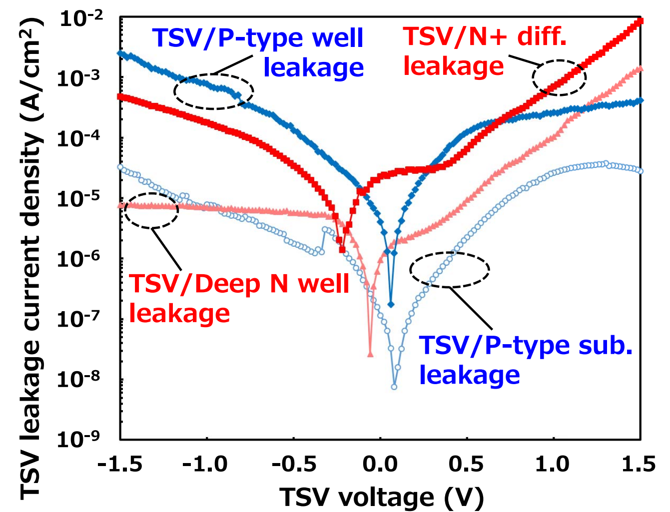

FIGURE 11. J-V characteristics between TSV and each well of the test sample with multiwell structure.

has a multiwell structure. SCM can obtain the 2D distribution of the carrier concentration by measuring the capacitance between the sample and the probe, such as the cantilever of the atomic force microscope (AFM), because the capacitance can be changed by the carrier concentration change. This chip has a 180-nm N-type diffusion layer, 780-nm P-type well, and 2830-nm deep N-type well. The value of the dopant concentration of each layer was that which is used in the standard 90-nm CMOS technology. The multiwell structure can be clearly observed, the dependence of the interface state on the depth direction can be evaluated by fabricating TSVs across the multiwell. To fabricate multiwall-structured TSV, an IC chip was bonded on the Si interposer with Cu/Sn microbumps firstly. After flip-chip bonding, the thickness of the Si substrate of the IC chip was reduced to 30 µm. Then, the SiO_2 passivation layer was deposited and the via-hole was formed by the Bosch process. Following this, the TSV liner was deposited. In this study, the TSV liner was made of SiO_2 which was deposited by PE-CVD with O_2 and TEOS. The deposition thickness was 4 µm at the backside of the chip. The deposition temperature was 200 °C. The maximum process temperature was decided by the thermal stability of underfill or temporary adhesive in the chip-level 3D-integration process. After the bottom opening process, the Ti barrier and the Cu seed layer were deposited by RF magnetron sputtering. Then, the via-holes were filled with Cu by electroless and electrolytic plating. Finally, the overburden Cu was removed by the CMP process. Fig. 10 shows the cross-sectional SEM image of the fabricated- multiwell-structured TSV. The diameter and depth of the TSVs were 6 µm and 30 µm, respectively. The TSV liner was evaluated using this test sample.

B. MEASUREMENT RESULTS AND DISCUSSION

Firstly, the current density (J) versus voltage (V) characteristics between the TSV and each well, shown in Fig. 11, were measured. The difference of the leakage current between TSV and each well can be observed. The results indicate that the leakage current can be measured through the liner insulator at a different depth with the multiwell-structured TSVs. Fig. 12 shows the dependences of the leakage current and sidewall SiO_2 thickness on the depth direction. The thickness of the sidewall SiO_2 was measured from the cross-sectional SEM image of the test sample, as shown in Fig. 10. As the TSV depth increased, the leakage current decreased, while the sidewall SiO_2 thinned. This was induced by the poor step coverage characteristics of PE-CVD. In this study, the TSVs with the aspect ratio of 6 were used in the test structure. In the case of the TSVs with a higher aspect ratio, the signal of the noise can be increased due to poorer step coverage. These results indicate that the multiwell-structured TSV can measure the variation in electrical characteristics induced by the nonconformal TSV liner along the depth direction. In addition, large parasitic capacitance, which is induced by thinner sidewall SiO_2, can increase coupling noise. However,

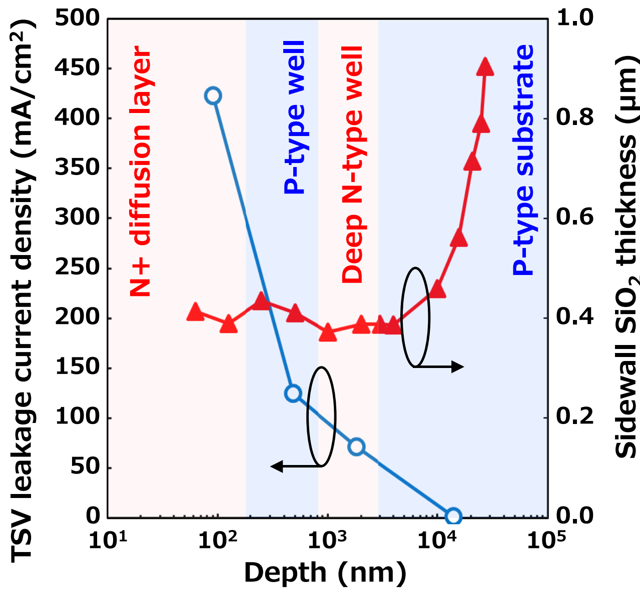

FIGURE 12. Effect of the sidewall SiO2 thickness on maximum TSV leakage current density.

the interface trap can also lead to noise propagation, as shown in Fig. 6. To evaluate the interface trap density, we measure the charge-pumping current around the SiO_2 liner using the multiwell-structured TSV.

Next, the drain current (I_d) – gate voltage (V_g) characteristics of the MOSFETs formed on the side wall of the TSVs were measured. Here, the Cu-TSV works as a gate electrode. Fig. 13 shows the I_d-V_g characteristics of the MOSFETs formed on the TSVs. The P-type well, deep-N-type well and N^+-diffusion layer were used as the body, source and drain, respectively, during measurement of the nMOSFET, while the deep-N-type well, P-type well, and P-type substrate were used as the body, source and drain during measurement of the pMOSFET. Thus, the typical I_d-V_g characteristics can be obtained. These results indicate that the interface traps of the TSV liner can be evaluated using the MOSFETs formed on the TSVs.

In this study, the charge-pumping technique was used to evaluate the dependence of interface traps of the TSV liner on the depth direction. Fig. 14 shows the measurement setup and pulse waveform for the measurement of the charge-pumping current. The TSV acts as a gate electrode of the MOSFET in this measurement; here, V_{Psub}, V_{dNw}, and V_{Pw} are the voltages impressed on the P-type substrate, the deep-N-type well, the P-type well, and the N-type diffusion layer, respectively, and I_{Psub}, I_{dNw}, and I_{Pw} are the currents flowing in the P-type substrate, deep-N-type well, P-type well, and N-type diffusion layer, respectively. First, I_{Psub} and I_{Pw} were measured at 0 V for V_{Psub}, V_{dNw}, and V_{Pw}. I_{Psub} and I_{Pw} were obtained as shown in Fig. 15; here, the frequency, duty ratio and amplification of the applied pulse were 100 kHz, 50% and 2.0 V, respectively. I_{Psub} includes the charge-pumping currents induced by the interface trap

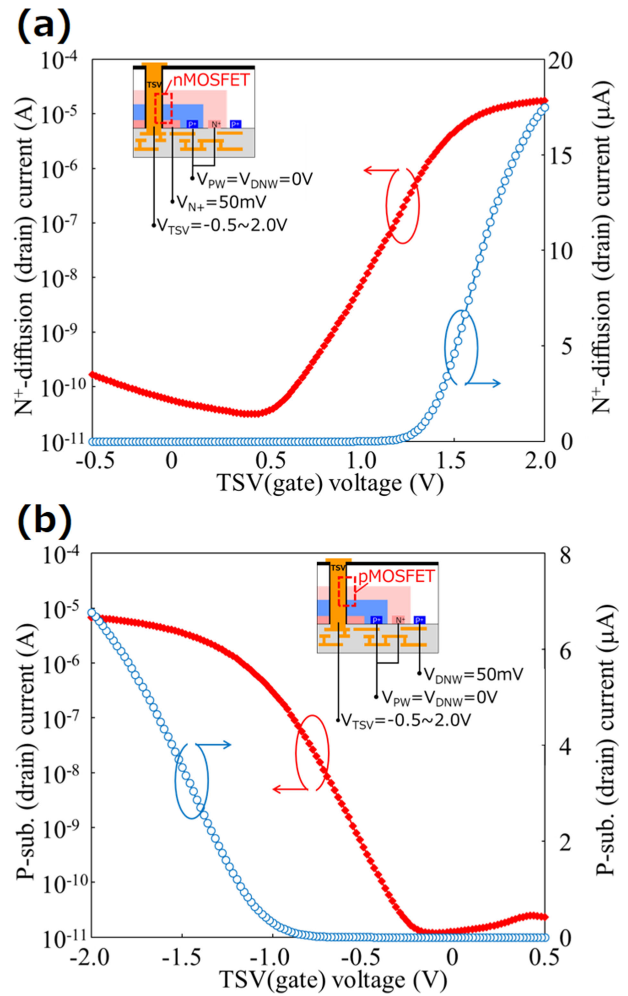

FIGURE 13. I_d-V_g characteristics of the (a) nMOSFET and (b) pMOSFET formed on the sidewall of the TSVs.

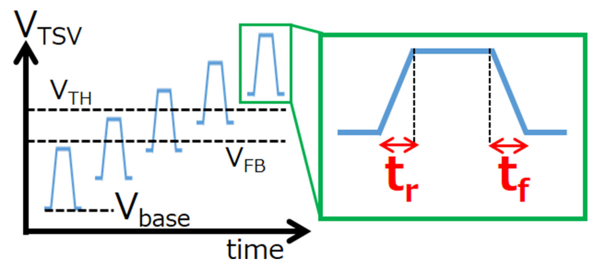

FIGURE 14. Pulse waveforms applied to TSV for charge-pumping current measurement.

between the TSV and the P-type substrate as well as that between the TSV and the deep N-type well. The interfaces of both the P-type substrate and deep N-type well shift into the accumulation and inversion state. I_{Pw} also includes charge-pumping currents induced by the interface trap between TSV and deep N-type well, and interface trap between TSV and P-type well. The charge-pumping current was extracted from I_{Psub} and I_{Pw} by peak separation using the Voigt function, as shown in Fig. 15. Then, the trap density between TSV

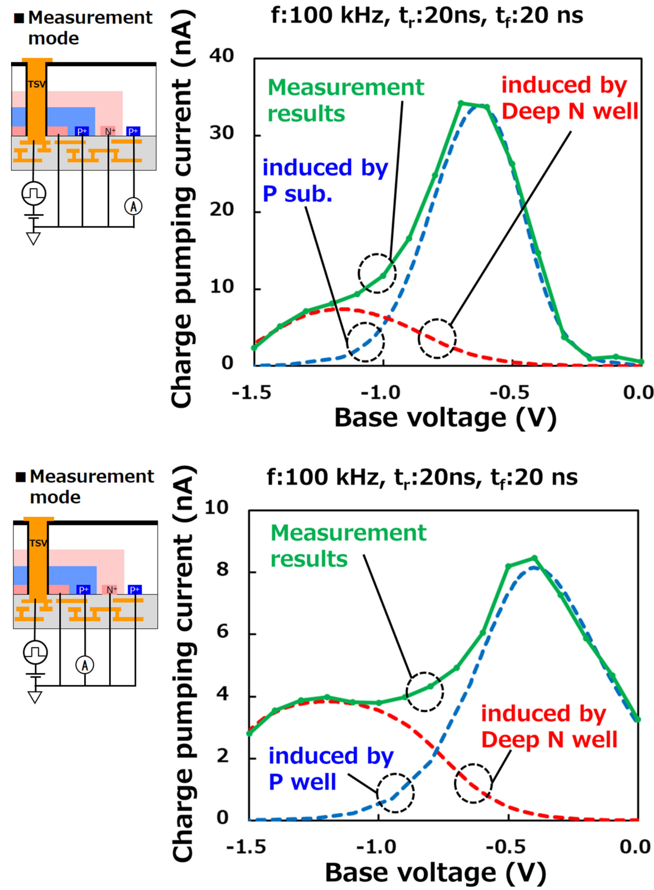

FIGURE 15. Charge-pumping currents between (upper) P-type substrate and TSV, and deep N-type well and TSV, (bottom) deep N-type well and TSV, and p-type well and TSV.

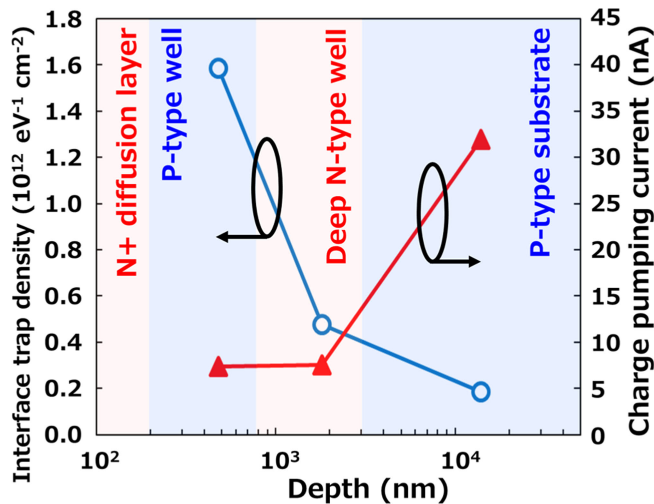

FIGURE 16. Dependence of interface trap density and charge-pumping current on TSV depth direction.

and each well was calculated from the charge-pumping current. Fig. 16 shows the dependence of the trap density and charge-pumping current on the TSV depth direction. Within a span of approximately 200 nm from the bottom of the TSV, the trap density decreases steeply. Meanwhile, the thickness of the sidewall SiO_2 of the bottom side was thinner than that of the top side, as shown in Fig. 12. This indicates that the plasma reaction to deposit the SiO_2 is not sufficient at the bottom side of the TSVs. This insufficient plasma reaction leads to an increase in the trap density. This can be induced by a charge-up phenomenon on the bottom side of the TSV during the deep etching process. The dependence of the TSV liner interface state on the depth direction was indicated for the first time. Fig. 17 shows the effect of the pulse frequency on charge-pumping currents. In general, the charge-pumping current has a proportional relationship with the pulse frequency. However, this relationship deviates slightly in the high-frequency region. These results indicate the existence of the ion or the traps, which have a low-frequency response. This phenomena was induced by Cu-ions diffusion into the liner layer. Therefore, the deposition method used to form the conformal barrier layer also requires investigation.

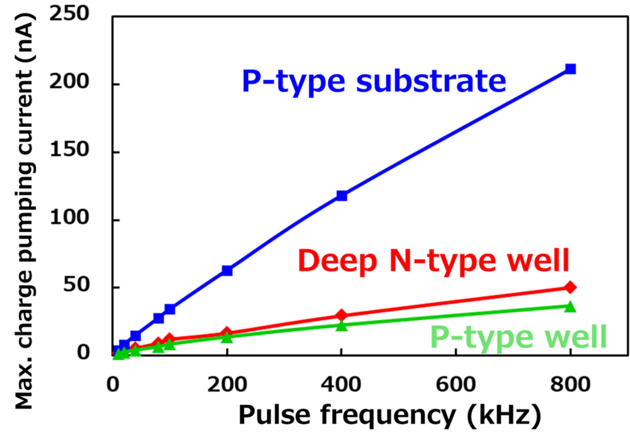

FIGURE 17. Effect of the pulse frequency on maximum charge-pumping current for each trap.

We demonstrated that a multiwell-structured TSV can evaluate the step coverage of the TSV liner and the dependence of trap density on the depth direction. Then, the evaluation results with multiwell-structured TSV indicated that for the TSV liner, improvements on the step coverage must be considered, and the trap density dependence must be suppressed.

IV. CONCLUSION

In this study, we fabricated a mixed-signal 3D-IC with the via-last/backside-via process. The results of measurements by the mixed-signal 3D-IC indicated that the ring-oscillator-induced noise in digital circuits was propagated to analog circuits through the Si substrate and TSVs. To further confirm the noise propagation in 3D-IC, the TSV liner interface was investigated using the multiwell-structured TSV and charge-pumping method. As a result, it was indicated, for the first time, that depth-dependent interface states existed in the TSV liner, which enhances the noise propagation among

stacked chips. For high reliability mixed-signal 3D-IC, novel technologies such as an atomic layer process, novel barrier technologies and a polymer liner process are necessary to improve step-coverage and decrease the trap density around the TSV liner [15]–[22].

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