Received 3 June 2019; revised 29 July 2019; accepted 8 August 2019. Date of publication 13 August 2019; date of current version 30 August 2019.
The review of this article was arranged by Editor N. Collaert.

*Digital Object Identifier 10.1109/JEDS.2019.2934745*

# Characterization of High-Performance InGaAs QW-MOSFETs With Reliable Bi-Layer $HfO_xN_y$ Gate Stack

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This work was supported in part by the Nano Material Technology Development Program under Grant 2017M3A7B4049515, and in part by the Basic Science Research Programs through the National Research Foundation of Korea under Grant 2019R1A2C1008894.

**ABSTRACT** In this work, we report high-performance InGaAs quantum-well MOSFETs with optimized bi-layer high-k gate dielectrics incorporating high-quality plasma-assisted atomic -layer-deposited (PA-ALD) $HfO_xN_y$ interfacial layer (IL). With more than 1 nm IL deposition to passivate the InGaAs surface, excellent sub-threshold characteristics ($SS_{min}$ = 68 mV/dec) were achieved through the proposed gate stack technology. We performed positive-bias-temperature-instability (PBTI) measure -ments in order to ensure a reliable gate operation. The proposed bi-layer III-V gate stack achieved the excellent value of maximum gate overdrive voltage ($V_{OV,max}$) of 0.49 V with CET = 1.04 nm. The proposed gate stack has a great potential for III-V MOSFET technology to low power logic applications.

**INDEX TERMS** Indium gallium arsenide (InGaAs), III-V MOSFET, high-k gate dielectric, hafnium oxynitride ($HfO_xN_y$), PBTI reliability.

## I. INTRODUCTION

Though the traditional physical scaling of advanced metal-oxide semiconductor field-effect transistors (MOSFETs) in conjunction with Dennard's scaling rules has become very challenging [1], various technologies have been introduced to enable the pursuit of the scaling roadmap [1]–[4]. Among the proposed technologies, III-V channel technology has emerged as one of the most promising n-type channel candidates for the future highly scaled CMOS applications, due to its significant carrier transport characteristics [2]. However, the defective interface quality of high-k/III-V MOS has been one of the major bottlenecks toward the practical realization of III-V compound semiconductor devices for several decades [5], and thus a great deal of research has been mainly oriented to the interface quality improvement [6]–[13]. The reliability improvement of the gate stack is also an important issue for logic devices [14], [15]. The major concern associated with the high-k dielectrics for scaled MOS devices is that the defects not only residing in the interface but also in the high-k dielectric itself exert great impact on the device reliability characteristics [15], [16]. Even though $HfO_2$ has been regarded as the most promising high-k candidate to replace $SiO_2$ in various electronic devices, high-density intrinsic electron traps, mainly generated from the oxygen vacancies within $HfO_2$, have severely degraded the oxide reliability [15], [16].

Direct deposition of $HfO_2$ on InGaAs substrate has been difficult to use due to large density electron traps and the approach to employ bi-layer high-k schemes with the improved interface layer (IL) has become the common strategy to address the goal of thin effective-oxide-thickness (EOT) and good interface quality simultaneously [6], [8]–[10]. Among several IL candidates, $Al_2O_3$ has been the dominant high-k IL in III-V MOS research due to its strong advantage of 'self-cleaning effect' [6], [7], [12]. Despite employing $Al_2O_3$ has accomplished the excellent interface passivation results in wide literatures, the issues concerning the oxide reliability are still unresolved [17].

Recently, it was reported that the polycrystalline AlN is effective to passivate the III-V surface dangling bonds in conjunction with a substantial improvement in the gate stack reliability [18]. Also, the most advanced results were recently reported by using the combination of unknown ALD IL material which was developed with ASM system referred to as ASM-IL ($\kappa$-value ~6) and $LaSiO_x$ on the InGaAs substrate [10]. It was suggested that the developed IL might form a more favorable defect band distribution and a further reduction on the oxide defects.

Our previous work demonstrated the excellent interface characteristics with the optimized plasma-assisted atomic -layer-deposition (PA-ALD) $HfO_xN_y$ process [11]. Noticeable trade-off relationships in terms of bulk and interface quality existed between the $O_3$ and Isopropyl-alcohol (IPA) based $HfO_xN_y$. In order to achieve a reliable gate stack, we need to compromise the trade-off relationship in the $HfO_xN_y$ processes. In this work, we propose a bi-layer ALD high-k gate stack scheme which utilizes an IPA-based $HfO_xN_y$ IL and an $O_3$-based $HfO_xN_y$ bulk layer. The proposed gate stack shows strong potential in achieving not only an excellent interface quality but also an improvement in reliability performance. Also, our proposed scheme is expected to achieve better EOT scalability compared to the previously reported III-V MOS researches due to the high dielectric constant of $HfO_xN_y$.

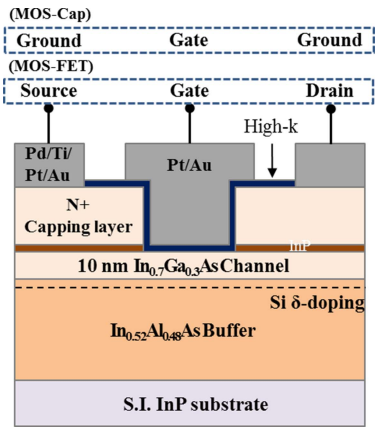


**FIGURE 1.** Schematic diagram of the fabricated InGaAs QW MOSFETs.

## II. EXPERIMENTAL DETAILS

Quantum-well InGaAs MOSFETs were fabricated with the schematic shown in Fig. 1. The epitaxial III-V MOSFET material structure was composed of a semi-insulating InP substrate, a thick $In_{0.52}Al_{0.48}As$ buffer with a Si-delta doping layer under the channel, a 10 nm $In_{0.7}Ga_{0.3}As$ channel, a 3 nm InP etch stop layer, and highly doped capping layers. The capping layers consisted of a 20 nm $n^+$ $In_{0.52}Al_{0.48}As$ (Si-doped, $2 \times 10^{19}$ $cm^{-3}$), a 15 nm $n^+$ $In_{0.53}Ga_{0.47}As$ layer (Si-doped, $3 \times 10^{19}$ $cm^{-3}$), and a 10 nm $n^+$ $In_{0.7}Ga_{0.3}As$ layer (Si-doped, $3 \times 10^{19}$ $cm^{-3}$). The process flow of MOSFET fabrication was as followings. The mesa isolation was first performed with phosphoric acid wet etching. Then the selective gate recess was done with citric acid using a $SiN_x$ dielectric mask. Then after removing the $SiN_x$ mask, 4 cycles of digital etching based on sequential $O_2$ plasma and HCl etching were performed to fully remove the InP etch stop layer [19]. After high-k dielectric deposition, Pt/Au gate metal contact was deposited by lift-off process and the post metallization annealing was carried out at 400°C for 30 min in forming gas ambient ($N_2$ 95%, $H_2$ 5%). Finally, Pd/Ti/Pt/Au ohmic metal stack was deposited.

**TABLE 1.** Description of III-V MOS gate stacks.

| Sample | Bi-layer high-k design | |
|---|---|---|
| | (IL) IPA-based $HfO_xN_y$ | (Bulk) $O_3$-based $HfO_xN_y$ |
| Ref. | 0 cycle | 30 cycle |
| A | 5 cycle | 25 cycle |
| B | 10 cycle | 20 cycle |
| C | 30 cycle | 0 cycle |

The gate stacks studied in this work are shown in Table 1. Details of the pretreatment and the high-k dielectric deposition processes were described in our previous work [11]. The bi-layer gate stack consisted of an IPA-based PA-ALD $HfO_xN_y$ for the interface and an $O_3$-based PA-ALD $HfO_xN_y$ for the bulk. The IPA-based PA-ALD $HfO_xN_y$ IL was employed due to its superior interface characteristics, which was attributed to both the low surface oxidation ability of IPA and the suppression of oxygen diffusion by effective nitrogen passivation of oxygen vacancies in $HfO_2$ [11]. The $O_3$-based PA-ALD $HfO_xN_y$ yielded better bulk characteristics such as the reduced leakage currents, probably due to the strong oxidizing ability of $O_3$ [20], [21]. Therefore, the IL thickness should be optimized to achieve both improved interface and reliability performance.

## III. RESULTS AND DISCUSSION

The $I_D$-$V_G$ transfer characteristics of InGaAs QW MOSFETs are shown in Fig. 2 for all the samples. As expected, improved device characteristics were achieved for the samples employing the IPA-$HfO_xN_y$ IL compared to the reference having only $O_3$-based $HfO_xN_y$ dielectric. As shown in Fig. 3, significant improvements in the aspect of on/off current ratio were achieved by inserting the IL through the on-current improvement for sample A and B, reaching ~ $10^6$ at $V_D = 0.5$ V. However, slight off-current degradation occurred for the single-layer IPA-based PA-ALD $HfO_xN_y$ gate dielectric (sample C) due to the gate leakage increase.

Moreover, the $I_D$-$V_D$ family characteristics of InGaAs QW MOSFETs are shown in Fig. 4 for all the samples. It was noticed that the drain current and the on-resistance dramatically improved for the samples employing the IPA-$HfO_xN_y$ IL compared to the reference having only $O_3$-based $HfO_xN_y$ dielectric.

Also, as shown in Fig. 5, remarkable subthreshold-slope (SS) improvement was observed by employing the IPA-based $HfO_xN_y$ IL. The extracted SS value at the gate length of 20 $\mu$m was 77, 76, and 72 mV/dec at $V_D = 0.5$ V

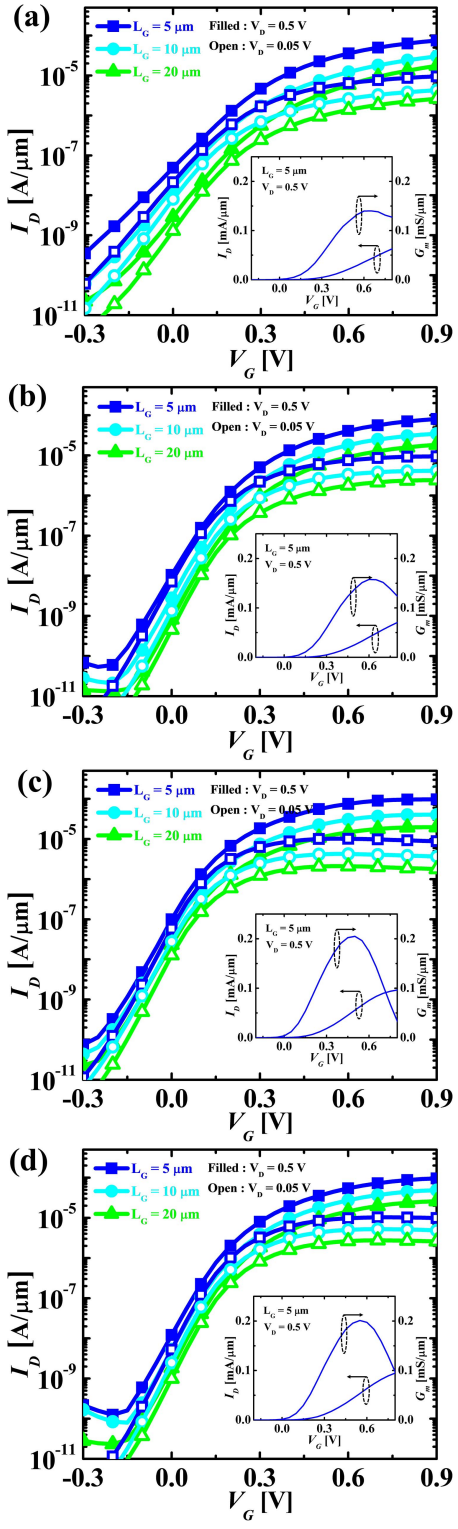


**FIGURE 2.** The $I_D$-$V_G$ transfer characteristics with gate length $L_G$ = 5, 10, 20μm of sample (a) ref. (b) A (c) B and (d) C measured at $V_D$ = 0.5 and 0.05 V; Insets represent the linear-scale $I_D$-$V_G$ curve of $L_G$ = 5μm device measured at $V_D$ = 0.5 V.

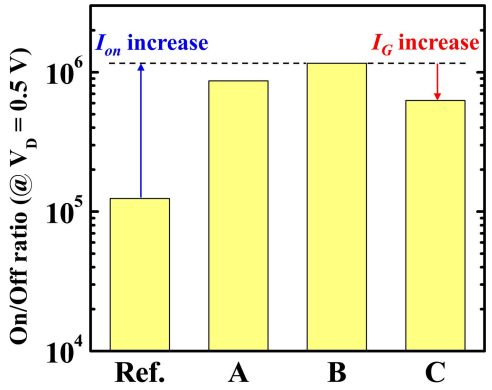


**FIGURE 3.** On/off ratio comparison of varied gate stacks measured at $V_D$ = 0.5 V.

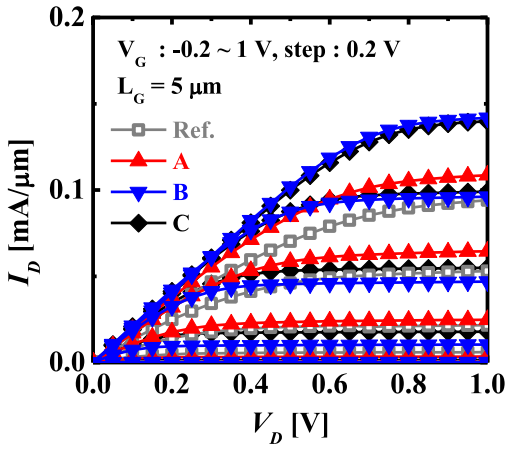


**FIGURE 4.** The $I_D$-$V_D$ family characteristics for all samples with $L_G$ = 5μm.

and 72, 70, and 68 mV/dec at $V_D$ = 0.05 V for sample A, B, and C, respectively. The low SS values achieved in this work are comparable to the best results on planar III-V devices [10]. It suggests that an extraordinary interface quality can be achieved with the IL of this work. In addition, as shown in the insets of Fig. 2, the maximum transconductance ($G_{m,max}$) increased as the IL thickness increased. The $G_{m,max}$ increase was saturated at the IL thickness above 1 nm.

For the detailed interface analysis, the multi-frequency (1 kHz – 1 MHz) C-$V_G$ measurements were performed at a ring shape device and the results are shown in Fig. 6. The capacitance-equivalent thickness (CET) was extracted considering the semiconductor capacitance of the III-V substrate [22]. Significant improvements in both the CET and the frequency dispersion were achieved with the IL insertion. As the IL thickness increased, the CET decreased down to 1.04 nm (sample B and C). This CET improvement with the suppression of undesired interfacial oxide [11] exerted definite impacts on the electrical characteristics regarding the SS and $G_{m,max}$ results. Furthermore, distinct suppression of frequency dispersion was observed through the IL deposition. In particular, the gate capacitance in the accumulation region showed the smallest frequency dispersions in the sample B which reflects the reduced border trap density [23]. The $D_{it}$ distributions were extracted by the conductance method and

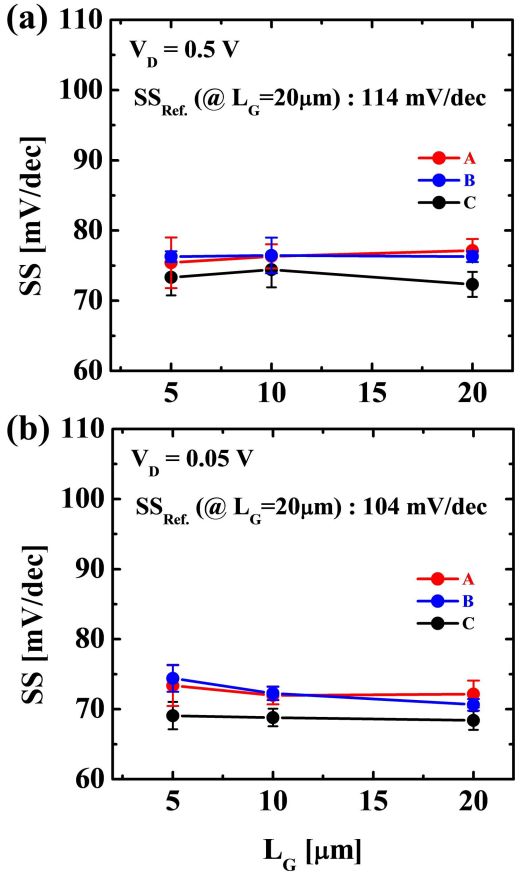


**FIGURE 5.** Minimum SS for varied gate stacks in terms of gate length measured at (a) $V_D = 0.5$ V (b) $V_D = 0.05$ V.

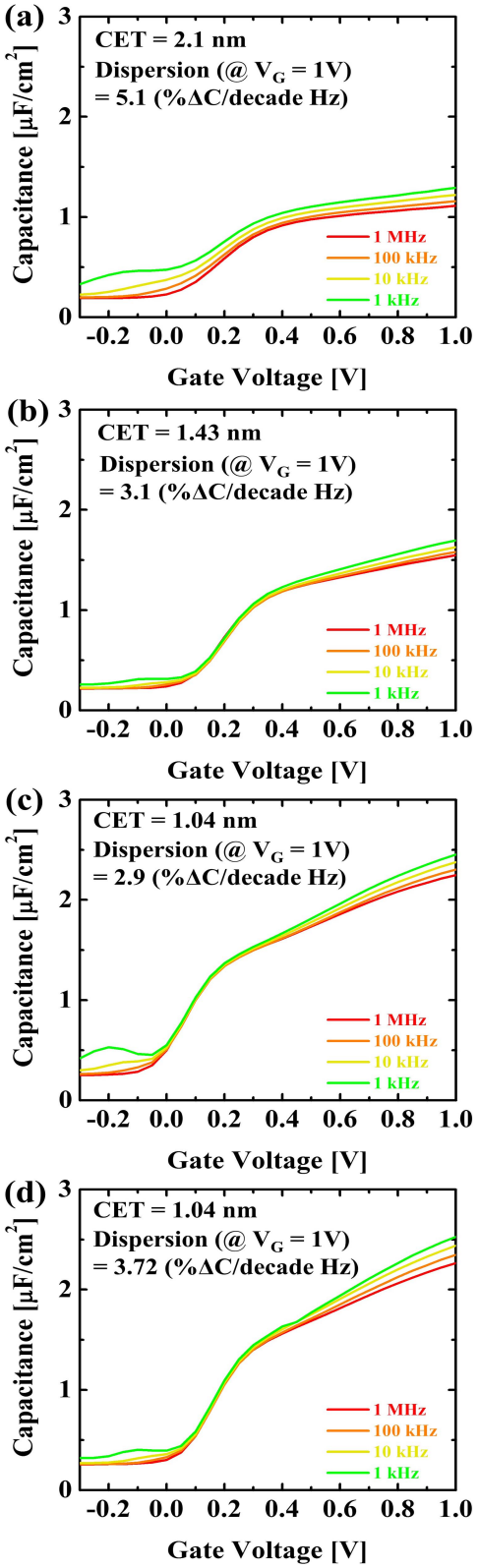


**FIGURE 6.** The multi-frequency C-$V_G$ characteristics of sample (a) ref. (b) A (c) B and (d) C.

shown in Fig. 7 for all the samples. While high values of mid-gap $D_{it}$ over $10^{12}$ $eV^{-1}cm^{-2}$ were observed for the reference sample, mid-gap $D_{it}$ decreased remarkably down to $3 \times 10^{11}$ $eV^{-1}cm^{-2}$ with IL insertion, which was consistent with the SS improvement. In conclusion, in terms of the interface quality, at least 1nm IPA-based $HfO_xN_y$ IL deposition was required.

In addition, the positive bias temperature instability (PBTI) characteristics were measured for sample B and C in order to investigate the advantage of using bi-layer gate stack scheme further. The PBTI stress measurements were performed using the measure-stress-measure technique under various positive gate stress voltages [10], [17], [18]. The amount of threshold voltage shift $\Delta V_{th}$ under high gate stress bias represents the electron trapping rate in defects located at both the interfacial layer and the bulk high-k dielectric. Figure 8 shows the measured $\Delta V_{th}$ of InGaAs QW-MOSFETs as a function of stress time for varied gate stress voltages. The threshold voltage $V_{th}$ was extracted using the linear extrapolation method at the $G_{m,max}$ gate bias. It should be noted that the bi-layer gate stack approach (sample B) exhibited much smaller $\Delta V_{th}$ under similar $V_G$ - $V_{th}$ stress compared to the single-layer IPA-based $HfO_xN_y$ gate dielectric (sample C). Also, the power law time exponent (n) at high gate stress biases which represents the trap generation rate and electron trapping rate reduced significantly from 0.18 to 0.11 with employing the bi-layer gate stack. These results support that

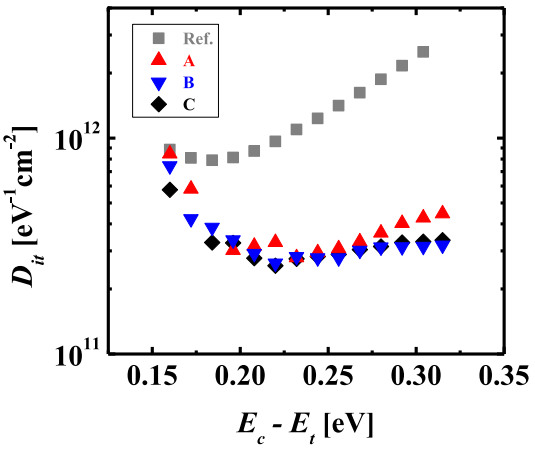


**FIGURE 7.** $D_{it}$ distribution of varied gate stacks extracted by conductance method.

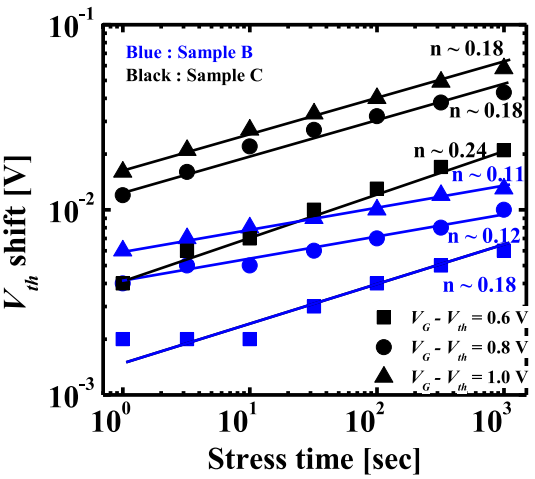


**FIGURE 8.** Stress time evolution of threshold voltage shift under varied PBTI stress for sample B and C.

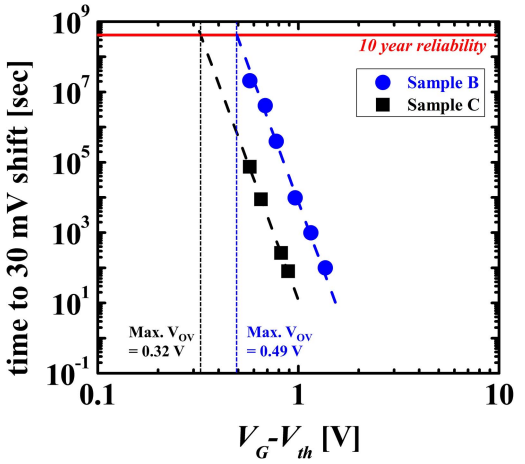


**FIGURE 9.** The lifetime extrapolation with varied gate stress for sample B and C.

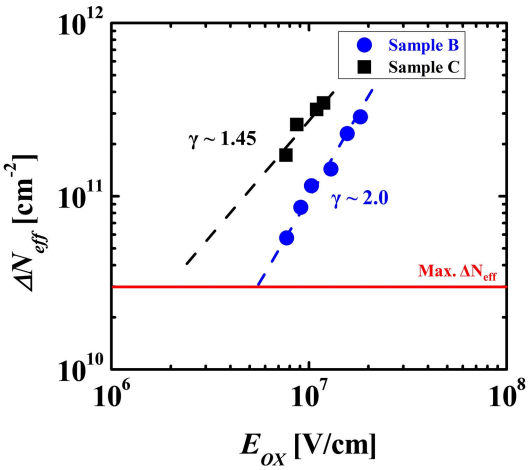


**FIGURE 10.** Trapped charge density as a function of $E_{ox}$ for sample B and C.

the superior bulk characteristics of the $O_3$-based $HfO_xN_y$ are well reflected in the proposed bi-layer high-k gate stack.

Moreover, based on the PBTI measurements, the 10 year lifetime reliability was extrapolated from the time to $\Delta V_{th}$ = 30 mV shift at various gate stress conditions (Fig. 9). The maximum operating overdrive voltage ($V_{OV}$) that ensures 10 year reliability was estimated to be 0.49 V and 0.32 V for sample B and C, respectively. It is worth mentioning that the maximum $V_{OV}$ targets for the accumulation mode III-V MOSFETs of $V_{DD}$ = 0.5 V and 0.75 V are 0.33 V and 0.5 V, respectively [10]. The proposed bi-layer gate stack achieved these values successfully even on low CET.

In addition, the trapped charge density ($\Delta N_{eff}$, $\Delta N_{eff} = \Delta V_{th} \times C_{ox}/q$) was evaluated on the stress time of 1 sec (Fig. 10) as a function of effective oxide field ($E_{ox}$, $E_{ox} = (V_G - V_{th}) / CET$). It was proposed that in order to ensure reliable device operation, the maximum $\Delta N_{eff}$ should be less than $3 \times 10^{10}$ cm$^{-2}$ at the operating field ($E_{ox}$ = 3.5 MV/cm) for an EOT 1nm gate stack [10]. For sample B, great reduction of $\Delta N_{eff}$ to $1.3 \times 10^{10}$ cm$^{-2}$ at $E_{ox}$ = 3.5 MV/cm was achieved with the bi-layer gate stack approach. Also, the electric field acceleration exponent ($\gamma$), which represents the oxide defect level distribution, beneficially increased from 1.45 to 2.0, suggesting the improved defect band distribution [10].

**TABLE 2.** Benchmarking of III-V MOS gate stacks.

| Research | Device properties | | | | |
|---|---|---|---|---|---|
| | $L_G$ [μm] | Dielectric | CET [nm] | $SS_{min}$ (@ $V_D$ = 50 mV) [mV/dec] | Max. $V_{OV}$ [V] |
| [17] | 20 | $Al_2O_3$ | 5.3 | 77 | 0.23 |
| [10] | 50 | ASM-IL / $LaSiO_x$ / $HfO_2$ | 1.46 | 68 | 0.43 |
| [18] | 6 | AlN / $HfO_2$ | 1.4 | 120 | 0.41 |
| Sample B (This work) | 20 | HfON (IPA) / HfON ($O_3$) | 1.04 | 70 | 0.49 |
| Sample C (This work) | 20 | HfON (IPA) | 1.04 | 68 | 0.32 |

In Table 2, the device properties of various III-V MOS gate stacks are benchmarked. Although the $Al_2O_3$ reported superior interface characteristic in the early stage of research, it certainly degraded the reliability performance. Among the proposed technologies, the bi-layer high-k design developed in this work demonstrates the most outstanding overall device performances. It is believed that the proposed IPA-HfON IL bi-layer gate stack would provide a path to establish high performance III–V MOSFETs with reliable gate stacks, fulfilling the stringent requirement for energy-efficient nanoscale MOSFETs.

## IV. CONCLUSION

In this work, we proposed a high quality IPA-based PA-ALD $HfO_xN_y$ IL technology and presented an excellent device performance along with a great reliability improvement. With the IL insertion, low SS was achieved with $G_m$ improvement and low CET. Also, a significant mid-gap $D_{it}$ reduction was observed, which brought the excellent sub-threshold performance. In addition, through the PBTI measurements, clear advantage of using a bi-layer gate stack scheme was reported achieving the stringent BTI reliability targets. In summary, we believe that the developed $HfO_xN_y$ IL has great potential over the low-k IL materials and it would contribute to the most advanced III-V MOSFETs for future technology node.

## REFERENCES

[1] M. T. Bohr and I. A. Young, "CMOS scaling trends and beyond," *IEEE Micro*, vol. 37, no. 6, pp. 20–29, Nov./Dec. 2017. doi: 10.1109/MM.2017.4241347.

[2] J. A. del Alamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature*, vol. 479, no. 7373, p. 317, Nov. 2011. doi: 10.1038/nature10677.

[3] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, p. 405, Dec. 2008. doi: 10.1021/nl071804g.

[4] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-*k* gate dielectric," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007. doi: 10.1109/TED.2007.899389.

[5] J. Robertson, Y. Guo, and L. Lin, "Defect state passivation at III–V oxide interfaces for complementary metal–oxide–semiconductor devices," *J. Appl. Phys.*, vol. 117, no. 11, Mar. 2015, Art. no. 112806. doi: 10.1063/1.4913832.

[6] R. Suzuki *et al.*, "1-nm-capacitance-equivalent-thickness $HfO_2/Al_2O_3$/InGaAs metal–oxide–semiconductor structure with low interface trap density and low gate leakage current density," *Appl. Phys. Lett.*, vol. 100, no. 13, Feb. 2012, Art. no. 132906. doi: 10.1063/1.3698095.

[7] C. L. Hinkle *et al.*, "GaAs interfacial self-cleaning by atomic layer deposition," *Appl. Phys. Lett.*, vol. 92, no. 7, Feb. 2008, Art. no. 071901. doi: 10.1063/1.2883956.

[8] Q. H. Luc *et al.*, "Effects of *in-situ* plasma-enhanced atomic layer deposition treatment on the performance of $HfO_2/In_{0.53}Ga_{0.47}As$ metal–oxide–semiconductor field-effect transistors," *IEEE Electron Device Lett.*, vol. 37, no. 8, pp. 974–977, Jun. 2016. doi: 10.1109/LED.2016.2581175.

[9] C.-Y. Chang *et al.*, "Impact of $La_2O_3$ interfacial layers on InGaAs metal–oxide–semiconductor interface properties in $Al_2O_3/La_2O_3$/InGaAs gate stacks deposited by atomic-layer-deposition," *J. Appl. Phys.*, vol. 118, no. 8, Aug. 2015, Art. no. 085309. doi: 10.1063/1.4929650.

[10] A. Vais *et al.*, "On the development of a reliable gate stack for future technology nodes based on III–V materials," *Adv. Sci. Technol. Eng. Syst.*, vol. 3, no. 5, p. 36, Sep. 2018. doi: 10.25046/aj030506.

[11] S. K. Eom, M.-W. Kong, M.-J. Kang, J.-G. Lee, H. Y. Cha, and K. S. Seo, "Enhanced interface characteristics of PA-ALD $HfO_xN_y$/InGaAs MOSCAPs using IPA oxygen reactant and cyclic $N_2$ plasma," *IEEE Electron Device Lett.*, vol. 39, no. 11, pp. 1636–1639, Nov. 2018. doi: 10.1109/LED.2018.2870176.

[12] V. Chobpattana, J. Son, J. J. Law, R. Engel-Herbert, C.-Y. Huang, and S. Stemmer, "Nitrogen-passivated dielectric/InGaAs interfaces with sub-nm equivalent oxide thickness and low interface trap densities," *Appl. Phys. Lett.*, vol. 102, no. 2, Jan. 2013, Art. no. 022907. doi: 10.1063/1.4776656.

[13] T. Kent *et al.*, "The influence of surface preparation on low temperature $HfO_2$ ALD on InGaAs (001) and (110) surfaces," *J. Chem. Phys.*, vol. 143, no. 16, Oct. 2015, Art. no. 164711. doi: 10.1063/1.4934656.

[14] M. Denais *et al.*, "Interface trap generation and hole trapping under NBTI and PBTI in advanced CMOS technology with a 2-nm gate oxide," *IEEE Trans. Device Mater. Rel.*, vol. 4, no. 4, pp. 715–722, Dec. 2004. doi: 10.1109/TDMR.2004.840856.

[15] A. Kerber and E. A. Cartier, "Reliability challenges for CMOS technology qualifications with hafnium oxide/titanium nitride gate stacks," *IEEE Trans. Device Mater. Rel.*, vol. 9, no. 2, pp. 147–162, Mar. 2009. doi: 10.1109/TDMR.2009.2016954.

[16] J. L. Gavartin, D. M. Ramo, and A. L. Shluger, "Negative oxygen vacancies in $HfO_2$ as charge traps in high-k stacks," *Appl. Phys. Lett.*, vol. 89, no. 8, Aug. 2006, Art. no. 082908. doi: 10.1063/1.2236466.

[17] J. Franco *et al.*, "Suitability of high-k gate oxides for III–V devices: A PBTI study in $In_{0.53}Ga_{0.47}As$ devices with $Al_2O_3$," in *Proc. IEEE Int. Rel. Phys. Symp.*, Jun. 2014, p. 6A.2.1. doi: 10.1109/IRPS.2014.6861098.

[18] P.-C. Chang *et al.*, "Electrical analysis and PBTI reliability of $In_{0.53}Ga_{0.47}As$ MOSFETs with AlN passivation layer and $NH_3$ postremote plasma treatment," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3466–3472, Aug. 2016. doi: 10.1109/TED.2016.2593022.

[19] J. A. del Alamo, D. A. Antoniadis, J. Lin, W. Lu, A. Vardi, and X. Zhao, "Nanometer-Scale III-V MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 4, no. 5, pp. 205–214, Sep. 2016. doi: 10.1109/JEDS.2016.2571666.

[20] M. Cho *et al.*, "Comparison of properties of an $Al_2O_3$ thin layers grown with remote $O_2$ plasma, $H_2O$, or $O_3$ as oxidants in an ALD process for $HfO_2$ gate dielectrics," *J. Electrochem. Soc.*, vol. 152, no. 5, p. F49, Apr. 2005. doi: 10.1149/1.1884130.

[21] H. Sim, H. Chang, and H. Hwang, "Electrical characteristics of ozone-oxidized $HfO_2$ gate dielectrics," *Jpn. J. Appl. Phys.*, vol. 42, no. 4A, p. 1596, Apr. 2003. doi: 10.1143/JJAP.42.1596.

[22] R. Engel-Herbert, Y. Hwang, and S. Stemmer, "Quantification of trap densities at dielectric/III–V semiconductor interfaces," *Appl. Phys. Lett.*, vol. 97, no. 6, Aug. 2010, Art. no. 062905. doi: 10.1063/1.3479047.

[23] Y. Yuan *et al.*, "A distributed bulk-oxide trap model for $Al_2O_3$ InGaAs MOS devices," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2100–2106, Aug. 2012. doi: 10.1109/TED.2012.2197000.