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Direct Correlation of Ferroelectric Properties and Memory Characteristics in Ferroelectric Tunnel Junctions

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ABSTRACT Ferroelectric memories have made big advancements in the last years due to the discovery of ferroelectricity in already widely used hafnium oxide. Here we investigate ferroelectric tunnel junctions (FTJ) consisting of a ferroelectric hafnium zirconium oxide layer and a dielectric aluminum oxide layer. By varying the set and reset amplitude and pulse width the fraction of reversed ferroelectric domains can be controlled. Due to the statistical distribution of the coercive voltage the current can be tuned between the minimum off-state and maximum on-state current. This leads to possible multi-level information storage in our FTJs. In this paper a detailed study of the set/reset operation and the intermediate current levels is presented. Furthermore, the endurance properties of the memory device can be directly correlated to the wake-up and fatigue phenomena in the ferroelectric layer. While the usability of the memory window is still limited by the initial polarization increase and ultimately by the hard breakdown of the device, a further optimization of the ferroelectric layer itself and the ferroelectric/dielectric interface can directly improve the viability of the tunnel junction. Finally, we show that the current of our FTJs scales as expected and reproducible results across different devices are obtained.

INDEX TERMS Ferroelectrics, tunnel-junction, hafnium zirconium oxide, memory.

I. INTRODUCTION

The ever-increasing need for high density and fast data storage has become prevalent in all sectors in the last years due to the rise of smart hard- and software (Internet-of-Things, Industry 4.0, big data, etc.) [1]–[3]. Due to this, new emerging memory concepts are promising, which combine low power consumption, fast access speeds, high scalability and non-volatility. Several different kinds of memories, such as magnetic [4], phase-change [5], resistive [6] and also ferroelectric [7] random access memories have been explored in the recent past. Ferroelectric memories in the form of 1T (ferroelectric field-effect transistor, FeFET) or 1T1C (ferroelectric random access memory, FeRAM) cells have great prerequisites for these kinds of applications [8]–[9]. Especially the discovery of ferroelectricity in hafnium-based dielectrics in 2011 [10] led to new promising results for the aforementioned memory applications, as well as other areas, such as logic-in-memory [11], negative capacitance [12] and neuromorphic computing [13]. Besides these common research fields, ferroelectric tunnel junctions (FTJ) have gained popularity in the last years [14]–[16]. An FTJ consists of two metal electrodes with a ferroelectric layer in between, whose remanent polarization can be used to store information. Contrary to FeRAM, the read operation in an FTJ is non-destructive since the tunneling electroresistance/current is sensed, whereby the polarization in the ferroelectric layer remains unchanged. As an alternative to the nominally symmetric metal-ferroelectric-metal (MFM) approach we are utilizing an additional dielectric layer. In this double-layer stack, the ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) layer serves as the memory layer – where the binary information is stored

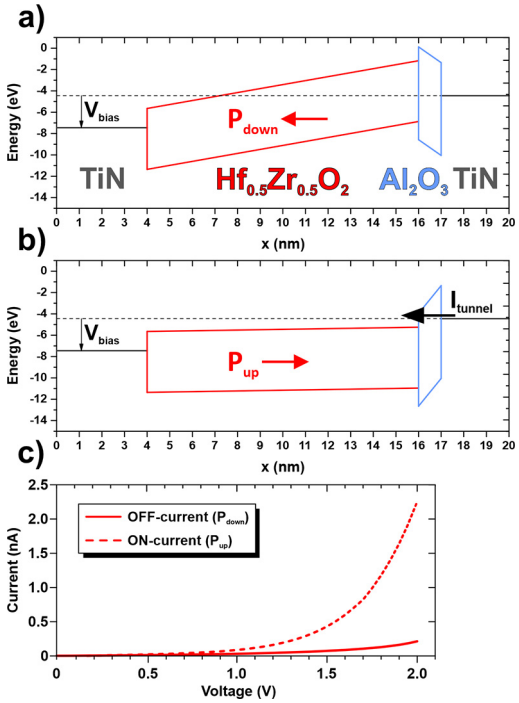

FIGURE 1. **Simulated band diagrams for both polarization states for a) P_{down} and b) P_{up} of TiN/$Hf_{0.5}Zr_{0.5}O_2$/Al_2O_3/TiN ferroelectric tunnel junctions indicating the different tunneling electroresistances, c) corresponding I-V curves for 12 nm HZO and 2 nm Al_2O_3 thickness for both opposite polarization states.**

– while a dielectric aluminum oxide (Al_2O_3) layer serves as the tunneling barrier for the electron conduction in this metal-ferroelectric-insulator-metal (MFIM) structure. Due to the internal band bending related to the imperfectly screened charges at the ferroelectric/dielectric interface, an asymmetry in the band diagram for opposite polarization states is achieved. The novelty of this MFIM stack was proposed and proven first by Meyer *et al.* in 2004 as a ferroresistive RAM cell [17]. We have adapted this concept to the HfO_2/ZrO_2 ferroelectric material family, which can enable another potent memory cell in the future. The main drawback of this stack design is the deliberate introduction of the depolarization field As a consequence, the retention of the device gets worse. But by implementing different metal work function, the retention behavior can be enhanced again to retain the memory window after 10 years [18]. Potential applications in a memory array with different selector devices are discussed elsewhere [19]–[20]. The fundamental operation principle for both polarization states is shown in the band diagrams in Fig. 1a) and b). The corresponding I-V curve for both polarization states P_{up} and P_{down} are shown in Fig. 1c) revealing the memory window with an on/off ratio of about 10. In Table 1 the parameters for the band diagram simulation are given.

II. SAMPLE DESCRIPTION AND EXPERIMENTAL DETAILS

Our TiN/$Hf_{0.5}Zr_{0.5}O_2$/Al_2O_3/TiN metal-ferroelectric-insulator-metal samples were deposited directly on a p-doped silicon wafer. The 12 nm thick TiN bottom electrode was sputtered at room temperature using a physical vapor deposition (PVD) process. Atomic layer deposition (ALD) in an Oxford ALD tool was used to grow the HZO layer (1:1 ratio of TEMA-Hf and TEMA-Zr precursor pulses, water as oxygen source) and the aluminum oxide layer (TMA and water) at 260 °C directly on the TiN bottom electrode. The TiN top electrode (12 nm) was sputtered on top using the same process conditions as for the bottom electrode. Afterwards a post-deposition anneal at 600 °C for 20 s in nitrogen atmosphere was done to crystallize the HZO into the ferroelectric phase. Circular capacitor structures were formed by Ti/Pt evaporation through a shadow mask (200 µm diameter) and subsequent SC1 etching of the underlying TiN top electrode. Polarization-voltage measurements were performed on an Aixacct TF3000 Analyzer, using triangular voltage pulses with a frequency of 10 kHz. The current-voltage response of the FTJ was analyzed with a Keithley 4200 SCS on a semi-automatic Cascade probe station with pulsed measurement units for voltage and current sensing.

TABLE 1. **Parameters for the band diagrams of the ferroelectric tunnel junction.**

Symbol	Quantity	Value
d_{FE}	Thickness $Hf_{0.5}Zr_{0.5}O_2$	12 nm
d_{DE}	Thickness Al_2O_3	1 nm
P_r	Remanent polarization	20 µC cm^{-2}
ε_{FE}	Relative permittivity $Hf_{0.5}Zr_{0.5}O_2$	32
ε_{DE}	Relative permittivity Al_2O_3	9
$E_{g,FE}$	Band gap $Hf_{0.5}Zr_{0.5}O_2$	5.75 eV
$E_{g,DE}$	Band Gap Al_2O_3	8.7 eV
χ_{FE}	Electron affinity $Hf_{0.5}Zr_{0.5}O_2$	2.7 eV
χ_{DE}	Electron affinity Al_2O_3	1.35 eV
$W_{F,TiN}$	TiN work function	4.45 eV
V_{bias}	External voltage bias (read voltage)	2 V

III. RESULTS AND DISCUSSION

For fabrication of our ferroelectric HZO layer in the MFIM stack we are using an optimized process that is described in [21]. An important attribute of thin hafnia based ferroelectric films is the polycrystalline nature. After the thermal anneal during sample preparation, the typical grain size inside the ferroelectric layer films is in the range of about 10-30 nm [20]. Since we are using comparably large capacitor areas, this leads to a high number of different grains and domains in the whole layer [22]. The polycrystallinity has profound effects on the different applications using ferroelectric HfO_2, such as negative capacitance [23] and single-domain switching effects in ferroelectric field effect transistors [24]. Typically these grains have a certain distribution for the domain orientation, coercive switching field and remanent polarization, which also depends on the kind of dopant or composition and the grain size itself [25]–[27]. This is reflected in the typical current-voltage and polarization-voltage curves that show broader switching peaks and a tilted hysteresis curve.

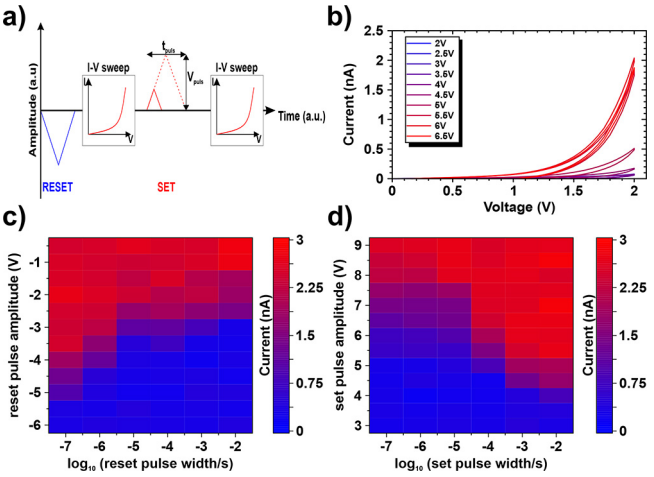

FIGURE 2. Set and reset operation of an HZO-based ferroelectric tunnel junction. a) waveform used for setting the reference state and assessing the stored memory state, b) increase of the on-state current with higher set amplitudes, c)+d) color-coded read current depending on reset (left) and set (right) pulse amplitude and pulse width.

In order to store two different states inside the ferroelectric layer through the remanent polarization, a high switching voltage has to be applied to the capacitor electrodes in order to drive the polarization into the saturated state. The amplitude of this switching voltage not only depends on the HZO thickness, but also on the Al_2O_3 thickness [28]. Additionally, there is only a certain thickness window for the HZO and the aluminum oxide where the ferroelectric tunnel junction is operational, which sets the minimum and maximum for the required voltages [28]. We have found that through the polycrystalline nature of our HZO film, a multi-level data storage is possible. In Fig. 2a the measurement waveform for the assessment of the set operation is shown (equivalent for reset by changing the voltages polarities). The ferroelectric tunnel junction is always reset into the P_{down} state (off-state) with a fixed amplitude of -6 V. After this reset an I-V sweep from 0 V to 2 V is measured to obtain the whole I-V response curve, which shows a low tunneling current corresponding to the off-state of the device. The set operation is done using a triangular voltage pulse with different amplitudes V_{puls} and pulse widths t_{puls}, while keeping the slope dV/dt constant. The constant slope of the voltage pulse leads to constant dielectric displacement currents through the device which in turn makes assessment of the polarization switching current easier (see Fig. 3). In Fig. 2b the tunneling current vs. readout voltage of the FTJ is shown for different switching amplitudes (t_{puls} is in the µs-range; please note here that we also changed the pulse width proportionally to keep the same ramp rate). It can be seen that for small set amplitudes, the ferroelectric is not switching and the read-current remains very low and is not distinguishable from the off-state current. Only when increasing the set amplitude to higher values, an increase of the memory window is visible. As we increase V_{puls} and reach the minimum coercive field, ferroelectric domains start to switch into the opposite state and contribute to a higher tunneling current. After 6 V are applied to the device, all domains have switched orientation and the tunneling on-state current cannot increase further. The I-V curve is now clearly different from the off current giving rise to the desired two-state memory operation. It is known from ferroelectric switching that there is no single, well-defined coercive field for a ferroelectric film but also a strong dependency on the time during which the electric field is applied [29]. For polycrystalline ferroelectrics, a nucleation-limited model is suitable to describe the polarization reversal in the randomly oriented grains. Here the polarization switching occurs due to the independent nucleation of ferroelectric domains in different regions across the whole capacitor area [30]. As shown before for thin polycrystalline films this leads to a broad distribution over a couple of decades for the nucleation time [31]. The same effect can be seen here for the switching kinetics of our ferroelectric tunnel junctions. In Fig. 2c and 2d, the tunneling current is shown color-coded as a function of the switching amplitude and switching pulse width. These measurements have been performed on FTJ's with 12 nm HZO thickness and 2 nm Al_2O_3 thickness. A clear trade-off between the necessary switching amplitude and the switching speed is visible in the two dimensional plot. For the set operation, a minimum switching voltage of 4 V is needed to obtain a significant memory window between on- and off-state, independent on the time length that the pulse was applied for. At lower voltages, the electric field across the HZO layer is not high enough to reverse the polarization. If the pulse length is reduced the set amplitude needs to increase in order to switch the same fraction of ferroelectric domains. For 100 ns pulse width the amplitude has to be around 8 V for a maximum on current. For the reset operation a very similar trend can be observed. The only difference is the highest absolute voltage that is needed for complete polarization reversal due a shift of the hysteresis curve to higher voltages. This internal bias field that is responsible for this imprint effect is likely related to fixed charges at the HZO/Al_2O_3 interface which have been observed before [32]–[33].

To further increase the memory density of ferroelectric tunnel junctions or utilize the device in neuromorphic computing, multi-level data storage within one capacitor can be beneficial. To achieve this we can utilize the total memory window of our devices (on/off ratio of ~10) to set intermediate current levels. The overall tunneling resistance can be influenced by applying the appropriate set pulse amplitude and pulse width. For the following results the pulse width was fixed at 1 ms (at 4V) and was only proportionally changed to obtain a constant slope of the triangular signal. The ferroelectric response in Fig. 3a shows the total switching current when a set operation with varying amplitude was performed. It is evident that with a higher voltage the total amount of switched domains inside the HZO layer increases. When the device is reset back to the reference state, the current increment is also visible on the negative hysteresis branch. In Fig. 3c the read-out current is shown

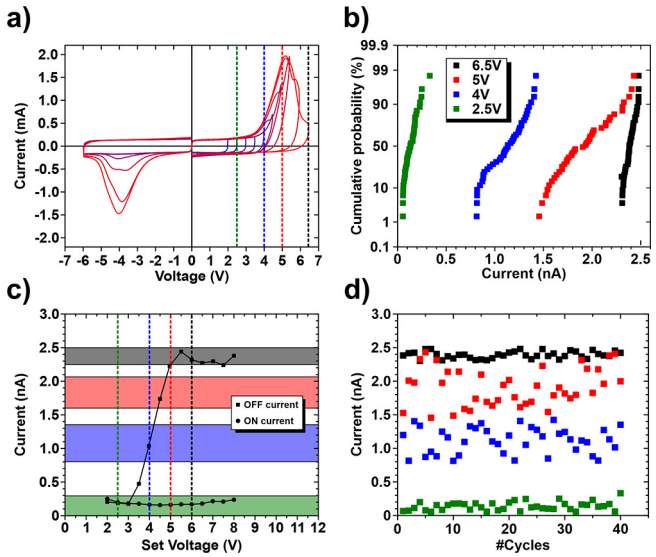

FIGURE 3. **Utilizing intermediate current states for multi-level memory function. a) current-voltage response from setting both polarization states, dashed lines indicate the different voltages used for setting the P_{up} state, b) cumulative probability plot for the cycle-to-cycle variability, c) dependency of off- and on-state current at 2 V read voltage for different set voltages, d) 4 different current levels measured over 40 switching cycles.**

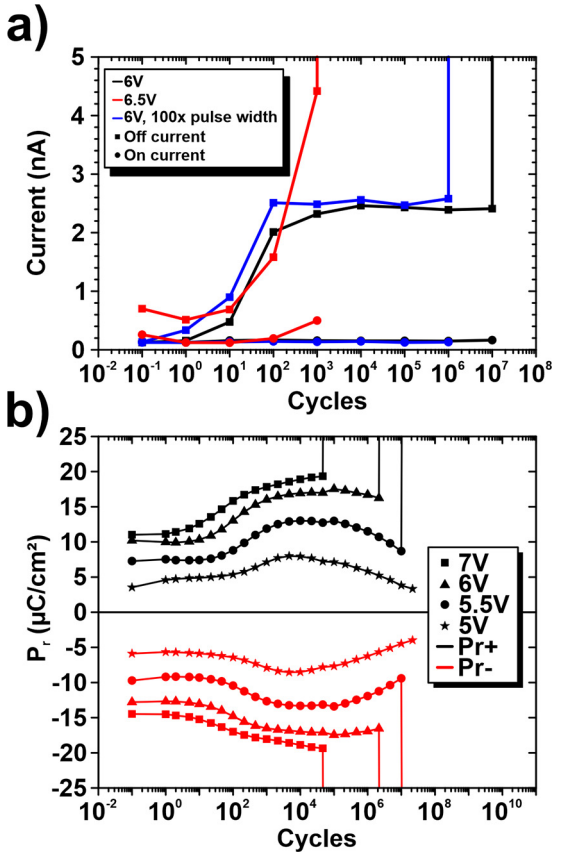

FIGURE 4. **a) off- and on-state current endurance characteristics measured up to 10^7 cycles for different switching pulse amplitudes/widths, b) endurance characteristics of the remanent polarization from the HZO/Al_2O_3 double-layer showing wake-up and fatigue for different amplitudes.**

depending on the set voltage amplitude. For four different set voltages 2.5 V, 4 V, 5 V and 6.5 V different current level can be written into the FTJ, which are marked green (lowest current, off state), blue, red and black (highest current, on state), respectively. In Fig. 3d the cycling stability of these intermediate levels are shown for 50 total switching cycles. The device was reset into the off-state after each measurement before the next cycle with the desired set amplitude. For a set voltage of 2.5 V no current increase is visible. The device remains in the off-state and no ferroelectric domain reversal takes place. This "on" current at about 0.2 nA is the same as the off current and corresponds to the same memory state (green dots). This state is very stable over a high number of switching cycles. The same can be said for the highest amplitude, where all domains switch and the highest tunneling current can be achieved (black dots). Again this state is very stable at 2.5 nA over 40 switching cycles. When applying the intermediate set amplitudes, only a fraction of domains will reverse their orientation and contribute to the higher tunneling current. The total current is therefore a combination of the low current from non-switched domains and higher current from already-switched domains. The fraction can be tuned by the corresponding voltage. Since the switching process at the coercive voltage is stochastic and non-deterministic as shown in [28], [34], the variation in the number of switched domains is rather large. Due to the broadness of the ferroelectric current switching peak as well as small shifts of the whole curve due to trapped charges/internal bias fields, the same external voltage may switch a slightly different number of domains, which then results in a variation of the tunneling current at the same set voltage. The sequence of setting the same intermediate state over 50 cycles shows this behavior as a broad current band. The cumulative probability of the corresponding current levels in Fig. 3b shows a low cycle-to-cycle variability for the minimum and maximum off-and on-state currents with high reproducibility. The other two intermediate states show a broader distribution, where especially for the 5 V set amplitude an overlap with the high current state (6 V set amplitude) leads to indistinguishable current sensing.

To further investigate the feasibility of our ferroelectric tunnel junctions, endurance and retention properties were characterized as they are important features of memory devices. A high endurance is needed for high write/rewrite cycles, while long retention is crucial for 10 year memory storage function. The retention properties of these devices and advancements/limits have been discussed elsewhere [27], [35]. Hafnium oxide based ferroelectric memories are known to suffer from wake-up and fatigue of the ferroelectric polarization with electric field cycling. Currently a strong research focus is on increasing the number of switching cycles while maintaining the memory window at all stages [36]–[37]. The endurance properties of our FTJ TiN/HZO/Al_2O_3/TiN structures are shown in

Fig. 4a. The current that is sensed after the very first polarization set/reset operation (10^{-1} = pristine) is equal for both on- and off-state. Only when switching the device back and forth between P_{up} and P_{down}, the on-current starts to increase with higher cycling numbers, while the off current remains at about 0.25 nA. After about 10^2 cycles the maximum on-state current is reached and is stable for up to 10^6 or 10^7 cycles until a hard breakdown of the device occurs. The maximum number of cycles is dependent on the used set voltage amplitude. When applying 6 V the device breaks down after 10^7 cycles, with 6.5 V after 10^6 cycles. An increase of the pulse width to 100 ms at 6 V shows that the device can also reach the maximum current of 2.5 nA already after 100 polarization switching cycles. The increase for both on and off current after 10^3 cycles is due to higher leakage current through the whole device, which is the result of the high stressing voltage/time leading to the creation of defects in the ferroelectric layer. The measurement of the ferroelectric polarization as a function of the number of switching cycles is shown in Fig. 4b for different voltages. It is known that lower voltages lead to higher endurance of ferroelectric memories, but at the same time decrease the memory window as the highest reachable remanent polarization is lower. By applying 5 V the maximum P_r value is about 6 μCcm^{-2} reaching an endurance of roughly 10^8 cycles. An increase of the voltage to 7 V results in a P_r value of 20 μCcm^{-2} but limited cycling stability only up to $4{\cdot}10^4$ cycles. Higher voltages induce more electric field stress in the ferroelectric layer which increases the defect/trap generation, leading to an earlier breakdown of the ferroelectric layer. The reason for the strong wake-up effect, which is not found in the reference TiN/HZO/TiN capacitor [21], [28], is the additional dielectric Al_2O_3 layer. In the symmetrical reference structure, which was used to investigate the ferroelectric properties of the hafnia layer, almost no wakeup or fatigue is seen. Due to the optimized process for the HZO deposition the non-ferroelectric interfaces at the electrodes, the defect generation and the monoclinic/tetragonal phase fractions are all reduced, leading to good ferroelectric performance. When the dielectric Al_2O_3 layer is introduced, the capacitive voltage divider leads to a higher required voltage for ferroelectric switching. As a new step in the deposition process is introduced, more defects in the HZO can be generated, which are the reason for the wake-up effect seen in the MIFM structures. Furthermore, the Al_2O_3 layer will lead to increased depolarization fields in the HZO layer. Also it is assumed that at the newly formed HZO/Al_2O_3 interface injected charges contribute to shift and degradation of the remanent polarization. The increased stress conditions increase the leakage current, defect generation and promote earlier breakdown of the devices, leading to fatigue after 10^4 cycles.

The correlation between the evolution of the remanent polarization and the tunneling current is evident when comparing the Fig. 4a and 4b. As the polarization increases, domain de-pinning and charge redistribution inside the HZO layer take place leading to a higher number of domains contributing to the remanent polarization value. This also leads to a higher tunneling current value for the on-state. As the polarization stays stable after wake-up, the maximum on-state current is sensed. The breakdown of the device for a programming voltage of 6 V occurs after roughly 10^6 cycles when the leakage current dominates. Through additional interface engineering, e.g., by substituting the Al_2O_3 layer with a different dielectric, the endurance properties might be optimized for less or even no wake-up or fatigue region.

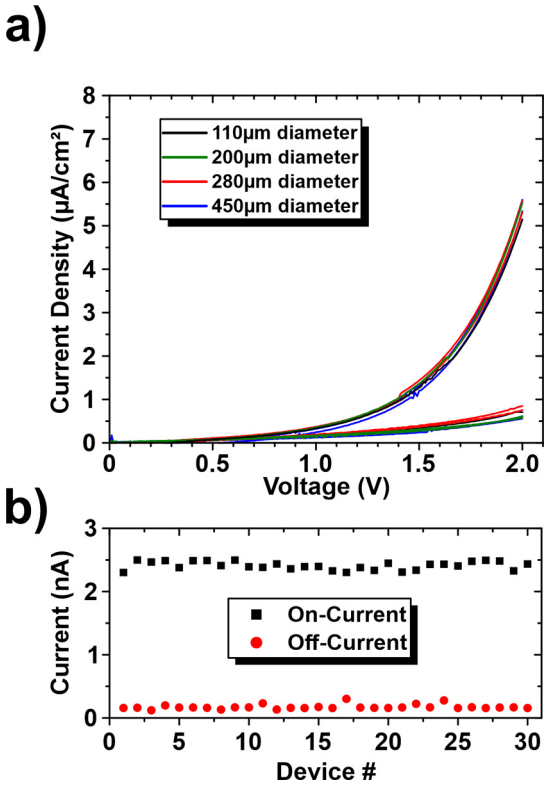

FIGURE 5. a) Current density vs. voltage for different capacitor areas revealing the scalability of the TiN/12nm HZO/2nm Al_2O_3/TiN device, b) off- and on-state current for 30 different devices showing good reproducibility.

The scalability and reproducibility of the FTJ with 12 nm thick HZO and 2 nm Al_2O_3 can be inferred from Fig. 5a and 5b. The I-V sweeps for tunneling current sensing were measured on different capacitors with different areas. In Fig. 5a the current density vs. voltage is shown. All curves are overlapping showing that the on- and the off-state current are proportionally scaling with the area of the device. The same memory characterization measurements have also been carried out on multiple capacitors with identical areas, showing very good reproducibility as shown in Fig. 5b.

IV. CONCLUSION

We have investigated ferroelectric tunnel junctions that utilize a ferroelectric HZO film as the memory layer and

a dielectric Al_2O_3 layer that serves as the tunneling barrier for the current through the device. Through polarization reversal in the HZO layer the band diagram is changed asymmetrically which enables the two different tunneling electroresistances for both opposite polarization states. By applying different set and reset amplitudes with varying pulse widths the current through the device can be tuned into different levels between the maximum on and the minimum off current. Since the domain reversal in thin ferroelectric film is a stochastic process (due to the polycrystalline nature) when voltages close to the coercive field are applied, a rather large range in the intermediate current levels is present, while the off- and on-state current show only a small spread over 50 switching cycles. The endurance behavior of the FTJ with a strong on-state current increase during the first 100 switching cycles can be directly connected to the wake-up behavior of the HZO layer. Although only small wake-up is present in reference TiN/HZO/TiN layers, the addition of the dielectric Al_2O_3 layer introduces additional defects, interface charges and depolarization fields which lead to the pronounced wake-up effect. Due to the depinning of domains and redistribution of defects/trapped charges during cycling the remanent polarization of the ferroelectric layer increases, which in turn leads to higher tunneling currents through our memory device until the device suffers from hard breakdown after 10^6-10^7 cycles. Although the absolute currents are still quite low we could show that the normalized current scales proportional to the capacitor area as expected from a uniform current over the device. Finally the reproducibility on different samples was confirmed.

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REFERENCES

[1] R. Aitken, V. Chandra, J. Myers, B. Sandhu, L. Shifren, and G. Yeric, "Device and technology implications of the Internet of Things," in *Proc. Symp. VLSI Technol.*, 2014. doi: 10.1109/VLSIT.2014.6894339 .

[2] S. Yin and O. Kaynak, "Big data for modern industry: Challenges and trends," *Proc. IEEE*, vol. 103, no. 2, pp. 143–146, Feb. 2015. doi: 10.1109/JPROC.2015.2388958.

[3] P. Ranganathan and J. Chang, "(Re)designing data-centric data centers," *IEEE Micro*, vol. 32, no. 1, pp. 66–70, Jan./Feb. 2012. doi: 10.1109/MM.2012.3.

[4] Y. Lu *et al.*, "Fully functional perpendicular STT-MRAM macro embedded in 40 nm logic for energy-efficient IOT applications," in *Proc. IEEE Int. Electron Devices Meeeing (IEDM)*, Washington, DC, USA, 2015. doi: 10.1109/IEDM.2015.7409770.

[5] M. Qureshi, V. Srinivasan, and J. A. Rivers, "Scalable high performance main memory system using phase-change memory technology," in *Proc. 36th Annu. Int. Symp. Comput. Archit.*, 2009, pp. 24–33. doi: 10.1145/1555815.1555760.

[6] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories—Nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, nos. 25–26, pp. 2632–2663, 2009. doi: 10.1002/adma.200900375.

[7] S. Dünkel *et al.*, "A FeFET based super-low-power ultra-fast embedded NVM technology for 22nm FDSOI and beyond," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2017. doi: 10.1109/IEDM.2017.8268425.

[8] J. Müller *et al.*, "High endurance strategies for hafnium oxide based ferroelectric field effect transistor," in *Proc. 16th Non Volatile Memory Technol. Symp. (NVMTS)*, 2016. doi: 10.1109/NVMTS.2016.7781517.

[9] J. Müller, P. Polakowski, S. Müller, and T. Mikolajick, "Ferroelectric hafnium oxide based materials and devices: Assessment of current status and future prospects," *ECS J. Solid-State Sci. Technol.*, vol. 4, no. 5, pp. N30–N35, 2015. doi: 10.1149/2.0081505jss.

[10] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and T. Mikolajick, "Ferroelectricity in hafnium oxide thin films," *Appl. Phys. Lett.*, vol. 99, no. 10, 2011, Art. no. 102903. doi: 10.1063/1.3634052.

[11] E.T. Breyer, H. Mulaosmanovic, T. Mikolajick, and S. Slesazeck, "Reconfigurable NAND/NOR logic gates in 28 nm HKMG and 22 nm FD-SOI FeFET technology," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2017. doi: 10.1109/IEDM.2017.8268471.

[12] M. Hoffmann *et al.*, "Unveiling the double-well energy landscape in a ferroelectric layer," *Nature*, vol. 565, pp. 464–467, Jan. 2019. doi: 10.1038/s41586-018-0854-z.

[13] H. Mulaosmanovic, E. Chicca, M. Bertele, T. Mikolajick, and S. Slesazeck, "Mimicking biological neurons with a nanoscale ferroelectric transistor," *Nanoscale*, vol. 10, pp. 21755–21763, Nov. 2018. doi: 10.1039/C8NR07135G.

[14] E. Y. Tsymbal and A. Gruverman, "Beyond the barrier," *Nat. Mater.*, vol. 12, pp. 602–604, May 2013. doi: 10.1038/nmat3669.

[15] A. Chanthbouala *et al.*, "Solid-state memories based on ferroelectric tunnel junctions," *Nat. Nanotechnol.*, vol. 7, pp. 101–104, 2012. doi: 10.1038/nnano.2011.213.

[16] S. Fujii, Y. Kamimuta, T. Ino, Y. Nagasaki, R. Takaishi, and M. Saitoh, "First demonstration and performance improvement of ferroelectric HfO_2-based resistive switch with low operation current and intrinsic diode property," in *Proc. IEEE Symp. VLSI Technol.*, 2016. doi: 10.1109/VLSIT.2016.7573413.

[17] R. Meyer, J. R. Contreras, A. Petraru, and H. Kohlstedt, "On a novel Ferro resistive random access memory (FRRAM): Basic model and first experiments," *Integr. Ferroelect.*, vol. 64, no. 1, pp. 77–88, 2004. doi: 10.1080/10584580490893655.

[18] B. Max, T. Mikolajick, M. Hoffmann, S. Slesazeck, and T. Mikolajick, "Retention characteristics of $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric tunnel junctions," in *Proc. Int. Memory Workshop (IMW)*, 2019. doi: 10.1109/IMW.2019.8739765.

[19] S. Slesazeck and T. Mikolajick, "Nanoscale resistive switching memory devices: A review," *Nanotechnology*, vol. 30, no. 35, 2019, Art. no. 352003. doi: 10.1088/1361-6528/ab2084.

[20] S. Slesazeck *et al.*, "Uniting the trinity of ferroelectric HfO_2 memory devices in a single memory cell," in *Proc. Int. Memory Workshop (IMW)*, 2019. doi: 10.1109/IMW.2019.8739742.

[21] T. Mittmann, F. P.G. Fengler, C. Richter, M. H. Park, T. Mikolajick, and U. Schröder, "Optimizing process conditions for improved $Hf_{1-x}Zr_xO_2$ ferroelectric capacitor performance," *Microelectron. Eng.*, vol. 178, pp. 48–51, Jun. 2017. doi: 10.1016/j.mee.2017.04.031.

[22] M. Hoffmann *et al.*, "Stabilizing the ferroelectric phase in doped hafnium oxide," *J. Appl. Phys.*, vol. 118, no. 7, 2015, Art. no. 072006. doi: 10.1063/1.4927805.

[23] M. Hoffmann *et al.*, "Direct observation of negative capacitance in polycrystalline ferroelectric HfO_2," *Adv. Funct. Mater.*, vol. 26, no. 47, pp. 8643–8649, 2016. doi: 10.1002/adfm.201602869.

[24] H. Mulaosmanovic *et al.*, "Evidence of single domain switching in hafnium oxide based FeFETs: Enabler for multi-level FeFET memory cells," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2015. doi: 10.1109/IEDM.2015.7409777.

[25] Y. Tan, "Unfolding grain size effects in barium titanate ferroelectric ceramics," *Sci. Rep.*, vol. 5, May 2015, Art. no. 9953. doi: 10.1038/srep09953.

[26] A. Gruverman and Y. Ikeda, "Characterization and control of domain structure in $SrBi_2Ta_2O_9$ thin films by scanning force microscopy," *Jpn. J. Appl. Phys.*, vol. 37, 1998, Art. no. L939. doi: 10.1143/JJAP.37.L939.

[27] M. Hoffmann *et al.*, "Ferroelectric phase transitions in nanoscale HfO_2 films enable giant pyroelectric energy conversion and highly efficient supercapacitors," *Nano Energy*, vol. 18, pp. 154–164, Nov. 2015. doi: 10.1016/j.nanoen.2015.10.005.

[28] B. Max, M. Hoffmann, S. Slesazeck, and T. Mikolajick, "Ferroelectric tunnel junctions based on ferroelectric-dielectric $Hf_{0.5}Zr_{0.5}.O_2/A1_2O_3$ capacitor stacks," in *Proc. 48th Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2018. doi: 10.1109/ESSDERC.2018.8486882.
[29] H. Mulaosmanovic *et al.*, "Switching kinetics in nanoscale hafnium oxide based ferroelectric field-effect transistors," *ACS Appl. Mater. Interfaces*, vol. 9, pp. 3792–3798, Jan. 2017. doi: 10.1021/acsami.6b13866.
[30] S. D. Hyun *et al.*, "Dispersion in ferroelectric switching performance of polycrystalline $Hf_{0.5}Zr_{0.5}O_2$ thin films," *ACS Appl. Mater. Interfaces*, vol. 10, pp. 35374–35384, Sep. 2018. doi: 10.1021/acsami.8b13173.
[31] A. K. Tagantsev, I. Stolichnov, N. Setter, J. S. Cross, and M. Tsukada, "Non-Kolmogorov–Avrami switching kinetics in ferroelectric thin films," *Phys. Rev. E, Stat. Phys. Plasmas Fluids Relat. Interdiscip. Top.*, vol. 66, Dec. 2002, Art. no. 214109. doi: 10.1103/PhysRevB.66.214109.
[32] D. K. Simon, P. M. Jordan, T. Mikolajick, and I. Dirnstorfer, "On the control of the fixed charge densities in Al_2O_3-based silicon surface passivation schemes," *ACS Appl. Mater. Interfaces*, vol. 7, pp. 28215–28222, Nov. 2015. doi: 10.1021/acsami.5b06606.
[33] M. Hoffmann, B. Max, T. Mittmann, U. Schroeder, S. Slesazeck, and T. Mikolajick, "Demonstration of high-speed hysteresis-free negative capacitance in ferroelectric $Hf_{0.5}Zr_{0.5}O_2$," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2018. doi: 10.1109/IEDM.2018.8614677.
[34] Y.-H. Shin, I. Grinberg, I-W. Chen, and A. M. Rappe, "Nucleation and growth mechanism of ferroelectric domain-wall motion," *Nature*, vol. 449, pp. 881–884, Oct. 2007. doi: 10.1038/nature06165.
[35] B. Max, M. Hoffmann, S. Slesazeck, and T. Mikolajick, "Retention characteristics of $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric tunnel junctions," in *Proc. Int. Memory Workshop (IMW)*, 2019.
[36] U. Schröder *et al.*, "Lanthanum-doped hafnium oxide: A robust ferroelectric material," *Inorganic Chem.*, vol. 57, pp. 2752–2765, Feb. 2018. doi: 10.1021/acs.inorgchem.7b03149.
[37] F. P. G. Fengler *et al.*, "Analysis of performance instabilities of Hafnia-based ferroelectrics using modulus spectroscopy and thermally stimulated depolarization currents," *Adv. Elect. Mater.*, vol. 4, no. 3, 2018, Art. no. 1700547. doi: 10.1002/aelm.201700547.

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