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A Novel p-LDMOS Additionally Conducting Electrons by Control ICs

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ABSTRACT A silicon-on-insulator (SOI) p-channel lateral double-diffused MOSFET (p-LDMOS), conducting not only holes but also electrons, is proposed and investigated by TCAD simulations. Its most important advantage is the greatly improved relationship between the breakdown voltage (BV) and the specific on-resistance ($R_{on,sp}$). The improvement is mainly attributed to two aspects. First, many holes can accumulate in the p-drift region in the on-state, which provides a low-resistance path for hole conduction. Second, a paralleled n-LDMOS is, meanwhile, automatically triggered to form a new path for electrons. Electrons have higher mobility than holes; thus, the device performance is further improved. Based on a simulation comparison with the previous p-LDMOS at the same BV of 300 V, the $R_{on,sp}$ of the proposed p-LDMOS decreased by 78% and the figure of merit (FOM) increased approximately 3.4 times. Moreover, the proposed device still has the conventional three-terminal style, and its fabrication process is compatible with CMOS technology.

INDEX TERMS High-side switch, power MOSFET, silicon-on-insulator.

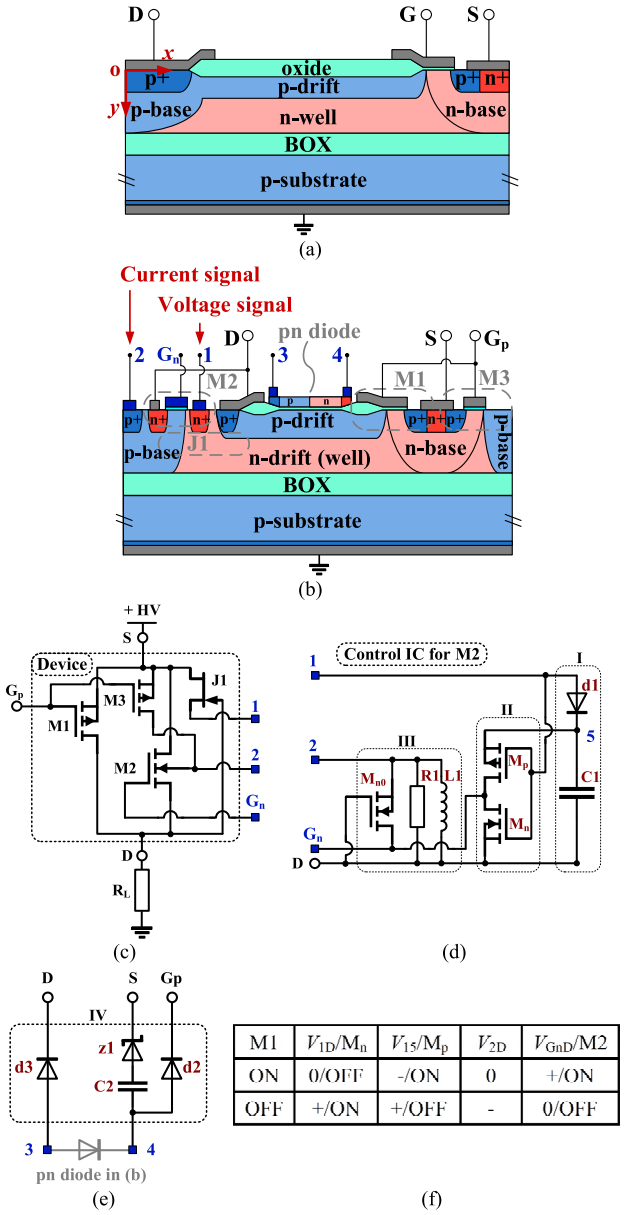
I. INTRODUCTION

The p-channel lateral double-diffused MOSFET (LDMOS) fabricated in silicon-on-insulator (SOI) has been widely used as a high-side power switch [1]–[3]. However, under the same requirement of breakdown voltage (BV), a p-LDMOS usually has a larger specific on-resistance ($R_{on,sp}$) than an n-LDMOS. To address this problem, many structures such as the "double hole-conductive paths" and the "dual-channels for holes and electrons" have been proposed [4]–[7]. The effective utilization of electrons with high mobility in the "dual-channels for holes and electrons" leads to a smaller $R_{on,sp}$ than in the "double hole-conductive paths". However, to synchronously control the dual-channels for holes and electrons, normally the device should be four-terminal style. Moreover, in the high-side application, the reference potential for the n-channel gate floats from the highest voltage to the ground voltage, which complicates the driving circuits.

In this paper, a p-LDMOS with a paralleled, self-biased n-channel gate is proposed and investigated by TCAD simulations. It exhibits significantly improved performance and has the conventional three-terminal style. To achieve the simultaneous conductions for both holes and electrons, the proposed structure evolves from a previous p-LDMOS [8] for the acquirements of a voltage signal and a current signal. Compared with the previous works in this area [5]–[7], a different structure is utilized for a different method to control the n-channel gate in this work. The mechanism will be detailed in the following, and it should be noticed that only simulation results, no experimental results, are included.

II. DEVICE STRUCTURE AND MECHANISM

Device structures of the previous SOI p-LDMOS and the proposed device are schematically shown in Fig. 1(a) and (b), respectively. The proposed structure features three major differences. First, an n-LDMOS (M2) is added on the left side, whose control gate is G_n. Second, a pn junction is added on the oxide, above the p-drift region. Third, the other p-MOSFET (M3), also controlled by G_p, is added on the right side. In the figure, J1 is a parasitic n-channel JFET, composed of the left-side p-base, the n-drift and the p-drift. The equivalent circuit is illustrated in Fig. 1(c). M3 is connected to node 2, and the reason is that, in Fig. 1(b), the



M1	V_{1D}/M_n	V_{15}/M_p	V_{2D}	V_{GnD}/M2
ON	0/OFF	-/ON	0	+/ON
OFF	+/ON	+/OFF	-	0/OFF

FIGURE 1. (a) Previous SOI p-LDMOS. (b) Proposed device. (c) High-side equivalent circuit for the proposed device. (d) Control IC for n-LDMOS. (e) Circuit relevant to the formation of the hole accumulation layer. (f) Simplified voltage chart for the switching response, where "+" or "−" represents a positive or a negative bias.

n-drift, the BOX and the p-substrate forms a semiconductor-insulator-semiconductor (SIS) capacitor, when the proposed device turns on, both the source S and the drain D are positive with respective to the p-substrate, and a hole inversion layer, as shown in Fig. 2, is consequently formed at the interface of n-drift/BOX, which connects two separated p-bases together. Relevant control integrated circuits (ICs) for the proposed device are illustrated in Fig. 1(d) and (e). The elements in Fig. 1(d) and (e) are not illustrated in the proposed device structure, although they can be integrated together. The pn diode in Fig. 1(e) is a symbol for the pn diode on the oxide

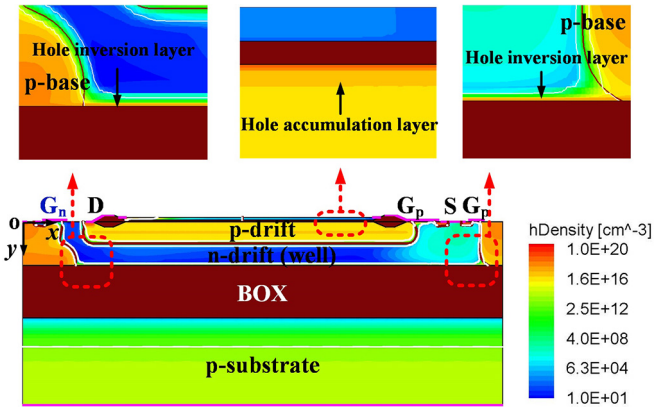


FIGURE 2. Distribution of hole concentration in the on-state of the proposed structure. HV = 250 V, V_{SD} = 1 V, V_{GpS} = −15 V, V_{GnD} = 10 V.

over the p-drift shown in Fig. 1(b). By utilizing a voltage signal and a current signal spontaneously generated in the device, the electron conduction is controlled automatically, and a simplified voltage chart for the switching response is illustrated in Fig. 1(f).

A. AUTOMATIC CONTROL FOR N-CHANNEL GATE

In Fig. 1(b), a voltage signal and a current signal are acquired from node 1 and node 2, respectively. When the proposed device turns off, V_{1D} increases with the increment of V_{SD} until the channel of J1 pinches off. Moreover, no current flows into node 2, since M3 turns off, and no hole inversion layer is formed at the interface of n-drift/BOX. When the device turns on, V_{1D} decreases to approximately 0 due to that node 1 is connected to the source S through the n-drift, which is approximately equipotential with the drain D. Simultaneously, a hole inversion layer is formed at the interface of n-drift/BOX, which connects two separated p-bases (on the right and left sides) together. Then, a hole current from the source can flow through M3, the hole inversion layer, and the left-side p-base, in sequence, and flow out from node 2. It indicates that a current signal could be detected by node 2 with the turn-on of M3. Therefore, when the device is in the OFF-state, there is a high-level voltage signal (V_{1D}) and a low-level current signal, and when the device is in the ON-state, the voltage signal (V_{1D}) and the current signal switch to a low-level and a high-level status, respectively. The "high-level" and the "low-level" are used to distinguish the relative values for signals in the ON and OFF states. These corresponding changes are shown in Fig. 1(f).

In Fig. 1(d), part I is a low-voltage supply for the control IC [9]. The capacitor C1 charges up, V_{5D} increasing, when the voltage signal is of high level ($V_{1D} > 0$). The current for charging C1 is from the source S, and flows into node 1, as shown in Fig. 3. As for a low-level voltage signal ($V_{1D} \approx 0$), the reversely-biased diode d1 prevents C1 from discharging itself, which is the reason for part I storing energy and providing power for the control IC. Part II is an inverter that

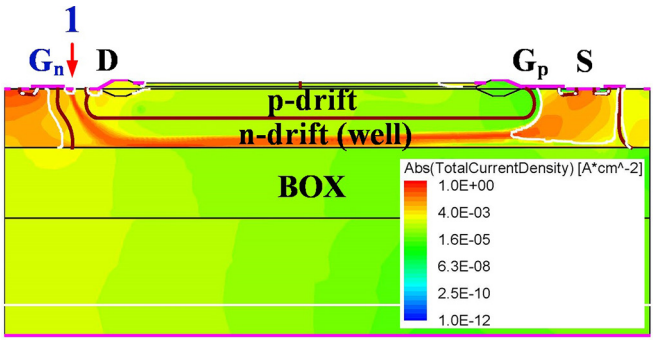


FIGURE 3. Distributions of current density in the OFF-state for the proposed device. HV = 250 V, V_{SD} = 1 V, V_{GpS} = V_{GnD} = 0.

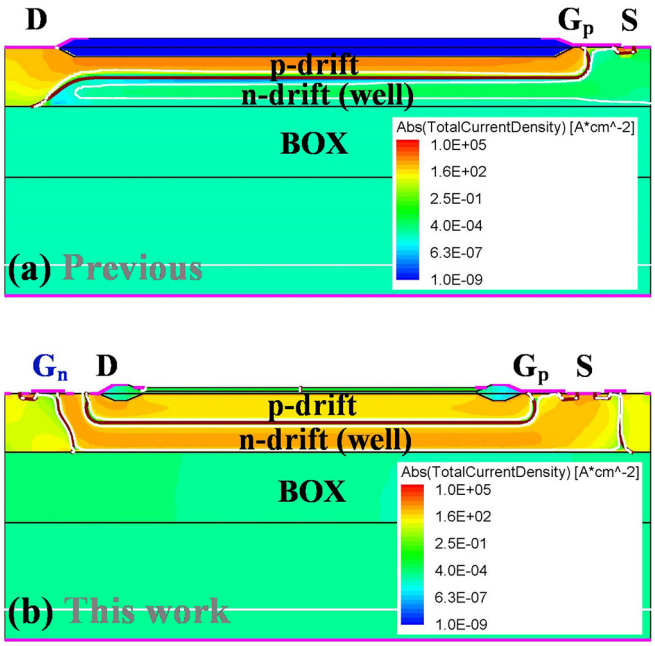


FIGURE 4. Distributions of current density in the ON-state of (a) the previous LDMOS and (b) the proposed device. HV = 250 V, V_{SD} = 1 V, V_{GpS} = −15 V, V_{GnD} = 10 V.

is controlled by the voltage signal (V_{1D}). In the OFF-state, M_n turns on for a high-level V_{1D} with a consequent turn-off of M_p. In the ON-state, V_{1D} is at a low level, and the switch states for M_n and M_p interchange. V_{GnD}, namely the output of the inverter, is approximately equal to the voltage of C1 (V_{5D}) in the ON-state, for M_p turning on to connect G_n to C1. The gate G_n is charged by C1, and n-LDMOS turns on. The device conducts both holes and electrons, as the current density illustrated in Fig. 4(b).

The device is not able to be turned off, with only the help of part I and II in the control IC. The electron current still flows from the source S to the drain D even the hole conduction paths (M1 and M3) are turned off. V_{1D} is unable to switch from the high level to the low level, because the turn-off of the hole conduction paths (M1 and M3) is unable to cause a significant increase in V_{SD} for a large electron current still flowing in the device. To address this problem, part III is in the control IC.

In the ON-state, a hole current is detected by node 2, which flows through the inductor L1 in part III. In the OFF-state, the hole current no longer flows into node 2. However, for the current continuity of L1, a voltage ($V_{2D} < 0$ V) is generated across R1, since L1 and R1 are in a return circuit. The effect is twofold: providing a negative substrate bias for M2 and switching on M_{n0} to discharge G_n. Both aim to decrease electron currents, and increase V_{SD}. A negative substrate bias increases the threshold voltage for M2. Consequently, V_{1D} switches to a high level for the inverter in part II, and M_n turns on to short the gate and source of M2. The output of part II $V_{GnD} = 0$, and M2 turns off.

B. FORMATION OF HOLE ACCUMULATION LAYER

In the ON-state, the drain D and the source S are approximately equipotential, and are positively biased with respect to the gate G_p. In Fig. 1(e), the diode d3 is reversely biased, while the pn diode and the diode d2 are almost zero biased, which means the potential of the pn diode is close to that of the gate G_p. In Fig. 1(b), there is a SIS capacitor composed of the pn diode, the p-drift and the oxide between them. The potential difference between the p-drift (connected to the drain D) and the pn diode, namely V_{DGp}, causes accumulated electrons (provided by the gate current) and holes (provided by the source S) in the pn diode and the p-drift region, respectively. The resistance of the hole-conductive path is reduced because there are more holes in the p-drift region, whose density is shown in Fig. 2.

In the OFF-state, in Fig. 1(e), with V_{SD} increasing, the pn diode changes its condition form zero bias to reverse bias, and accumulated electrons in the pn diode are forced by the electric field to move towards, and finally are stored on the capacitor C2. In the following switching period, when the device turns on, C2 would discharge itself, and, instead of the gate current, provides those aforementioned stored electrons for the SIS capacitor to induce a hole accumulation layer in the p-drift region. It is a transfer process of negative charges stored on C2 to the SIS capacitor, since the source S and the drain D are approximately equipotential, and there are different voltages of these two capacitors. However, by the method proposed in [10], during the first turn-on process, the gate current not only provides electrons for the SIS capacitor but also simultaneously charges C2, which means the device requires a large gate current. To eliminate this synchronous charging current for C2 in the total gate current, a Zener diode z1 is connected to C2 in series in this work. When $V_{GpS} < 0$ V, z1 sustains the voltage and stops the current from charging C2. The requirement for the BV of z1 is just $|V_{GpS}|$ in the on-state of the device.

III. RESULTS AND DISCUSSION

The proposed device is investigated by TCAD simulations. In the simulation, the thicknesses of the BOX and the SOI layer on it are 3 μm and 2.5 μm, respectively. The

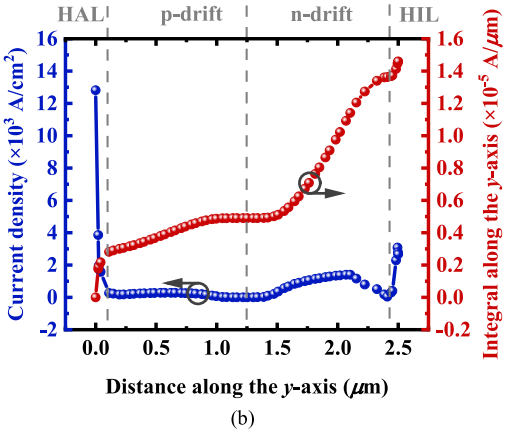


FIGURE 5. Distributions of the current density in the ON-state along the *y*-axis for the proposed device.

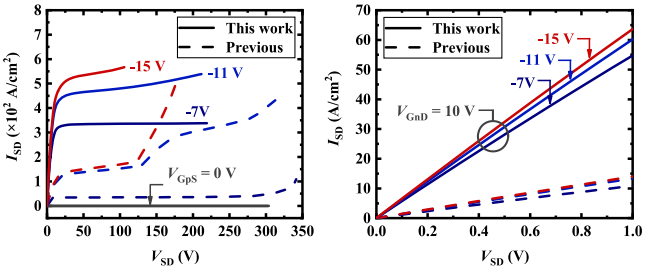


FIGURE 6. Comparison of simulated output characteristics (left) and partial enlarged detail of the linear region (right).

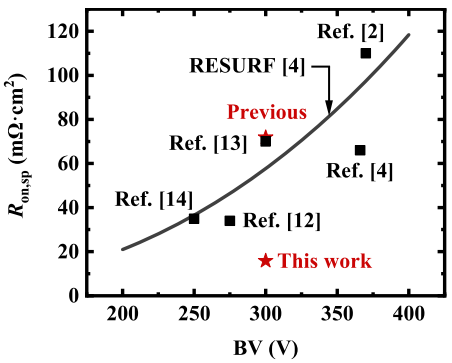


FIGURE 7. Comparison of $R_{on,sp}$ versus BV between the previous p-LDMOS and the proposed p-LDMOS. Reference [13] is a simulation study, while the other references use experimental results.

drift region length is 20 μm. The channel lengths of M1, M2 and M3 are 1.2 μm, 0.9 μm and 0.5 μm, respectively. The thickness of gate oxide is 100 nm. The width for the channel of the JFET (J1), namely the minimum width between the left-side p-base and the p-drift, is 1 μm. The doping concentration of the n-well, as well as the n-drift region, is 2.5×10^{16} cm^{-3}. The optimized doses of the p-drift region are 4.4×10^{12} cm^{-2} for the previous structure and 5.4×10^{12} cm^{-2} for the proposed one. The other values for passive components are $R1 = 10^8\ \Omega \cdot \mu$m, $L1 = 1\ \text{H} \cdot \mu$m, $C1 = 5 \times 10^{-15}$ F/μm, and $C2 = 10^{-14}$ F/μm. The main common physics models are incorporated in Synopsys Sentaurus TCAD simulations [11], including Mobility (DopingDep HighFieldSaturation Enormal), Effective Intrinsic Density (OldSlotboom), Recombination (SRH(DopingDep) Auger Avalanche(Okuto)), and corresponding SPICE models for elements in the circuits.

Fig. 4 compares the distributions of current density in the ON-state. For the previous device, there is no hole accumulation layer induced in the p-drift region. Moreover, although a hole inversion layer is formed at the bottom of the n-drift region, no conductive path connects it to the source and, hence, no hole currents flow through it. These two issues are addressed by the proposed device. In addition, due to the n-channel gate, the proposed device has a higher current density than the previous device in the n-well region.

Fig. 5 shows the contribution of each component to the total current. Through a simple calculation by integral, for the proposed device, it is obvious that the electron current in the n-drift makes the greatest contribution (approximately 58%) to the total current. The hole current in the p-drift and in the hole accumulation layer (HAL) both account for approximately 18% of the total current. The other 6% of the total current is the hole current flowing through the hole inversion layer (HIL) in the n-drift.

The comparison of output characteristics is shown in Fig. 6, which indicates an improved current capability obtained by the device proposed in this work. The n-channel gate voltage (V_{GnD}) of 10 V is automatically supplied by the internal IC in Fig. 1(e), and at $V_{\text{GpS}} = -15$ V, the proposed device has a $R_{\text{on,sp}}$ of 15.8 m$\Omega \cdot$cm^2 and an FOM ($= \text{BV}^2/R_{\text{on,sp}}$) of 5.7 MW/cm^2, which are 71.8 m$\Omega \cdot$cm^2 and 1.3 MW/cm^2 for the previous device, respectively. Specifically, the decrease in $R_{\text{on,sp}}$ is 78%, and the increase in FOM is 338%. Compared with the previous studies listed in Fig. 7, there is a significant improvement in the relationship between the BV and $R_{\text{on,sp}}$ in this work.

The above discussion does not include the area cost by the control IC, especially by the inductor that may require a large area. Taking the area of L1 into consideration for a simple estimation, the device is assumed to operate under the current density of 50 A/cm^2 at $I_{\text{DS}} = 10$ A, and the area of the device is 0.2 cm^2, which means the width of the device is approximately 7.3×10^5 μm (the length of each cell is 27.5 μm). The inductance of L1 for the proposed device is thus 1.375 μH. Refer to [15], a 20 μH/cm^2 is achieved, and the area cost by the inductor L1 is approximately 0.069 cm^2, which leads a small increase in $R_{\text{on,sp}}$ from 15.8 m$\Omega \cdot$cm^2 to 21.3 m$\Omega \cdot$cm^2.

Fig. 6 also indicates that the proposed device has a higher snapback voltage even at a larger current density. According to Poisson's equation, less net charges accounts for an even electric field profile with a high breakdown voltage. Compared with the previous structure, both holes and electrons participate in conducting electric current in the

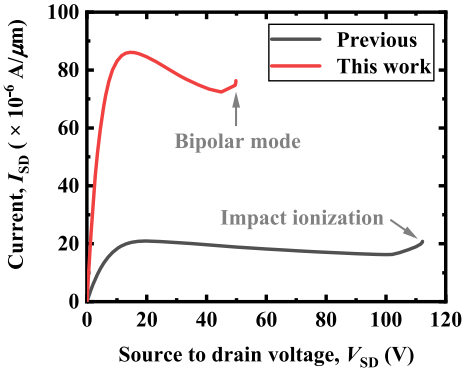


FIGURE 8. Thermal dynamic simulation of I_{SD}-V_{SD} for the previous LDMOS and the proposed structure at $V_{GpS} = -15$ V.

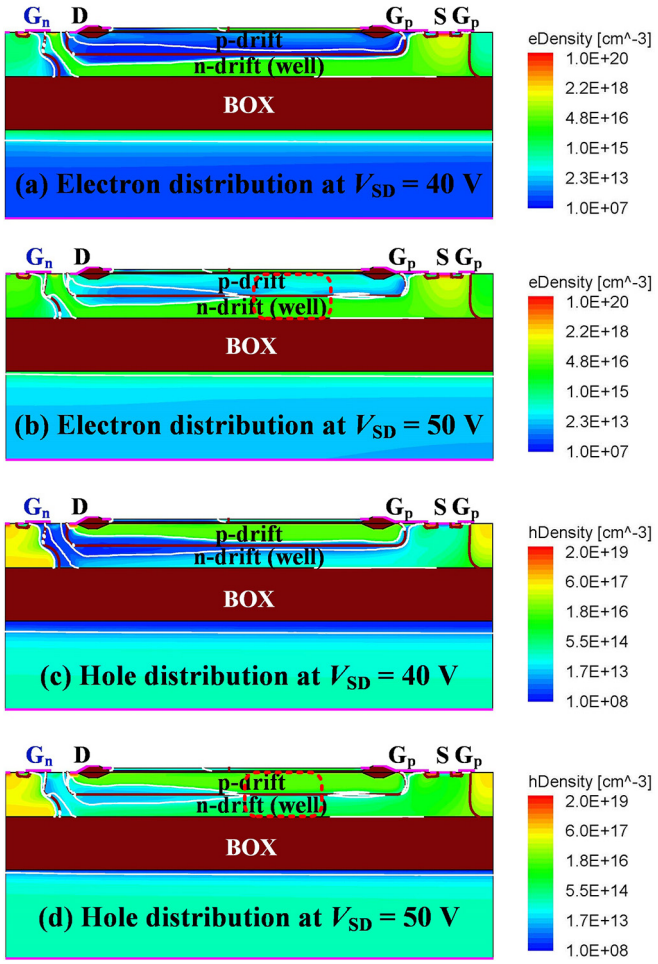


FIGURE 9. Distribution of electrons/holes (a)/(c) before and (b)/(d) after the turn-on of bipolar mode for the proposed device in the thermal dynamic simulation.

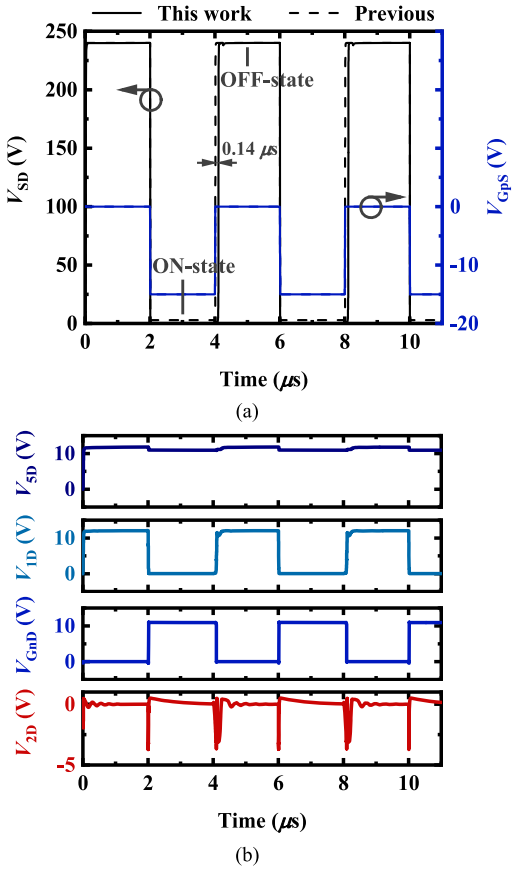


FIGURE 10. Transient simulation. (a) Switching waves. (b) Several voltage waves of relative importance for the proposed p-LDMOS.

proposed device, which decreases the net charges in the drift regions, hence there is a larger safe operating area.

In the proposed device, a parasitic PNP transistor is composed of the p-drift, the n-drift and the left-side p-base, which would turn on because of the self-heating effect. It should be noticed that before this case happens, there is only a unipolar mode in the proposed device, although both types of carriers conducting current. Fig. 8 shows the thermal dynamic simulation for the proposed device. For a high temperature, the lattice vibrates intensely, and the possibility of the lattice-vibration scattering increase. A large amount of scattering leads to a low mobility for carriers, which is the reason for a gradually decreased saturation current. The proposed device has a snapback voltage of approximately 45 V with a forward bias of the p-drift/n-drift junction, which means the bipolar mode turns on. This phenomenon has a close relationship with a narrowed bandgap and a high generation-recombination rate at high temperature. Due to the turn-on of the bipolar mode, the conductivity modulation between p-drift/n-drift reduces the resistance of the device and the snapback happens with an increase on the current.

Fig. 9 shows the distributions of electrons and holes in the proposed device. In Fig. 9(b) and (d), there are many minority carriers in both the p-drift and the n-drift because of the forward bias of the p-drift/n-drift junction, shown in red dashed circles, which can be identified by the boundary of the depletion region, white solid lines, and, meanwhile, indicates that the bipolar mode turn-on in the proposed device.

Fig. 10 shows the transient simulation of the proposed device. As shown by the switching waves in Fig. 10(a),

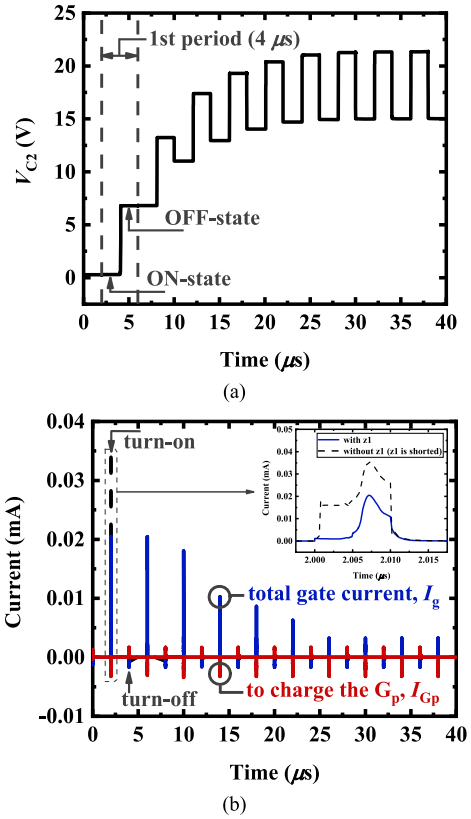


FIGURE 11. Variations in (a) the voltage of C2 and (b) the total gate current.

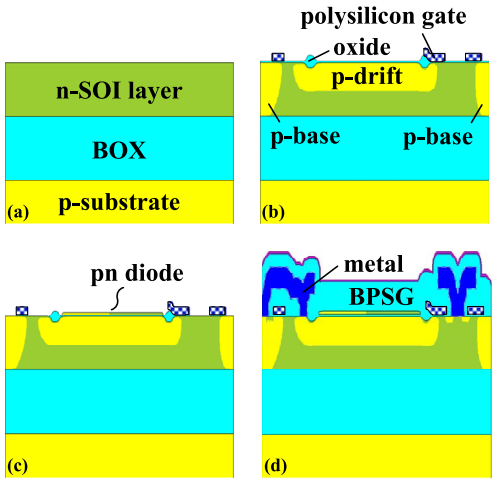


FIGURE 12. Key fabrication sequence of the proposed structure: (a) SOI wafer; (b) p-base and p-drift implantation and diffusion during oxidation, followed by polysilicon deposition and etching to form gate; (c) pn diode formation; (d) same steps as those of the previous structure, which are compatible with the mainstream CMOS technology.

the turn-off delay time for the proposed device is 0.14-μs longer than the turn-off delay time of the previous device because C1 and C2 charge up during the turn-off process. The synchronous variations, along with the switching waves, in the potentials of G_n and nodes 1, 2, and 5 are illustrated in Fig. 10(b). A low voltage of approximately 10 V (V_{5D}) provides a positive bias on the n-channel gate of M2 (V_{GnD}) for conducting electron currents, when V_{1D} is low level (0 V) and M_p turns on (for $V_{15} < 0$). To turn off M2, the peak value of the aforementioned negative substrate bias, namely V_{2D}, is approximately -4 V. The 2D structure plots of current density for the proposed device in the OFF-state and the ON-state are illustrated in Fig. 3 and Fig. 4(b), respectively.

The voltage of the capacitor C2 (V_{C2}) versus time is shown in Fig. 11(a). In the first period, V_{C2} remains 0 V in the on-state, and increases in the off-state to store charge. This finding indicates that z1 successfully stops the gate current from charging C2, and the total gate current (I_g) is consequently reduced, as shown in Fig. 11(b). After several periods, C2, instead of I_g, provides electrons for inducing the hole accumulation layer, which is illustrated in the figures by V_{C2} decreasing and $|I_g| = |I_{Gp}|$, because there are enough electrons stored in C2.

Fig. 12 illustrates the key fabrication sequence of the proposed device, which is verified by the process simulator Tsurprem-4, and is compatible with CMOS technology. By utilizing corner regions, it is not difficult to integrate the circuit on a chip without taking away from the area of the active region in the main device. The proposed device has two differences from the previous device in the fabrication, which are as follows.

One difference is the fabrication of the pn diode on the oxide. After the direct deposition over the oxide, the deposited silicon is normally polycrystalline, which is not able to sustain a high voltage. However, this problem can be solved by using a method of recrystallization in laser [16]–[18]. The laser recrystallized polysilicon exhibits an improved static performance that is almost as good as the single-crystal silicon. The other difference is to fabricate the integrated inductor L1, which complicates the process [15], [19]. For example, in [15], processes such as electroplating copper on the oxide, spin-coating and hard-curing polyimide PI-2611, sputter-deposition and wet-etch of amorphous CoTaZr film (the magnetic core), which are not standard CMOS processing steps, are required. However, as an alternative option for this work, it is also possible to package a discrete inductor and other components together for achieving this functionality.

Both aforementioned differences increase the complexity of the fabrication process, which is a disadvantage. However, these changes significantly improve the electrical characteristics of the device.

IV. CONCLUSION

In this paper, an improved SOI p-LDMOS is proposed and investigated by TCAD simulations. The conduction of high-mobility electrons and accumulated holes significantly improves its electrical characteristics, to which the achievement of a small $R_{on,sp}$ and a high current capability can be attributed. Owing to the self-controlled n-channel

gate, the proposed device still has the conventional three-terminal style, and its fabrication process is compatible with CMOS technology. The simulation results indicate that, compared with the previous device at the same BV of 300 V, the proposed device has decreased the $R_{on,sp}$ by 78% and increased the FOM approximately 3.4 times.

REFERENCES

[1] S. Shimamoto *et al.*, "High performance Pch-LDMOS transistors in wide range voltage from 35V to 200V SOI LDMOS platform technology," in *Proc. IEEE 23rd Int. Symp. Power Semicond. Devices ICs (ISPSD)*, May 2011, pp. 44–47. doi: 10.1109/ISPSD.2011.5890786.

[2] T. Miyoshi *et al.*, "300 V field-MOS FETs for HV-switching IC," in *Proc. IEEE 23rd Int. Symp. Power Semicond. Devices ICs (ISPSD)*, May 2011, pp. 40–43. doi: 10.1109/ISPSD.2011.5890785.

[3] S. Shimamoto *et al.*, "High-performance P-channel LDMOS transistors and wide-range voltage platform technology using novel P-channel structure," *IEEE Trans. Electron. Devices*, vol. 60, no. 1, pp. 360–365, Jan. 2013. doi: 10.1109/TED.2012.2228202.

[4] X. Zhou, M. Qiao, Y. He, Z. Wang, Z. Li, and B. Zhang, "Back-gate effect on $R_{on,sp}$ and BV for thin layer SOI field p-channel LDMOS," *IEEE Trans. Electron Devices*, vol. 62, no. 4, pp. 1098–1104, Apr. 2015. doi: 10.1109/TED.2015.2399504.

[5] F. Udrea, A. Popescu, and W. I. Milne, "3D RESURF double-gate MOSFET: A revolutionary power device concept," *Electron. Lett.*, vol. 34, no. 8, pp. 808–809, Apr. 1998. doi: 10.1049/el:19980504.

[6] M. Kong, W. Du, and X. Chen, "Study on dual channel n-p-LDMOS power devices with three terminals," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3508–3514, Oct. 2013. doi: 10.1109/TED.2013.2275076.

[7] Y. Zhang, S. Pendharkar, P. Hower, S. Giombanco, A. Amoroso, and F. Marino, "A RESURF P-N bimodal LDMOS suitable for high voltage power switching applications," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Jun. 2015, pp. 61–64. doi: 10.1109/ISPSD.2015.7123389.

[8] J. Kim, S.-G. Kim, Q. S. Song, S. Y. Lee, J.-G. Koo, and D. S. Ma, "Improvement of P-channel SOI LDMOS transistor by adapting a new tapered oxide technique," *IEEE Trans. Electron Devices*, vol. 46, no. 9, pp. 1890–1894, Sep. 1999. doi: 10.1109/16.784190.

[9] X. Chen, "Low voltage power supply," U.S. Patent 8 294 215, Oct. 23, 2012. [Online]. Available: https://www.google.com/patents/US8294215

[10] X. Lyu and X. Chen, "An ultralow specific ON-resistance LDMOST using charge balance by split p-gate and n-drift regions," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3821–3826, Nov. 2013. doi: 10.1109/TED.2013.2283426.

[11] *Sentaurus Device User Guide, Version I-2013.12*, Synopsys, Inc., Mountain View, CA, USA, 2013.

[12] T. Miyoshi, T. Tominari, H. Fujiwara, T. Oshima, and J. Noguchi, "Design of a reliable p-channel LDMOS FET with RESURF technology," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1451–1456, May 2014. doi: 10.1109/TED.2014.2309672.

[13] K. Kobayashi, H. Yanagigawa, K. Mori, S. Yamanaka, and A. Fujiwara, "High voltage SOI CMOS IC technology for driving plasma display panels," in *Proc. IEEE 10th Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Jun. 1998, pp. 141–144. doi: 10.1109/ISPSD.1998.702655.

[14] B. Luo *et al.*, "High voltage SJ-pLDMOS with variation lateral doping drift layer," in *Proc. Int. Conf. Commun. Circuits Syst. (ICCCAS)*, Jul. 2010, pp. 503–506. doi: 10.1109/ICCCAS.2010.5581945.

[15] D. W. Lee, K.-P. Hwang, and S. X. Wang, "Fabrication and analysis of high-performance integrated solenoid inductor with magnetic core," *IEEE Trans. Mag.*, vol. 44, no. 11, pp. 4089–4095, Nov. 2008. doi: 10.1109/TMAG.2008.2003398.

[16] N. Bidin and S. N. A. Razak, "Crystallization of poly-silicon film by different annealing techniques," in *Proc. Saudi Int. Electron. Commun. Photon. Conf. (SIECPC)*, Apr. 2011, pp. 1–4. doi: 10.1109/SIECPC.2011.5877013.

[17] A. Gat, L. Gerzberg, J. F. Gibbons, T. J. Magee, J. Peng, and J. D. Hong, "CW laser anneal of polycrystalline silicon: Crystalline structure, electrical properties," *Appl. Phys. Lett.*, vol. 33, no. 8, pp. 775–778, Oct. 1978. doi: 10.1063/1.90501.

[18] R. R. Shah, D. R. Hollingsworth, G. A. DeJong, and D. L. Crosthwait, "P-N junction and Schottky barrier diode fabrication in laser recrystallized polysilicon on SiO2," *IEEE Electron Device Lett.*, vol. 2, no. 7, pp. 159–161, Jul. 1981. doi: 10.1109/EDL.1981.25382.

[19] X. Fang, R. Wu, L. Peng, and J. K. O. Sin, "A novel silicon-embedded toroidal power inductor with magnetic core," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 292–294, Feb. 2013. doi: 10.1109/LED.2012.2234077.

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