Top-Bottom Gate Coupling Effect on Low Frequency Noise in a Schottky Junction Gated Silicon Nanowire Field-Effect Transistor

XI CHEN[1], SI CHEN[1], PAUL SOLOMON[2], AND ZHEN ZHANG [1]

1 Division of Solid-State Electronics, Department of Engineering Sciences, Ångström Laboratory, Uppsala University, 75121 Uppsala, Sweden
2 IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598, USA

CORRESPONDING AUTHOR: Z. ZHANG (e-mail: zhen.zhang@angstrom.uu.se)

ABSTRACT In this letter, strong low frequency noise (LFN) reduction is observed when the buried oxide (BOX)/silicon interface of a Schottky junction gated silicon nanowire field-effect transistor (SJGFET) is depleted by a substrate bias. Such LFN reduction is mainly attributed to the dramatic reduction in Coulomb scattering when carriers are pushed away from the interface. The BOX/silicon interface depletion can also be achieved by sidewall Schottky junction gates in a narrow channel SJGFET, leading to an optimal LFN performance without the need of any substrate bias.

INDEX TERMS Schottky junction gate, silicon nanowire, low frequency noise, substrate bias.

I. INTRODUCTION

Silicon nanowire (SiNW) field-effect transistors (FETs) have been demonstrated as a fast, highly sensitive, and label-free detection platform targeting charged biomolecules in electrolyte [1]–[4]. During operation, association and dissociation between targets in the electrolyte and receptors immobilized on the SiNW surface will generate charge and electrical potential variations which can modulate the drain-to-source current (I_{DS}) of the SiNWFETs. The lower detection limit of the SiNWFET sensor is determined by its noise with the intrinsic device noise as a major component [5]–[7]. Such noise source in a MOS-type SiNWFET is known to be associated to the trapping/detrapping of charged carriers at the gate oxide/silicon interface [8].

In previous work, we demonstrated that the aforementioned carrier trapping/detrapping processes can be greatly reduced by replacing the noisy gate oxide/silicon interface on the top of the SiNW channel with a Schottky junction gate (SJG) interface [9]. The resulting Schottky junction top-gate SiNWFETs (SJGFETs) exhibit significantly reduced low frequency noise (LFN) in comparison to that of reference MOS-type SiNWFETs. It is also observed that a substrate bias (V_{sub}) can modulate the LFN of the SJGFET by controlling the distance between the conduction channel and the buried oxide (BOX)/silicon interface which is known to have adverse effect on the LFN [10].

In this letter, the effects of V_{sub} on the electrostatic control as well as LFN of the SJGFET are systematically investigated using a tri-gate SJGFET (Tri-SJGFET) with a 3-dimentional (3D) SJG wrapping the top surface and the two sidewalls of the SiNW channel [11]. Previously established noise models [12]–[14] are employed for understanding LFN behavior of the Tri-SJGFET. A Tri-SJGFET with a wide channel is first employed to study the top-bottom gate coupling since it approximates to a top-gate SJGFET due to the high width-to-height ratio. We further observe that in a narrow channel Tri-SJGFET, the additional sidewall SJGs enable carrier depletion from the sidewalls and confine current conduction path within the bulk of the SiNW channel. Therefore, optimal LFN performance can be attained without an additional V_{sub}.

II. EXPERIMENTAL

Tri-SJGFETs were fabricated on a 100-mm SIMOX-type SOI wafer by means of standard silicon process technology. The SOI wafer comprised a 200-nm thick silicon layer on top of a 375-nm thick BOX. Detailed fabrication process
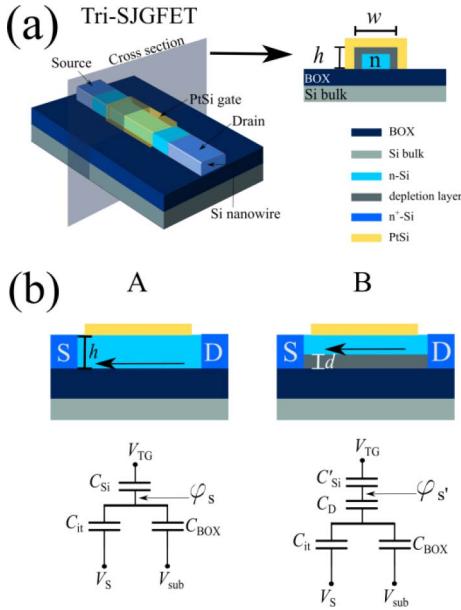
FIGURE 1. (a) 3D schematic of a SJGFET along with the respective cross-section of the gated SiNW section with the depletion layer illustrated as the grey region. (b) Cross-sectional sketches for a SJGFET without (A, left) and with (B, right) BOX/silicon interface depletion, and the arrow indicates the position of the current centroid. Corresponding equivalent capacitor network when the SJGFET is under top gate operation within subthreshold region with a fixed V_{sub} in the presence of C_{it} is shown below. V_S is the source potential. With a bottom depletion width of d, C_D in (B) can be expressed as $C_D = C'_{Si} \bullet (h - d)/d$.

can be found in previous work [9], [11]. A 3D schematic view of a Tri-SJGFET with SJGs present on the SiNW sidewalls is shown in Fig. 1(a). Tri-SJGFETs with two different channel widths (w_{si}), *i.e.*, 480 nm and 120 nm, are designed to evaluate the effect of sidewall depletion and hereafter are referred as SJG480 and SJG120, respectively. They have the same gate length L_G = 900 nm and channel height h = 90 nm. The SiNW channel is moderately *n*-doped with $N_D = 2.3 \times 10^{17}$ cm^{-3} as confirmed by sheet resistance measurement.

Transfer (I_{DS} vs. V_G) characteristics were measured at room temperature on a probe-station using a Keysight B1500A precision semiconductor parameter analyzer. The power spectrum density (PSD) of I_{DS}, S_{id}, was characterized using a Keysight E4727A advanced LFN analyzer at different I_{DS} set values. 3D device simulations were implemented using commercially available simulation tools (Sentaurus Device from Synopsys). Geometries and doping profiles of the SJGFETs were defined using Sentaurus Structure Editor.

III. RESULTS AND DISCUSSIONS

As shown in our previous work [9], the BOX/silicon interface becomes the dominant noise source of a SJGFET. Therefore, top gate, *i.e.*, SJG, referred voltage noise, S_{Vgt}, of the SJGFET can be expressed as

$$S_{Vgt} = \frac{S_{id}}{g_{m,t}^2} = \frac{S_{Vgb}g_{m,b}^2}{g_{m,t}^2}, \qquad (1)$$

where $g_{m,t}$ and $g_{m,b}$ are the top and bottom gate transconductances, respectively. S_{Vgb} is the bottom gate referred voltage noise and can be described by the carrier number fluctuations model (CNF) with additional correlated mobility fluctuations model (CMF) induced by the Coulomb scattering due to the interface charges [13], [15],

$$S_{Vgb} = S_{Vgbf}\left(1 + \alpha_{sc}\mu_{eff}C_{BOX}\frac{I_{DS}}{g_{mb}}\right)^2, \qquad (2)$$

with α_{sc} the Coulomb scattering coefficient, μ_{eff} the mobility, and C_{BOX} the BOX capacitance. S_{Vgbf} is the bottom gate voltage noise at flat-band condition [8], [15], given by

$$S_{Vgbf} = \frac{q^2 \lambda kTN_t}{wL_GC_{BOX}^2}\frac{1}{f}, \qquad (3)$$

with q the elemental charge, kT the thermal voltage, λ the oxide tunneling distance ($\sim$0.1 nm) [15], N_t the volume trap density (cm$^{-3} \cdot$eV^{-1}) in the gate oxide per eV, and f the frequency. From (1), it is clear the S_{Vgt} of the SJGFET strongly depends on S_{Vgb}, and bottom-to-top transconductance ratio $g_{m,b}/g_{m,t}$, suggesting that stronger top gate control (higher $g_{m,t}$) or weaker bottom gate control (lower $g_{m,b}$) can lead to a lower S_{Vgt}.

In the SJGFET, when I_{DS} conduction path is located at the BOX/silicon interface as shown by the case A in Fig. 1(b), the surface potential ψ_s is related SJG voltage V_{TG} through

$$\frac{\partial \psi_s}{\partial V_{TG}} = \frac{C_{Si}}{C_{Si} + C_{it} + C_{BOX}}, \qquad (4)$$

where C_{Si} is the silicon depletion-layer capacitance. C_{it} is the capacitance capacitance associated with the BOX/silicon interface traps. (C_{it} is in parallel with C_{BOX} because the substrate is AC grounded to the source). With a negative V_{sub} pushing the I_{DS} conduction path a distance of d away from the interface (case B), electrostatic control control from the SJG is enhanced and the dependence of surface potential ψ'_s on

$$\frac{\partial \psi'_s}{\partial V_{TG}} = \frac{C_{Si}}{C_{Si} + C_{it} + C_{BOX}} + \frac{C_{it} + C_{BOX}}{C_{Si} + C_{it} + C_{BOX}} \cdot \frac{d}{h} \quad (5)$$

The $g_{m,t}$ of the SJGFET is directly correlated to $\partial\psi_s/\partial V_{TG}$. From (4) and (5), it becomes clear that by pushing the I_{DS} conduction path away from the BOX/silicon interface, enhanced gate coupling from the SJG can be achieved, also referring to higher $g_{m,t}$. I_{DS} vs. V_{TG} curves of SJG480 measured at different V_{sub} are depicted in Fig. 2(a). As expected, the subthreshold slope (*SS*) of SJG480 is improved from 249 mV/dec at V_{sub} = 10 V to 78 mV/dec at V_{sub} = −30 V. The extracted $g_{m,t}$ as a function of I_{DS} are depicted in Fig. 2(b), showing a factor of about 3 increase when the BOX/silicon interface is swept from accumulation to depletion. On the other hand, $g_{m,b}$ is less sensitive to the position of the current path due to the dominating BOX thickness.
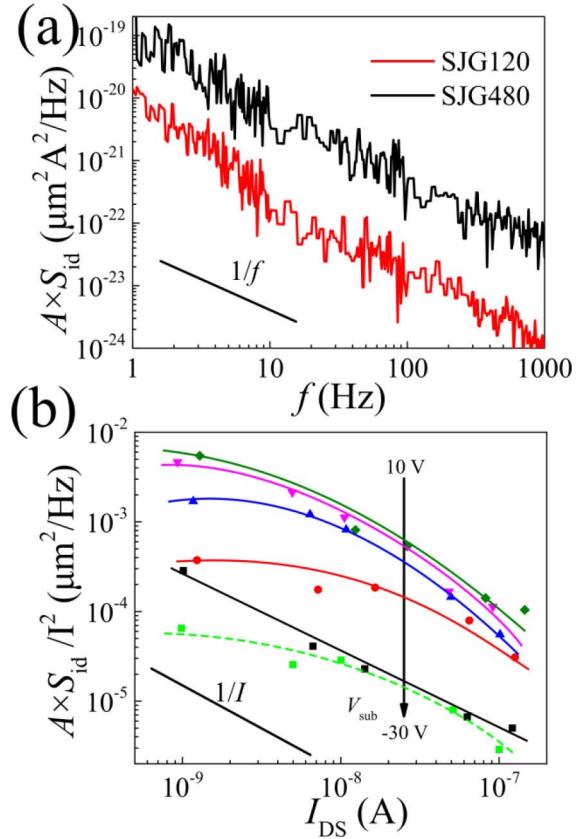
Gate area (A) normalized S_{id}, $A \times S_{id}$, as a function as f for SJG480 and SJG120 measured at I_{DS} = 50 nA are presented
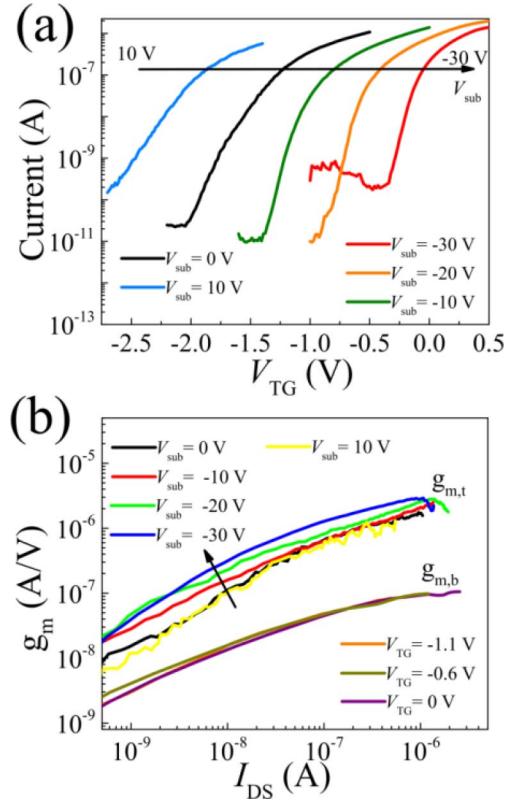
FIGURE 2. (a) I_{DS} as a function of V_{TG} for SJG480 measured at different V_{sub}, (b) $g_{m,t}$ and $g_{m,b}$ as a function of I_{DS} for SJG480 measured at different bias conditions, $V_{DS} = 0.1$ V. The arrow indicates V_{sub} from 10 V to −30 V.


FIGURE 3. (a) $A \times S_{id}$ as a function of f measured at $I_{DS} = 50$ nA for SJG120 and SJG480 at $V_{sub} = 0$ V, (b) comparison of measured $A \times S_{id}/I_{DS}^2$ as a function of I_{DS} for SJG480 (solid lines) with different V_{sub}, and for SJG120 (dashed line) at $V_{sub} = 0$ V, $V_{DS} = 0.1$ V. The arrow in (b) indicates V_{sub} change from 10 V to −30 V for SJG480.

in Fig. 3(a) measured at $V_{sub} = 0$ V. Both SJGFETs exhibit a $1/f$ like noise spectrum at low frequencies (1-1k Hz). To further identify the noise source, $A \times S_{id}/I_{DS}^2$ versus I_{DS} plots measured at $f = 10$ Hz for SJG480 (solid lines) at different V_{sub} and SJG120 (dashed line) at $V_{sub} = 0$ V are depicted in Fig. 3(b). In V_{sub} range from 10 to −20 V, the noise of SJG480 can be well described by CNF/CMF model [15]–[18], indicating trapping/detrapping process at BOX/silicon interface is the dominant noise source. However, at $V_{sub} = -30$ V, $A \times S_{id}/I_{DS}^2$ becomes proportional to $1/I_{DS}$, which follows Hooge mobility fluctuation (HMF) model [16] and suggests that carrier mobility fluctuations due to phonon interactions in the bulk channel is likely the dominant noise source. Such noise transformation from CNF/CMF to HMF has also been observed before [16] when conduction channel is moved away from surface to volume.

Gate area normalized S_{Vgt}, $A \times S_{Vgt}$, of SJG480 is strongly dependent on V_{sub} as shown in Fig. 4(a). At $I_{DS} = 10$ nA, $A \times S_{Vgt}$ is reduced by about 3 orders of magnitudes when V_{sub} is changed from 10 to −30 V at $f = 10$ Hz, which cannot be fully explained with (1) only by the enhanced SJG coupling and therefore reduction in $g_{m,b}/g_{m,t}$. To understand the root cause for such S_{Vgt} improvement, bottom gate transfer characteristic, *i.e.*, I_{DS} vs. V_{sub} curve with $V_{TG} = 0$ V, of SJG480 is examined in Fig. 4(b). Clearly, the BOX/silicon

interface is accumulated with electrons at $V_{sub} = 0$ V and I_{DS} mainly flows close to the BOX/silicon interface as illustrated by the current density contour in the insert of Fig. 4(b). The interface is under depletion when V_{sub} becomes more negative than −10 V. The dramatic reduction in S_{Vgt} suggests that the CMF [8], [15], [16], *i.e.*, second term in (2), is dominant as the Coulomb scattering coefficient α_{sc} is related to distance d, the electron centroid from the BOX/silicon interface, through [12], [14], [19]

$$\alpha_{sc} = \frac{\alpha_0}{(1 + d/\lambda_c)^2}. \quad (6)$$

where α_0 is a constant and λ_c is about 1.2 nm [19]. It can be estimated from (2) and (6) that an increase of d from 0 to $2\lambda_c$ could lead to reduction in both S_{vgb} and S_{vgt} by about 80 times. Therefore, rather than the reduction in $g_{m,b}/g_{m,t}$, the depletion which pushes the conduction path away from the BOX/silicon interface contributes dominantly to the dramatic noise reduction in SJG480.

With the data in Fig. 2(b) and 3(b) processed by (1), N_t and α_{sc} can be calculated using (2) and (3). With C_{BOX} of 9.4×10^{-5} F/m², and λ of 0.1 nm from [15], the resultant N_t and α_{sc} are summarized in Table 1. The N_t and α_{sc} are relatively high compared to reported values for typical SiO2/silicon
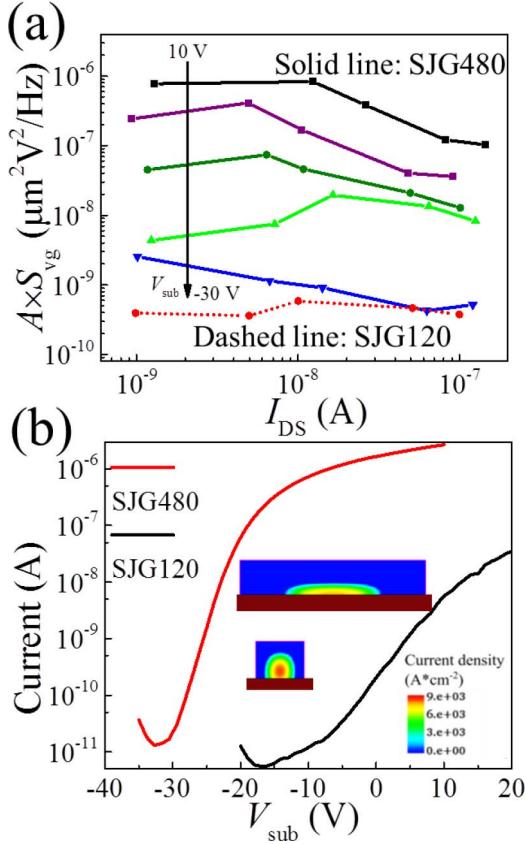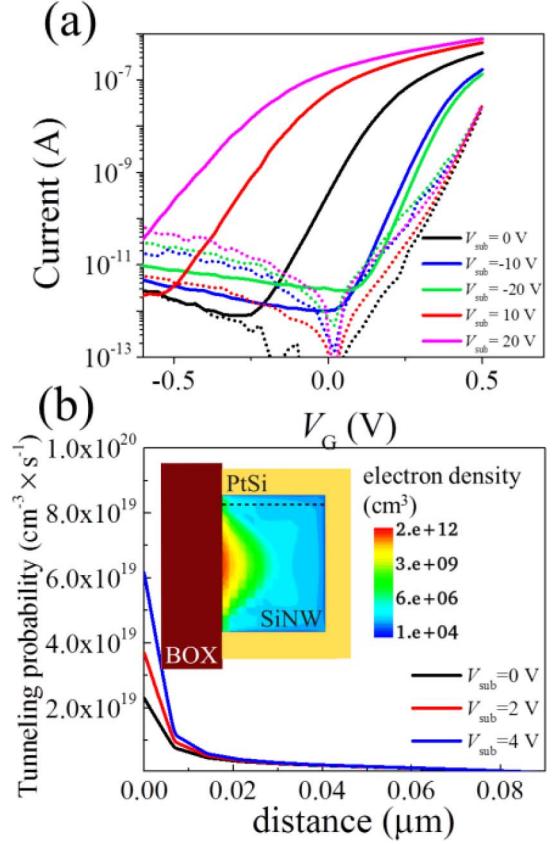
FIGURE 4. (a) $A \times S_{vg}$ as a function of I_{DS} at $f = 10$ Hz for SJG480 (solid lines) at different V_{sub}, and for SJG120 (dashed line) at $V_{sub} = 0$ V. (b) I_{DS} as a function of V_{sub} for SJG480 (red) and SJG120 (black) measured at $V_{TG} = 0$ V, $V_{DS} = 0.1$ V, insert: cross-section views of simulated current density contour in the SiNW channel for SJG480 and SJG120 at $V_{sub} = 0$ V and the same $I_{DS} = 100$ nA.

FIGURE 5. (a) I_{DS} (solid lines) and I_G (dashed lines) as a function of V_G for SJG120 measured at different V_{sub}, (b) simulated G_{tun} (along the dashed line located 5 nm away from the SG in the insert) vs. distance to the BOX/silicon interface with different V_{sub}. Insert: cross-section view of simulated electron density contour in the SiNW channel with a positive V_{sub}.

TABLE 1. Extracted N_t and α_{sc} for SJG480 under different V_{sub}.

V_{sub} (V)	-20	-10	0	10
N_t (cm^{-3}eV^{-1})	2.6×10^{19}			
α_{sc} (V·s/C)	1.4×10^5	9.8×10^5	2.1×10^6	2.5×10^6

interface [15], [17], which could be ascribed to the poor BOX/silicon interface quality of SIMOX-type SOI wafers. This also shows the potential for further noise reduction in our SJGFETs by using SOI wafers with high quality BOX/silicon interface.

When w of the SiNW channel is shrunk to the situation where depletion from the sidewall SJGs becomes dominant as the case for SJG120, BOX/silicon interface depletion can be achieved even at $V_{sub} = 0$ V. This is confirmed by the measured $I_{DS} - V_{sub}$ curved with $V_{TG} = 0$ V as depicted in Fig. 4(b) showing that SJG120 is in subthreshold region at $V_{sub} = 0$ V. Simulation also shows that the current distribution of SJG120 in the SiNW channel differs greatly to that of SJG480, as its centroid is now located further away from the BOX/silicon interface (insert in Fig. 4(b)). Meanwhile,

$g_{m,b}/g_{m,t}$ of SJG120 is lowered due to the enhanced electrostatic control by the top SJG as the SiNW channel is shrunk. Benefiting from the combination of reduced CMF contribution due to the SiNW bulk confined conduction and low $g_{m,b}/g_{m,t}$, SJG120 exhibits low $A \times S_{Vgt}$ already at $V_{sub} = 0$ V which otherwise requires $V_{sub} = -30$ V to achieve on SJG480 as shown in Fig. 4(a).

The sidewall SJGs may pose a potential risk for high gate leakage current, I_G, for the Tri-SJGFETs. As shown in Fig. 5(a), I_G is low at a few pA level with $V_{sub} = 0$ V when the SJG is under reverse bias but increases when a positive V_{sub} is applied. The positive V_{sub} biases the BOX/silicon interface into accumulation and thus dramatically raises the electron concentration close to the interface. Such high electron concentration will lead to reduced barrier thickness of the sidewall SJGs which are close to the BOX/silicon interface therefore enhance electron tunneling across the SJGs [20]. Such tunneling effect is confirmed by device simulations. As shown in Fig. 5(b), simulated electron tunneling generation rate (G_{tun}) increases rapidly towards the BOX/silicon interface as a result of increased electron concentration and can be further enhanced by a positive V_{sub}. It

is also noted that I_G increases as well at negative V_{sub} which elevates hole concentration near the BOX/silicon interface. The high I_G is also due to the hole tunneling to the near sidewall SJGs since PtSi/Si has a low junction barrier height for holes.

IV. CONCLUSION

LFN performance of the SJGFET is greatly improved when the BOX/silicon is depleted by a V_{sub}. It is explained by the combined effects of lowered $g_{m,b}/g_{m,t}$ due to the enhanced top SJG control and reduced Coulomb scattering as carriers are depleted away from the BOX/silicon interface, while the latter effect plays a dominant role in the noise reduction. Also with the conduction channel away from interfaces, volume phonon scattering related noise which can be described by HMF model is observed. It is further demonstrated that the BOX/silicon interface depletion can be achieved without the need for any V_{sub} by the sidewall SJGs in a narrow channel device. However, enhanced carrier tunneling through the sidewall SJGs may give rise to I_G.

REFERENCES

[1] Y. Cui, Q. Wei, H. Park, and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science*, vol. 293, no. 5533, pp. 1289–1292, Aug. 2001.

[2] E. Stern *et al.*, "Label-free biomarker detection from whole blood," *Nat. Nanotechnol.*, vol. 5, no. 2, pp. 138–142, Feb. 2010.

[3] Y. L. Bunimovich, Y. S. Shin, W.-S. Yeo, M. Amori, G. Kwong, and J. R. Heath, "Quantitative real-time measurements of DNA hybridization with alkylated nonoxidized silicon nanowires in electrolyte solution," *J. Amer. Chem. Soc.*, vol. 128, no. 50, pp. 16323–16331, Dec. 2006.

[4] G. Zheng, F. Patolsky, Y. Cui, W. U. Wang, and C. M. Lieber, "Multiplexed electrical detection of cancer markers with nanowire sensor arrays," *Nat. Biotechnol.*, vol. 23, no. 10, pp. 1294–1301, Sep. 2005.

[5] K. Bedner *et al.*, "Investigation of the dominant 1/f noise source in silicon nanowire sensors," *Sensors Actuators B Chem.*, vol. 191, pp. 270–275, Feb. 2014.

[6] D. Zhang *et al.*, "Direct assessment of solid–liquid interface noise in ion sensing using a differential method," *Appl. Phys. Lett.*, vol. 108, no. 15, Apr. 2016, Art. no. 151603.

[7] N. K. Rajan, D. A. Routenberg, and M. A. Reed, "Optimal signal-to-noise ratio for silicon nanowire biochemical sensors," *Appl. Phys. Lett.*, vol. 98, no. 26, 2011, Art. no. 264107.

[8] E. Simoen and C. Claeys, "The low-frequency noise behaviour of silicon-on-insulator technologies," *Solid-State Electron.*, vol. 39, no. 7, pp. 949–960, 1996.

[9] X. Chen, S. Chen, Q. Hu, S.-L. Zhang, P. Solomon, and Z. Zhang, "Device noise reduction for silicon nanowire field-effect-transistor based sensors by using a Schottky junction gate," *ACS Sensors*, vol. 4, no. 2, pp. 427–433, Feb. 2019.

[10] V. A. Kushner, K. Park, D. K. Schroder, and T. J. Thornton, "Low-frequency-noise spectroscopy of SIMOX and bonded SOI wafers," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3378–3382, Dec. 2007.

[11] X. Chen, S. Chen, S.-L. Zhang, P. Solomon, and Z. Zhang, "Low noise Schottky junction tri-gate silicon nanowire field-effect transistor for charge sensing," *IEEE Trans. Electron Devices*, to be published.

[12] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect MOS transistors," *Physica Status Solidi (a)*, vol. 124, no. 2, pp. 571–581, 1991.

[13] L. Zafari, J. Jomaah, and G. Ghibaudo, "Low frequency noise in multi-gate SOI CMOS devices," *Solid-State Electron.*, vol. 51, no. 2, pp. 292–298, Feb. 2007.

[14] F. N. Hooge, "1/f noise sources," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1926–1935, Nov. 1994.

[15] C. G. Theodorou *et al.*, "Low-frequency noise sources in advanced UTBB FD-SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1161–1167, Apr. 2014.

[16] K. Akarvardar, B. M. Dufrene, S. Cristoloveanu, P. Gentil, B. J. Blalock, and M. M. Mojarradi, "Low-frequency noise in SOI four-gate transistors," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 829–835, Apr. 2006.

[17] C. G. Theodorou *et al.*, "Front-back gate coupling effect on 1/f noise in ultra-thin Si film FDSOI MOSFETs," in *Proc. Int. Semicond. Conf. Dresden–Grenoble (ISCDG)*, Grenoble, France, 2012, pp. 223–226.

[18] D. Jang *et al.*, "Low-frequency noise in strained SiGe core-shell nanowire p-channel field effect transistors," *Appl. Phys. Lett.*, vol. 97, no. 7, Aug. 2010, Art. no. 073505.

[19] G. Ghibaudo, Ed., *Semiconductor-on-Insulator Materials for Nanoelectronics Applications*. Berlin, Germany: Springer-Verlag, 2011, pp. 307–322.

[20] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York, NY, USA: Wiley, 1981.