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Design of Power- and Variability-Aware Nonvolatile RRAM Cell Using Memristor as a Memory Element

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ABSTRACT A 3 CNFETs and 2 memristors-based half-select disturbance free 3T2R resistive RAM (RRAM) cell is proposed in this paper. While the two memristors act as the nonvolatile memory elements, CNFETs are employed as high-performance switches. The proposed cell is capable of implementing bit-interleaving architecture and various error correction coding (ECC) schemes can be applied to mitigate soft-errors. The 3T2R cell has been compared with the standard 6T SRAM (S6T) and 2T2R cells. At a supply voltage of 2 V, the 3T2R cell exhibits 7.24× shorter write delay (T_{WA}) and 2.89× lower variability in T_{WA} than that of 2T2R. Moreover, it exhibits 5.08 × /4.33× lower variability in T_{RA} and 1.46×10^7 × /2.07× lower hold power (H_{PWR}) dissipation than that of S6T/ 2T2R at $V_{DD} = 2$ V. In addition, it exhibits tolerance to variations in V_{th} of memristor while being immune to resistance-state drift and random telegraph noise (RTN)-induced instabilities during the read operation. The vastly superior characteristics of CNFET devices over MOSFETs, in combination with memristor technology, leads to such appreciable improvement in design metrics of the proposed design.

INDEX TERMS Nonvolatile memory, RRAM, memristor, CNFET, leakage power, write delay.

I. INTRODUCTION

Traditionally, the temporary and permanent data storage requirements of any information processing unit have been accomplished by MOSFET-based memories like DRAM, SRAM and flash memory. The volatile nature of SRAM/ DRAM leads to loss of stored data as soon as power supply is removed. Consequently, there is an intense demand for high-performance, power-efficient and high-density nonvolatile memory (NVM) in the semiconductor industry. Several novel approaches to NVM have been developed over the years. These include – the spin-transfer-torque magnetic random access memory (STT-MRAM), phase-change random access memory (PCRAM), conductive-bridging random access memory (CBRAM) and metal-oxide resistive random access memory (RRAM) [1]. In STT-MRAM, data is stored in terms of the orientation of the magnetization of a nanoscale ferromagnetic layer. It exhibits good endurance at the expense of very low packaging density [1]. In PCRAM, switching between high resistance amorphous phase and low resistance crystalline phase is brought about by joule heating of the phase-change material. On the other hand, in CBRAM, the migration of metal ions in a metal-insulator-metal (MIM) structure brings about resistive switching when subjected to an external electric field. Both PCRAM and CBRAM exhibit improved packaging density and resistance ratio. However, their endurance and speed are significantly low [1]. In metal-oxide RRAM, the repeated formation and destruction of oxygen vacancy-rich conductive filament (CF), in a MIM structure, resulting from the creation and motion of oxygen vacancies (V_O) when subjected to an electric field, leads to switching between a low resistance and high resistance state. The RRAM offers many advantageous traits such as high switching speed, low power consumption as well as high packaging density. Consequently, it is seen as an alternative for silicon-based flash memories [2]. Moreover, as RRAM is compatible

with CMOS [3], CNFET [4] and is highly scalable [2], it is capable of outperforming conventional high-performance memories such as conventional SRAMs in the nanometer regime. Therefore, the RRAM appears to be the most promising technology for memory applications.

Memristor switches between one or more than one value of resistances on application of appropriate voltage levels [5]. Such distinct resistance levels can have one or more discrete values or have a continuous variable resistance. The change in resistance is controlled by the past history of the device - that is, by the previous voltage applied to the device. The memristor is a nonlinear resistor which changes its state of resistance in accordance to the net electric flux or net charge passing through its terminals. After the electrical bias is removed, it retains its state. It is only recently, that a TiO_2-based physical implementation of the device was made possible by HP labs in 2008 [6]. Such metal oxide based resistive switching memory element can be used in RRAM due to its simple composition, low cost and compatibility with CMOS technology [7]. In addition, it also exhibits very low power consumption as well as high packing density. However, the TiO_2-based memristors exhibit low endurance ($\sim 10^5$ switching cycles) [8]. Consequently, HfO_x based memristors which show significantly higher endurance ($> 10^{11}$ switching cycles) and retention characteristics (around 10 years) are a better alternative for RRAM implementations [8]–[10].

The 1R RRAM is the most common form of nonvolatile memory implementation using memristors. However, it suffers from several problems in terms of speed, reliability and data-dependent leakage [11]. For example, in a 1R RRAM cell, the "sneak current" issue is a major design constraint which leads to large leakage current through unselected cells in the selected row and column, and results in erroneous read operation [12]. This takes place due to the absence of any shielding mechanism to isolate the unselected cells from bitline and wordline voltages during the read operation [13]. Consequently, the memory performance is considerably degraded [14]. By using an additional CMOS transistor (generally NMOS) adjacent to the memristor in each cell, the 1T1R configuration exhibits significant reduction in "sneak current" [15]. However, it is still highly susceptible to soft-error occurrence in the form of both single event upset (SEU) and multiple event upset (MEU) when the memristor of the half-selected cell is in the high resistance state (HRS) [16], [17], as one end of the memristor is directly connected to the bitline even though the other end is isolated by the transistor. Although this is an improvement when compared to 1R RRAM crossbar, which is prone to soft-errors in both low resistance state (LRS) and HRS, the memory performance of the 1T1R RRAM is still deteriorated [16].

Several memristor-based nonvolatile memories have been proposed over the years for cache memory applications such as the 8T2R [18], 6T1R [19], etc. However, the use of several CMOS transistors in their design leads to significant area overhead per cell. Although, the 2T2R RRAM cell in [20], is relatively area-efficient due to the presence of fewer transistors, it suffers from inherent half-select disturbance issues during the read operation (explained in Section III-B). In addition, all the aforementioned designs require the integration of memristor with CMOS technology, which is a particularly difficult process and requires very high temperature conditions ($> 1000°C$) [21]. This can be attributed to the fact that traditional 3D integration techniques (employed in CMOS technology) require parallel integration where the various heterogeneous components are processed individually and stacked together. Through silicon vias (TSVs) with typical pitch size of 10 μm are used to stack the wafers together [22]. Since dopant activation in MOSFETs takes place at very high temperatures ($>1000°C$), separate wafer processing of heterogeneous components is performed to ensure that the other components remain undamaged [21].

Therefore, to overcome the various limitations faced by 1R RRAM, 1T1R RRAM and 2T2R RRAM cells, we have proposed a half-select disturb free 3T2R RRAM cell for cache memory application in this work. It consists of 3 CNFET devices, which function as switches during various operations, and 2 memristors, which act as memory elements. The CNFET devices are instrumental in preventing half-select disturbance in the proposed cell, which renders it capable of implementing bit-interleaving architecture and thus mitigating SEUs and MEUs [23]. Moreover, the use of CNFETs instead of CMOS implies that the proposed cell is less susceptible to soft-errors due to the greater tolerance of radiations shown by the former as compared to the latter [24], [25]. In addition, modern techniques such as monolithic 3D integration is employed for the fabrication of CNFETs and memristors which involves sequential integration of various components, i.e., using the same substrate to integrate distinct tiers of components (such as layers of logic, memory or sensors) [26]. To avoid damage to components at lower tiers, the fabrication of upper tiers is performed at lower temperatures (<400 °C). Although, such a process is rather difficult to employ for CMOS technologies, the fact that both CNFETs and memristors require low temperature conditions for fabrication renders them suitable for efficient integration [4], [27]. Furthermore, when compared to traditional 3D integration techniques, monolithic 3D integration leads to a tighter integration of memory and logic with highly dense vertical connectivity [28]. Thus, the proposed cell is suitable for fabrication and exhibits improved electrical characteristics due to the use of CNFETs. The salient features of this paper are as follows:

- The proposed circuit exhibits better performance in terms of write delay as well as standby power consumption in comparison to the standard 6T SRAM (S6T) cell and previously proposed design (2T2R RRAM cell) [20].
- The 3T2R cell is immune to resistance-state drift due to the optimisation of read operation.

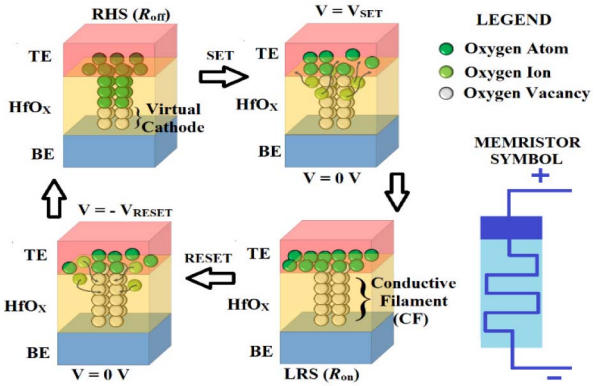

FIGURE 1. Switching mechanism of HfO_x-based memristor and its symbol.

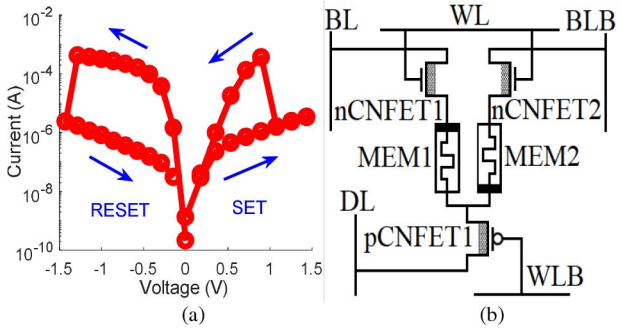

FIGURE 2. (a) I-V characteristics of HfO_x Stanford-PKU memristor model based on CF evolution model [29] and (b) proposed 3T2R RRAM cell.

- The proposed cell mitigates the half-select disturbance issue during the read operation.
- The variability of the 3T2R circuit in terms of delay and power consumption is much lesser than the comparison designs.
- The presence of CNFET devices in combination with memristors, makes the proposed circuit much more efficient than an equivalent CMOS integration.

The rest of the paper is arranged in the following sections – In Section II, a brief overview of the memristor and its switching mechanism is provided. Section III introduces the new CNFET based 3T2R RRAM cell proposed in this work and elucidates its functioning. The methodology of simulation employed and the obtained results have been discussed in Sections IV–VII. The paper is concluded in Section VIII.

II. MEMRISTOR AND ITS SWITCHING MECHANISM

In this work, the Stanford-PKU memristor model [29], which is a SPICE model of RRAM developed based on the conductive filament (CF) evolution model [30], [31], [32] has been employed. In this model, HfO_x (see Fig. 1) is the insulator, sandwiched between a top electrodes (TE) and a bottom electrode (BE) (see Fig. 1), which switches between two resistive states – HRS and LRS, depending on the polarity of the electric field applied across its terminals. It is assumed that the memristor stores '1' when it is in the HRS or R_{off} state and stores '0' when it is in the LRS or R_{on} state. The switching mechanism is shown in Fig. 1. During the SET process or the '0' writing process, a positive voltage is applied across the terminals of the memristor (storing '1'), which leads to the drift of oxygen ions towards the anode interface and their storage in the interfacial oxygen reservoir. This leaves behind a conductive oxygen vacancy path through the oxide, and consequently, the memristor is driven into LRS or R_{on} state. On the other hand, during the RESET process or the '1' writing process, a negative electric field is applied across the terminals of the memristor (storing '0'). This drives the oxygen ions stored in the reservoir towards the bulk HfO_x layer which results in their recombination with oxygen vacancies and drives the memristor into HRS or R_{off} state. This is illustrated by the I-V characteristics (see Fig. 2 (a)) which depicts the change in the amount of current flowing through the memristor with supply voltage across it, due to the change in its resistance. It indicates the ability of such a device to store data in a nonvolatile fashion [5]. The model parameters used in this work are chosen in accordance with [29].

III. PROPOSED CNFET BASED RRAM CELL

The 3T2R RRAM cell (see Fig. 2 (b)), proposed in this work, consists of two memristors, MEM1 and MEM2, of opposite polarity positioned end to end, with respect to each other. MEM1 and MEM2 are connected to the columnar data line (DL) through pCNFET1. The nCNFET1 and nCNFET2 connect MEM1 and MEM2 to bitlines, BL and BLB, respectively. The row-based wordline (WL) controls the access transistors nCNFET1 and nCNFET2 while the pCNFET1 is activated by row-based WLB.

A. WRITE OPERATION

During write operation, WL is activated to turn ON access transistors nCNFET1 and nCNFET2. The pCNFET1 is turned ON by setting WLB to GND. Depending upon the data to be written, BL/BLB and DL are either charged to supply voltage, V_{DD}, or discharged to GND. Consider the case of writing '0', i.e., turning MEM1 to low resistance state, R_{on}, and MEM2 to high resistance state, R_{off}. In this case, DL is kept at GND while both BL and BLB are kept at V_{DD}. Since the negative terminal (undoped side) of MEM1 is connected to DL while its positive terminal (doped side) is connected to BL, a positive voltage across the memristor drives it from R_{off} (high resistance state) to R_{on} (low resistance state). On the contrary, a negative potential is developed across MEM2 and it is driven into a high resistance state. To write '1', DL is kept at V_{DD} while BL/BLB is kept at GND.

Fig. 3 (a) shows the change in resistance of the memristors with time, during write '0' operation. It is seen that the MEM1 is driven into R_{on} state while MEM2 is driven into R_{off} state.

B. READ OPERATION

At the beginning of the read operation, all the CNFET switches are turned ON. Both BL and BLB are precharged

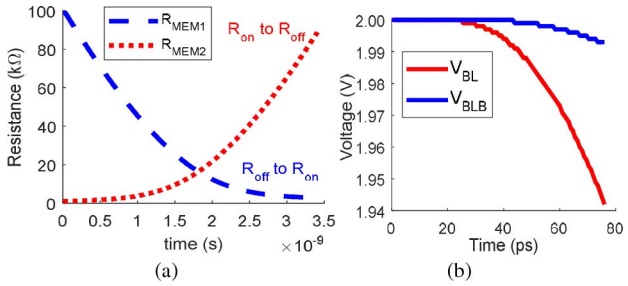

FIGURE 3. **(a) Change in memristances of MEM1 and MEM2 with time during a write '0' operation and (b) voltage drop at BL and BLB with time for a read '0' operation @ $V_{DD} = 2$ V.**

while DL is fixed at GND. As discussed earlier, a memristor in R_{on}/R_{off} state is considered to be storing '0'/'1'. Since, the rate at which voltage drops across the memristors depends on their resistances, either of the bitlines gets discharged and a 50 mV voltage difference is obtained between BL and BLB (see Fig. 3 (b)).

If a constant voltage difference is applied across the terminals of a memristor for a finite amount of time, it may lead to resistive switching and consequently, loss of stored data. Therefore, a read pulse of a duration just long enough to ensure a 50 mV voltage difference is obtained across the bitlines, is applied (for further discussion, see Section IV-A).

As mentioned earlier, one of the major limitations of 1R, 1T1R and 2T2R RRAM cells is their vulnerability to half-select disturbances during the read operation. This can be attributed to the presence of a direct path between BL and BLB via memristors MEM1 and MEM2 [20]. Consequently, whenever either of BL or BLB discharges during the read operation, an effective voltage drop across the memristors is obtained [5]. This may disturb the state of column half-selected cells and lead to loss of stored data. The proposed 3T2R cell makes use of 3 CNFET switches in its design to mitigate the half-select disturbance issue during the read operation. From Fig. 4, which shows the 2×2 memory architecture of the proposed cell, it can be seen that BL and BLB of the entire column of the selected cell are activated during read operation. However, the row-based WL and WLB signals are only activated for the selected row. As a result, the CNFET switches of the column half-selected cells, which are in standby mode, are OFF and their internal memristors are isolated from the bitlines. Thus, the proposed cell is half-select disturb free unlike the 1R, 1T1R and 2T2R cells. Since, the 3T2R cell is half-select disturb free, it is capable of implementing bit-interleaving architecture for mitigating soft-errors using error correction coding (ECC) schemes [23]. Moreover, the use of CNFETs, which show greater tolerance of radiations when compared to CMOS, makes the proposed design even less susceptible to soft-errors [24], [25].

C. HOLD OPERATION

All the CNFET switches are maintained in OFF state during the standby mode. While no operation takes place during the hold mode, a small amount of leakage power is dissipated due to the gate leakage at pCNFET1 as WLB is maintained at supply voltage (V_{DD}).

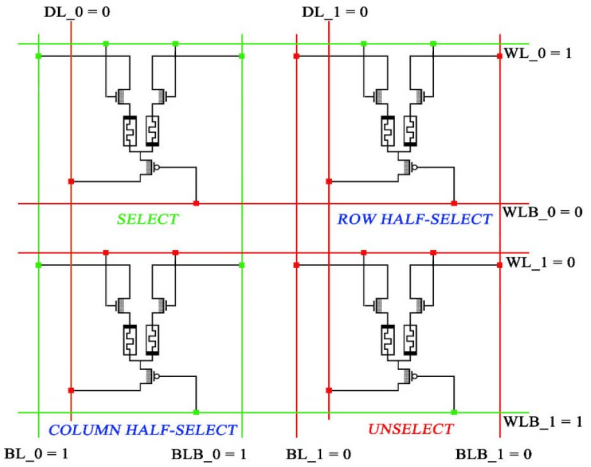

FIGURE 4. **A 2 × 2 memory architecture of 3T2R during the read operation.**

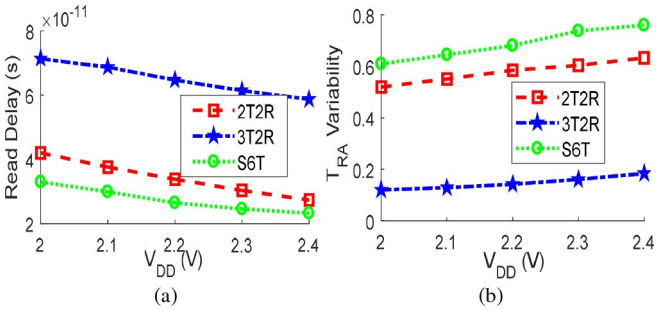

FIGURE 5. **(a) T_{RA} and (b) variability in T_{RA} of different cells at various V_{DD}.**

IV. SIMULATION SETUP AND RESULTS

The HfO_x based Stanford-PKU memristor model proposed in [29] (as explained in Section II) and the high-precision Stanford CNFET model [33], [34], have been used for the simulations of various design metrics of the RRAM cell. The proposed 3T2R RRAM cell has been compared with the 2T2R RRAM cell [20] and the standard 6T SRAM (S6T) cell to exhibit its relative strengths. The 32-nm PTM model [35], developed by the Nanoscale Integration and Modeling (NIMO) Group, has been employed for all the CMOS circuit simulations. The simulations have been performed on the HSPICE platform using Monte Carlo (MC) simulations with 5000 sample size.

A. READ DELAY (T_{RA})

In accordance with the method specified in [36], read delay has been estimated as the time required by a sense amplifier to sense a 50 mV voltage difference between the bitlines BL and BLB. As is evident from Fig. 5 (a), which shows the T_{RA} of different cells at various V_{DD}, the S6T exhibits shorter read delay than 2T2R and 3T2R. This can be attributed

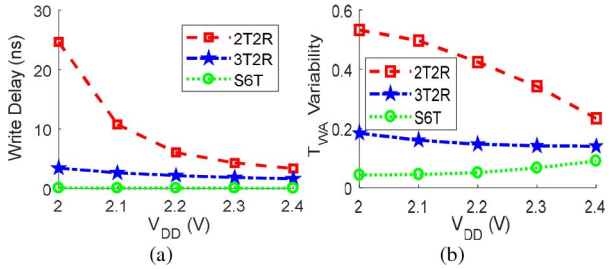

FIGURE 6. (a) T_{WA} and (b) T_{WA} variability of different cells at various V_{DD}.

to the absence of memristors, which leads to a low resistance path for BL/BLB to discharge through. The 3T2R cell exhibits a longer read delay than 2T2R due to the presence of CNFET switches between the bitlines and memristors, while the bitlines are directly connected to the memristors in the latter. Therefore, the 3T2R cell shows 1.82× and 1.75× longer read delay than S6T and 2T2R, respectively, at $V_{DD} = 2.0$ V.

Drift in resistance state is a major issue in memristor-based memory [37]. The resistance state may drift with multiple program/erase cycles as a voltage difference across the terminals of a memristor for a substantial amount of time leads to resistive switching due to migration of ionic charges inside it. However, this can be prevented by ensuring that the read process is very fast [37]. In particular, the read delay should be considerably shorter than the switching rate of the memristor, i.e., even if a fixed voltage is applied across the terminals of the memristors, switching will not occur if the duration of reading process is considerably shorter.

From Figs. 5 (a) and 6 (a), it can be observed that the switching time (write delay, see Section IV-B) of 3T2R is 47.78× longer than the time required for reading (read delay) at $V_{DD} = 2$ V. Thus, the reading process is fast enough to prevent state drift [38]. Moreover, state drift also depends on the duration and type of read pulse used [37]. Thus, to ensure that the stored data remains intact, the WL and WLB signals are applied for an appropriate amount of time to obtain a sufficient pulse width to complete the read operation successfully without damaging the stored data.

Process variation increases with device scaling and limits the performance of memory design in the submicron regime [36]. Fig. 5 (b) provides the variability in read delay of different cells at different V_{DD}. The use of CNFET devices instead of conventional CMOS devices in the proposed cell leads to the lowest variability in T_{RA} compared to the other cells in consideration. Therefore, from Fig. 5 (b), it is seen that the 3T2R cell exhibits 5.08× and 4.33× narrower spread in T_{RA} than S6T and 2T2R cells, respectively @ $V_{DD} = 2.0$ V.

B. WRITE DELAY (T_{WA})

Write access time, T_{WA}, or write delay is the time required to flip the data stored at the storage nodes of the memory cell. In the S6T cell, the write delay is estimated as the time required to raise the '0' (GND) storing node to 90% of the V_{DD} value [39]. For the memristor-based 2T2R and 3T2R cells, we have estimated T_{WA} as the time required by the memristor to reach 90% of R_{off} value from its initial R_{on} value. The write delay of the three cells at different V_{DD} are shown by Fig. 6 (a). The S6T cell shows the shortest T_{WA}. This can be attributed to the fact that a write operation in S6T involves the charging/discharging of a storage node only. On the contrary, writing in memristor-based cells involves changing the resistance state of the memristor, which takes a finite amount of time to occur. The 3T2R cell exhibits much shorter write delay compared to the 2T2R cell. This is because of the considerably higher current driving ability of CNFET compared to CMOS, which leads to faster change in the resistance state, R_{on} to R_{off}, of the memristor. Therefore, the 3T2R cell displays a 7.24× shorter write delay than the 2T2R cell at a supply voltage of 2 V.

From Fig. 6 (b), which represents the variability in T_{WA} of different cells at various supply voltages, it is seen that the memristor-based cells show higher variability than the S6T cell. This can be attributed to the intrinsic randomness that characterizes the mechanism of resistive switching in memristors during the write operation and leads to variations in switching behavior between distinct devices (known as device-to-device variations) or between different cycles in the same device (known as cycle-to-cycle variations) [40], [41]. However, when compared to 2T2R, the proposed 3T2R cell exhibits significantly lower (2.89×) variability due to the inherent advantageous characteristics of CNFET when compared to traditional CMOS.

TABLE 1. H_{PWR} values at different V_{DD}.

V_{DD} (V)	2T2R (pW)	S6T (μW)	3T2R (pW)
2.0	33.1	234	16.0
2.1	37.5	563	19.4
2.2	63.6	1061	33.2
2.3	123	2840	57.5
2.4	230	5410	81.3

C. HOLD POWER

As technology scales to deep submicrometer regime, hold power (H_{PWR}) dissipation has become a major roadblock in memory design as the memory cell remains in the standby mode for the majority of time [39]. Table 1 reports the H_{PWR} values of different cells at different supply voltages. It is observed that both 2T2R and 3T2R cells consume significantly lower hold power when compared to the S6T cell. The use of memristors in these cells implies that only WLB is needed to be maintained at V_{DD}, while all other control signals are grounded, which drastically reduces leakage power dissipation. On the contrary, the BL, BLB and V_{DD} of the S6T cell need to be provided with supply voltage to sustain the stored data. This leads to higher leakage current in MOSFET-based S6T resulting in higher power consumption. From Table 1, it is evident that the proposed cell consumes even lower hold power than the 2T2R cell. This

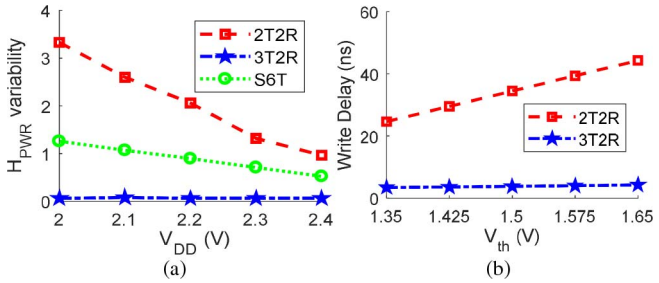

FIGURE 7. (a) Variability in H_{PWR} of different cells at various V_{DD} and (b) T_{WA} of the 3T2R and 2T2R cells at different Vth of memristor for $V_{DD} = 2$ V.

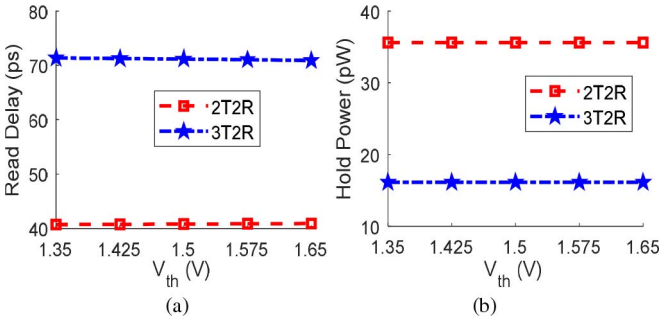

FIGURE 8. (a) T_{RA} and (b) H_{PWR} of the 3T2R and 2T2R cells at different V_{th} of memristor for $V_{DD} = 2$ V.

can be attributed to the vastly superior leakage characteristics of CNFET devices when compared to traditional CMOS devices, which are highly degraded due to short-channel effects [42].

Since H_{PWR} is a very important design metric of memory cell, the variability in H_{PWR} is an appropriate representative of the robustness of any memory cell. From Fig. 7 (a), it is seen that 3T2R shows lower variability in hold power than S6T and 2T2R cells at all the respective voltages.

V. VARIATIONS OF DESIGN METRICS WITH VTH OF MEMRISTORS

The need for multiple-cycle write-verify programming scheme, undesired drift in programmed resistance due to aging, as well as limited endurance of memristor devices are some of the limitations that plague memristor-based cells [41]. Such unwanted effects result in variation in V_{th} of the memristors.

Fig. 7 (b) presents a graphical representation of the impact of V_{th} variation on write time of 2T2R and 3T2R cells. A larger voltage drop is required across the terminals of a memristor to change its resistive state as V_{th} increases. CNFETs exhibit quicker switching ability owing to their lower V_t compared to MOSFETs. Therefore, there is negligible effect of V_{th} on the write time of proposed cell (see Fig. 7 (b)).

Read operation is a critical process in memristor-based cells owing to very high chances of data alteration, as discussed in Section III-B. Hence, a brief pulse is applied in such cases to complete the read operation successfully without altering the stored data in memristors by changing their memristances. The short interval of the pulse renders the effect of V_{th} on T_{RA} negligible in both 2T2R and proposed cells (see Fig. 8 (a)).

During the hold operation, almost all the control signals of both 2T2R and 3T2R are maintained at GND. Therefore, there is hardly any change in the hold power consumption with variation in V_{th} (see Fig. 8 (b)).

VI. VARIATION OF DELAY WITH TEMPERATURE

Temperature plays a key role in determining the performance of memristor-based memory cells. This is because various parameters which define the working of a memristive device are affected by change in temperature [43]. For example, the fundamental mechanism behind the switching activity of an oxide-based memristor is based on the hopping model which is determined by the migration of thermally activated ions [44]. However, the mobility of these ions/carriers is highly dependent on ambient temperature T_o and is responsible for determining the rate of switching as well as the conductivity levels of the device [44]. Moreover, rate of diffusion, charge carrier density and resistance states are also affected by changes in temperature. Therefore, the study of the impact of temperature variations on the characteristics of the cell is imperative. This is accomplished by carrying out the simulations for write and read time by varying temperature, in steps of five, from 27 °C to 125 °C at $V_{DD} = 2$ V.

In MOSFETs, increase in temperature leads to two decisive effects - decrease in threshold voltage and increase in scattering [45]. While the increase in scattering lowers the mobility of the MOSFETs and leads to decrease in driving current, the decrease in threshold voltage leads to increase in driving current. Since, the temperature dependence of driving current, in the saturation region, is predominantly dependent upon the carrier mobility [45], the drive current through the S6T cell, which is a purely MOSFET-based cell, is reduced and the write delay rises (see Fig. 9 (a), which depicts the T_{WA} of different cells at various temperatures for $V_{DD} = 2$ V).

However, the S6T cell exhibits the shortest T_{WA} amongst all comparison cells as its write operation only involves the charging/discharging of a storage node while that of memristor-based cells involves the resistive switching of memristors from one state to another. Since scattering mechanism is not dominant in CNFETs [46] because of long mean free path of carrier, the carrier mobility remains mostly unaffected by the increment in temperature. Therefore, one would expect the T_{WA} of MOSFET-based 2T2R and CNFET-based proposed design to increase significantly and marginally, respectively, with increase in temperature. However, their T_{WA} are dependent on the rate at which the memristances of the memristors change. Since, the mobility of oxygen ions increases with increase in temperature in HfO_x based memristors, the set/reset voltage and resistance-ratio

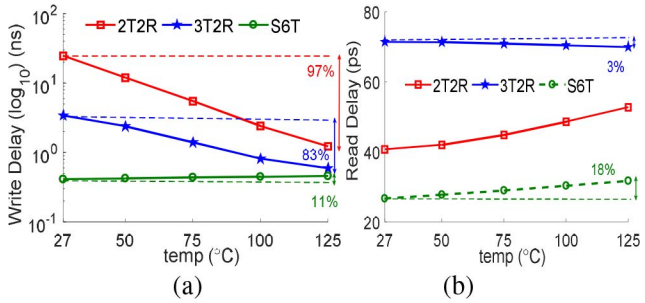

FIGURE 9. (a) T_{WA} and (b) T_{RA} of various cells at different temperatures for $V_{DD} = 2$ V.

of memristors decreases [47], [48]. Consequently, the rate of switching also increases with increase in temperature. Therefore, from Fig. 9 (a), it is observed that the T_{WA} of both 2T2R and 3T2R decreases with increase in temperature. However, the higher current driving ability of CNFETs, when compared to MOSFETs, leads to shorter T_{WA} in 3T2R than 2T2R.

Since the read delays of memristor-based 2T2R and 3T2R cells are not determined by the rate of switching, T_{RA} of these cells are hardly affected by any memristor-based effects of temperature. Instead, their read delay is dependent on the behaviour of MOSFETs and CNFETs when subjected to change in temperature. Since, decrease in mobility with temperature leads to lower current and slower response of the circuit, it inundates the effect of threshold voltage reduction and results in longer read delays with increase in temperature in the MOSFET-based 2T2R and S6T cells. This does not apply to CNFETs due to the negligible effect of scattering with rise in temperature. Therefore, the read time of 3T2R reduces marginally with rising temperature (see Fig. 9 (b)).

It must be noted from Fig. 9 (a)/9 (b), that the memristor-based 3T2R shows larger/smaller variation (between extreme temperature points) in T_{WA} (83%)/T_{RA} (3%) when compared to MOSFET-based S6T (11%)/(18%). This shows that the switching mechanism of memristors, which determines the write operation of 3T2R, is more susceptible to temperature variations when compared to the write operation of S6T cell. Although more susceptible to temperature variations, the write delay of 3T2R decreases with increase in temperature, which makes the device faster and hence, is acceptable. In addition, the proposed cell exhibits lower variation (83%) in T_{WA} than that of the 2T2R cell (97%) owing to the superior current carrying ability and chemically inert nature of CNFETs when compared to MOSFETs. The lower variation in T_{RA} of the proposed cell is an indication of the fact that the effects of temperature on memristor do not affect the read operation of 3T2R cell, while the read operation of S6T is considerably affected by the effect of temperature on the mobility of charge carriers in MOSFETs.

VII. IMPACT OF RTN ON RRAM DEVICE

Random telegraph noise (RTN) leads to current fluctuations in RRAM devices, especially in the high resistance

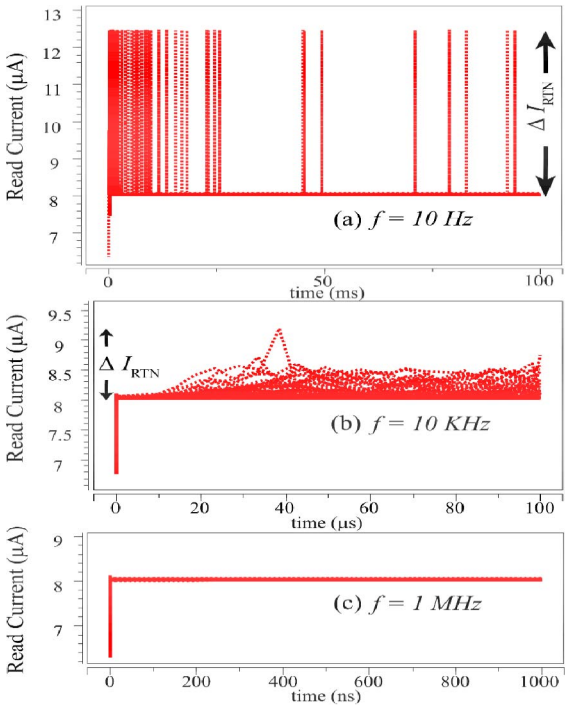

FIGURE 10. RTN induced fluctuations in read current at an operating frequency of (a) 10 Hz (b) 10 KHz and (c) 1 MHz.

state (HRS) [49]. Moreover, it is also known to induce read instability in memristor-based memory cells. This can be attributed to the fact that after every reset/set cycle, the CF is ruptured and reconstructed, which leads to a slightly different structure every time. As a result, fluctuations in read current and peak to peak read current values are produced which indicates instability in the read operation [50]. Therefore, it is necessary to consider the impact of RTN on the read operation of memristor-based circuits.

RTN is known to be a low-frequency phenomenon in CNFET devices and is prevalent below 1 KHz [51]. Moreover, current fluctuations due to RTN in RRAM devices also increases with decrease in operating frequency [50]. To verify the same, we have used the method adopted by authors in [50]. Accordingly, the read current obtained across memristors during read operation at different sampling rates under 5000 Monte Carlo simulations in HSPICE environment, have been plotted in Fig. 10. As is evident, the current fluctuation ($\Delta I_{RTN} = I_H$-I_L) at 10 Hz (see Fig. 10 (a)) is considerably higher than at 10 KHz (see Fig. 10 (b)) and is effectively nullified at a high frequency like 1 MHz (see Fig. 10 (c)).

Given that cache memory is capable of operating reliably at a very high frequency range (>> 1 MHz), RTN can be suppressed if the RRAM device is operated in the same range. Therefore, the proposed 3T2R RRAM cell operates at a frequency, much higher than 1 MHz, and is capable of mitigating the RTN induced instabilities.

VIII. CONCLUSION

A new 3T2R nonvolatile RRAM cell has been proposed in this paper. The half-select disturbance free nature of the cell renders it capable of implementing bit-interleaving architecture and thus, soft-errors can be mitigated using error correction coding (ECC) schemes. Emerging technologies like CNFET and memristor have been utilized to construct this cell owing to their immense potential. The proposed cell exhibits significantly shorter write delay than 2T2R while consuming considerably lower hold power when compared to both S6T and 2T2R. It also exhibits much lower variability in most of the design metrics when subjected to harsh process variations. Since, memristors are used, the nature of the RRAM cell is nonvolatile. Moreover, it is immune to resistance-state drift due to the application of optimized read operation and is unaffected by RTN induced instabilities due to its high frequency operation. In addition, the proposed cell is negligibly affected by variations in memristor threshold voltage owing to the inherently advantageous characteristics of CNFETs. Hence, the proposed 3T2R cell is a viable option for memory design applications.

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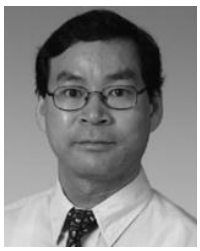

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