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InGaAs FinFETs 3-D Sequentially Integrated on FDSOI Si CMOS With Record Performance

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ABSTRACT In this paper, we demonstrate InGaAs FinFETs 3-D sequentially (3DS) integrated on top of a fully depleted silicon-on-insulator CMOS. Top layer III–V FETs are fabricated using a Si CMOS compatible HKMG replacement gate flow and self-aligned raised source-drain regrowth. We demonstrate that the low thermal budget of the top layer process does not affect the lower level FETs performance. An on-current of 200 μA/μm (at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V) is achieved, representing the highest reported for 3DS integrated III–V FETs on silicon, showing a 50% improvement in R_{ON} compared to previous work. The achieved improved performance can be attributed to the introduction of spacers, doped extensions underneath the gate region as well as improvements in the direct wafer bonding technique.

INDEX TERMS 3DS, III-V, FinFETs, sequential integration, wafer bonding, monolithic integration.

I. INTRODUCTION

Today the technology market is increasingly demanding low-power electronics, high-performance technology platforms and portable devices. Therefore, continuing the transistor scaling roadmap is necessary. While 2D scaling has reached several fundamental limitations due to power dissipation and fabrication challenges, 3D sequential (3DS) integration – the sequential fabrication of multiple transistor levels – is considered a key technology in the CMOS roadmap [1]. By exploiting the third dimension it is possible to increase the effective area used in the same footprint and enable added functionalities. Compared to 3D packaging using through-silicon vias, where levels are fabricated in parallel, then bonded together with low-resolution alignment, 3DS integration allows for alignment of subsequent levels as well as highly dense inter-level interconnects limited only by the resolution of the stepper. 3DS integration facilitates not only traditional scaling motivators [2]–[4], such as power density and delay reduction through shorter interconnects, but also "More than Moore" approaches, such as monolithic integration of functionally different layers, e.g., for photonics, RF and sensing. Key challenges of this technology include thermal budget management [5] and integration of channel layers with low defect density.

III-V materials [6], [7] are attractive in such systems, both as CMOS and RF performance boosters [8], [9] through high electron mobility, as well as enablers of new functionalities, e.g., as direct band gap materials. Hybrid solutions, combining Si CMOS and III-V channels [10], [11], furthermore, can leverage the low thermal budget process of III-V FETs [12], typically sub-600 °C, to avoid degradation of reliability and performance of the bottom level Si CMOS. We have previously demonstrated III-V InGaAs MOSFETs directly integrated on top of a pre-processed Si CMOS wafer [13]–[16], with InGaAs MOSFET performance approaching but not yet matching state-of-the-art InGaAs devices fabricated on silicon substrate [17]–[21], a challenging target due to the difference in fabrication complexity.

In this work we demonstrate InGaAs FinFETs using a Si CMOS-compatible low-thermal budget fabrication flow 3D sequentially integrated on Si CMOS. Through improved III-V wafer bonding and the implementation of a new device design including SiN_x spacers and raised-source-drain (RSD) doped extensions, devices with record I_{ON} for a 3DS III-V FET are demonstrated.

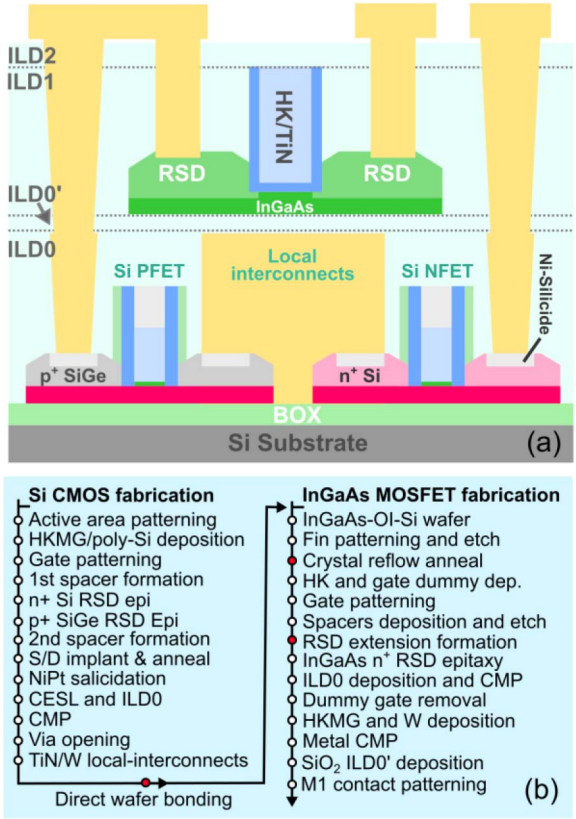

FIGURE 1. On top, schematic of the 3DS integrated stack, InGaAs nFETs on top of fully-depleted silicon-on-insulator Si pFETs and nFETs. A gate-first process is used for the Si CMOS and a RMG process for the InGaAs nFETs. Below, process flow schematic for the Si CMOS gate-first fabrication (left) and InGaAs nFET fabrication (right). Red dots indicate new or improved process modules in this work.

II. DEVICE FABRICATION

The 3DS integrated stack is composed of InGaAs FETs and FinFETs fabricated on top of a fully-depleted silicon-on-insulator (FDSOI) Si CMOS layer, as schematized in Fig. 1a. TiN/W contacts are used to connect the two tiers as well as for local interconnects. A standard gate-first FDSOI fabrication flow is carried out for the bottom Si CMOS layer [22]. The active device layer is patterned on a silicon-on-insulator (SOI) substrate and optimized gate high-k (HK) dielectric, gate metal and poly-Si gate are deposited on the mesas. Subsequently, gate patterning is followed by spacer formation. N^+-Si raised source/drain (RSD) is carried out for the nFET and p^+-SiGe for the pFET. Extension implants, both for n/pFET, and annealing is then performed, followed by spacer deposition and patterning. Highly doped source/drain contacts are obtaining by doping implantation and salicidation with Ni/Pt silicide.

A first inter-layer dielectric (IL0) is deposited and planarized by chemical-mechanical polishing (CMP). After that, vias are etched to the RSD contacts, filled out with TiN/W and subsequently planarized to form the interlayer contacts for the 3DS stack. Afterwards, a second thin inter-layer dielectric (IL0') is deposited on the Si CMOS devices and CMP is performed to planarize the layer. This represents a crucial step in achieving low-defect density and high mobility. In fact, a 20 nm $In_{0.53}Ga_{0.47}As$ layer is then sequentially integrated on the Si CMOS wafer by direct wafer bonding (DWB) [23]. The DWB starts with 2" active InGaAs layer as well as an InGaAs/InAlAs etch-stop heterostructure grown by Metal-Organic Chemical Vapor Deposition (MOCVD) on (100) InP substrate at 550 °C. Next, an Al_2O_3 adhesive layer is deposited on the III-V active layer. After cleaning the donor and substrate wafer by megasonic and ozone water, the wafers are brought to contact and annealed first at 100 °C then at 250 °C, for a total annealing time of two hours. The active III-V layer is then released from the donor wafer by wet etching in hydrochloric acid, stopping at the InGaAs/InAlAs etch-stop layers. The etch-stop layers are then selectively wet-etched slowly to stop on the active layer, which completes the DWB process.

Compared to our previously demonstrated 3DS integration platform [13], we modify the device design by introducing three new modules in the III-V FET fabrication flow. These the new modules consist in 4 nm SiN_x spacers, fins crystal reflow anneal, doped extensions underneath the spacers and improvements in the wafer bonding technique.

A replacement metal gate (RMG) fabrication is carried out on the top bonded layer for the nFETs fabrication. Planar and fins structures are patterned by electron beam lithography and dry etching. The as-patterned fins are then annealed in the MOCVD reactor under As overpressure at 500°C to reduce the sidewall roughness. The interlayer alignment accuracy is the same as in the Si CMOS layer. After active area patterning, the RMG fabrication flow starts by deposition of a dummy metal gate. Then the gate pattern is defined by e-beam lithography and dry etching and subsequently SiN_x spacers are deposited and formed by RIE. Doped extensions are formed by under-etching the III-V below the spacers with a digital etching (DE) process, as schematized in Fig. 3. The DE is performed in two steps: 8 min oxidation in a UV-Ozone chamber and etching in HCl:H2O (1:10) and the etching rate is about 1nm/cycle. This step is followed by self-aligned *in-situ* doped contacts formation. N^+InGaAs RSD epitaxy is done by metal-organic chemical vapor deposition (MOCVD). After depositing an etch-stop layer and an encapsulation oxide layer (ILD1), planarization by CMP and dummy gate removal is carried out. An optimized HK and metal gate featuring a scaled bilayer Al_2O_3/HfO_2 (approximately 0.5 nm/3 nm thick) dielectric and TiN metal are deposited on the exposed InGaAs channel. Afterwards, a new encapsulating ILD2 layer is deposited and again planarized. Finally, contact vias are opened and filled with W.

A STEM cross-section image of the fabricated InGaAs FET on top of Si pFET is shown in Fig. 2a whereas Fig. 2b shows a zoom-in view on the high-quality InGaAs channel, highlighting the 4 nm spacers as well as the HK layer.

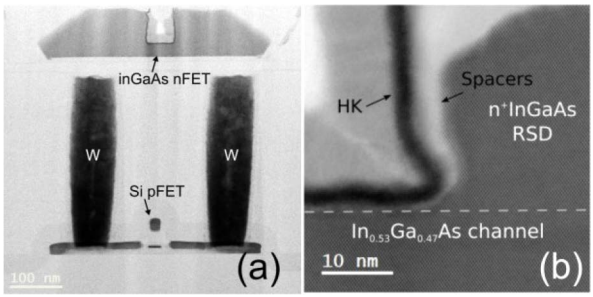

FIGURE 2. a) STEM cross-section of the 3DS integrated stack showing both transistor levels. Cross-section along the gate showing an InGaAs nFET with L_G = 60 nm on top of a Si pFET. W inter-layer contacts are also shown. b) Detailed STEM image of the InGaAs FET gate region featuring design A. High crystalline quality for the InGaAs channel is shown. The Al_2O_3/HfO_2 gate oxide and the approximately 4 nm thick SiN_x spacers are highlighted.

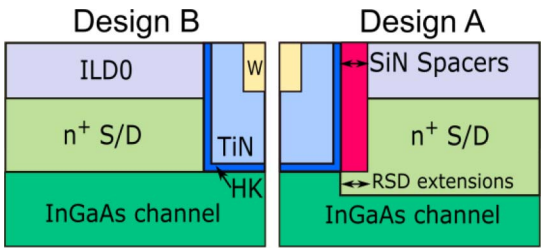

FIGURE 3. Schematic highlighting the implementation of spacers and RSD extensions in design A compared to design B.

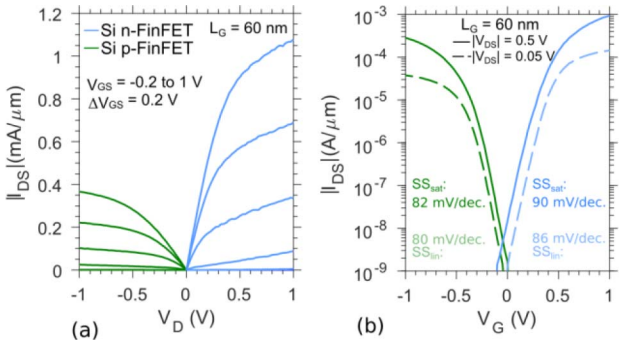

FIGURE 4. a) Output characteristic and b) subthreshold characteristic of Si n-FinFET (blue) and p-FinFET (green) with L_G = 60 nm after top-layer 3DS integration.

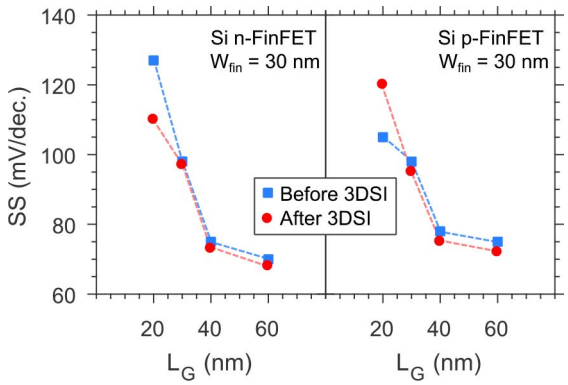

FIGURE 5. Subthreshold slope of Si CMOS n- and p-FinFETs in saturation, for devices with fin width of 30 nm before and after 3D sequential integration of the top III-V transistor level. Negligible change of SS is observed as a result of the 3DS integration.

III. RESULTS

Output and subthreshold characteristic, after 3DS integration, are shown in Fig. 4, for bottom level Si n-FinFET and p-FinFET devices with $L_G = 60$ nm showing well-behaved transistor characteristics. We have previously demonstrated interlayer functionality in III-V/Si 3D SRAM cells [13]. Fig. 5 shows subthreshold slope in saturation for Si p- and n-FinFETs with fin width of $W_{fin} = 30$ nm before and after 3DS integration of the top III-V transistor layer. No significant impact on the bottom layer is observed post-integration.

In the following, we report electrical results for InGaAs FinFETs from two different device designs, A and B (features summarized in Table 1). In this section, the impact on the electrical performance of the described technological implementations will be discussed.

In Fig. 6a, III-V FinFETs subthreshold characteristics for $L_G = 50$ nm devices are shown. For the design A, including spacers and RSD extensions, an excellent I_{ON} of 200 μA/μm is achieved, at $I_{OFF} = 100$ nA/μm and $V_{DD} = 0.5$ V. For the same device drain-induced barrier lowering (DIBL) of 80 mV/V and SS_{LIN} = 77 mV/dec is reported. The transconductance peaks at $g_m = 1.1$ mS/μm. With respect to the design B, we observe about one order of magnitude improvement in off-current as well as improved SS. Fig 6b shows the output characteristics for the designs A and B. Detailed analysis of the influence of the spacers on the off-state performance [24] as well as noise characterization [25] was reported elsewhere Fig. 7a shows the on-resistance R_{ON} versus gate lengths L_G, for the two different designs. R_{ON} is improved by approximatively 50% for the design A. We hypothesize that the reduction of R_{ON} could be explained by a lower defect density at the bonded InGaAs layer interface, yielding a higher electron mobility, obtained via improvements to the wafer bonding technique. The saturation of R_{ON} at short L_G may be caused by, e.g., SCE reducing g_m due to high output conductance. Another explanation is an inhomogeneous distribution of defects in the channel, particularly a higher density near the n^+ contact regions, causing a reduction of the effective mobility in scaled devices. Fig. 7b shows I_{ON} versus L_G for III-V FinFETs and planar FETs, featuring design A. For FinFETs, I_{ON} peaks at $L_G = 50$ nm, after which short-channel effects (SCE) impact SS. For planar devices, the I_{OFF} increases more strongly, limiting scalability, and at $L_G = 100$ nm, the $I_{OFF} = 100$ nA/μm target is no longer met.

Subthreshold slopes versus gate length and fin width are shown in Fig. 8a and 8b, respectively (design A). As also observed for I_{ON}, scaling L_G beyond 50 nm in FinFETs with $W_{fin} = 50$ nm causes SCE, increasing SS due to a lack of electrostatic control. Further scaling of W_{fin} will enhance off-state performance and scalability. For very long gate lengths

TABLE 1. Table summarizing the main technological features for the two wafers discussed in the results section.

Design	4 nm SiNx spacers	RSD extensions
A	✓	✓
B	-	-

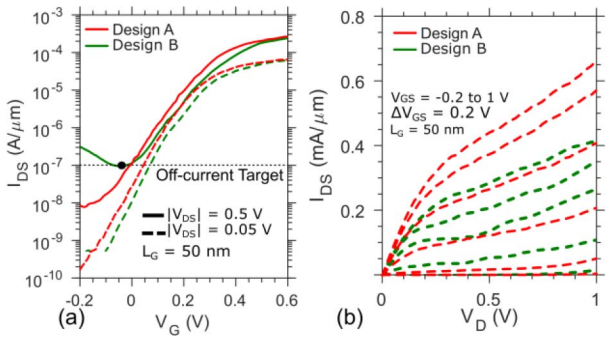

FIGURE 6. (a) Transfer characteristic of InGaAs FinFET for $L_G = 50$ nm for devices with design A (red) and B (green). The device with design A shows I_{ON} of 200 μA/μm (at $I_{OFF} = 100$ nA/μm and $V_{DD} = 0.5$ V), a record value for 3DS integrated InGaAs FET, enabled by SS in saturation of 92 mV/decade and transconductance of 1.1 mS/μm. Compared to design B, we achieve about one order of magnitude improvement in off-current as well as better SS. (b) Output characteristic from the same devices. On resistance extrapolated from the I_D/V_D characteristic at $V_{GS} = 1$V, results in a 50% improvement for the device featuring spacers.

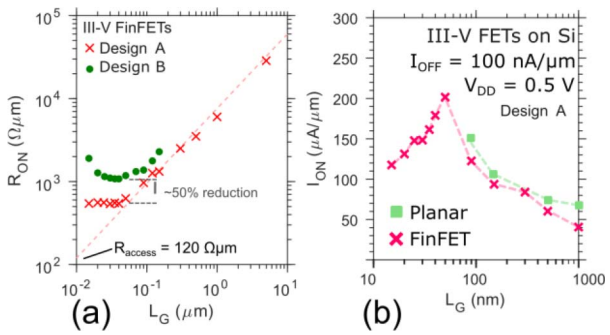

FIGURE 7. (a) R_{ON} versus L_G for III-V FinFETs structures comparing design A and B. A two-fold R_{ON} reduction at scaled gate lengths for design A is demonstrated. An access resistance of approximatively 120 Ωμm is extracted through linear extrapolation at $L_G = 0$ nm. (b) I_{ON} versus L_G for III-V Planar and FinFET structures with design A. I_{ON} peaks at $L_G = 50$ nm. Below $L_G = 50$ nm, short-channel effects degrade performance for FinFETs while planar scalability is limited to $L_G = 100$ nm by the off current.

($L_G > 5$ μm) planar devices outperform FinFETs due to fabrication-induced long-scale fin roughness.

Finally, for the same design, threshold voltage and DIBL behavior with L_G scaling is shown (Fig. 9a,b). V_T roll-off onset is observed at $L_G = 50$ nm for FinFETs and 500 nm for planar FETs. Similarly, a strong increase of DIBL is observed at 30 nm for FinFETs and 500 nm for planar FETs. Both cases indicate a strong increase of electrostatic control in FinFET devices.

Fig. 10 shows a benchmark of I_{ON} ($I_{OFF} = 100$ nA/μm and $V_{DD} = 0.5$ V) for state-of-the-art III-V-on-Si

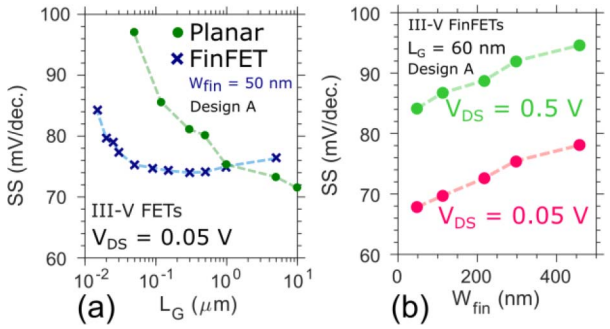

FIGURE 8. For design A, a) SS_{LIN} versus L_G for planar (green) and FinFETs (blue) structures. b) SS in linear and saturation region versus fin width.

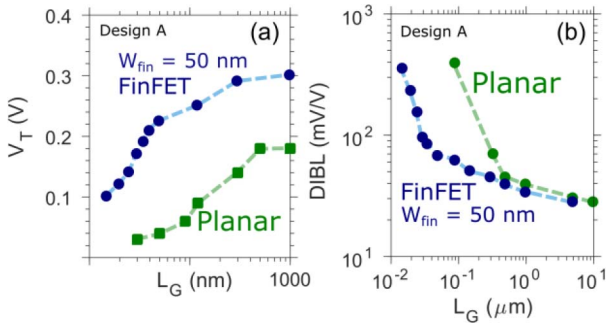

FIGURE 9. For design A, a) V_T versus L_G for planar (green) and FinFET (blue) devices with $W_{fin} = 50$ nm showing V_T roll-of onset at $L_G = 50$ nm. b) Drain-induce barrier lowering versus L_G for planar and FinFETs.

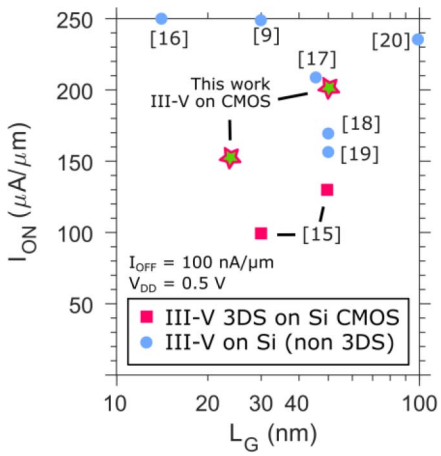

FIGURE 10. Benchmarking of I_{ON} versus L_G for 3DS integrated III-V FETs on Si (purple symbols) as well as non-3DS III-V on silicon (blue dots) works.

FETs, both with and without 3DS integration on Si CMOS [15], [17]–[21]. Peak I_{ON} at $L_G = 50$ nm represents the highest value reported for III-V FETs 3DS integrated on Si CMOS and approaching the record value for all III-V-on-Si devices, showing that III-V FETs can be 3DS integrated on processed substrates with minimal loss of performance.

IV. CONCLUSION

In this work we have demonstrated InGaAs FinFETs 3DS integrated on FDSOI Si CMOS. The low thermal budget of the III-V top layer fabrication flow enabled maintained Si CMOS performance post-3DS integration. By improvements to the wafer bonding technique and the implementation of a new device design featuring SiN_x spacers and raised-source-drain (RSD) doped extensions, we achieved a record I_{ON} of 200 μA/μm for 3DS integrated III-V FETs on Si. The resulting performance is approaching the record for all III-V-on-silicon FETs. These results show that 3DS integration of high-performance III-V FETs on Si CMOS can be performed with minimal performance degradation in both transistor levels.

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REFERENCES

[1] A. Mallik *et al.*, "The impact of sequential-3D integration on semiconductor scaling roadmap," in *Proc. Int. Electron Devices Meeting (IEDM)*, 2017, pp. 32.1.1–32.1.4.
[2] P. Batude *et al.*, "3D sequential integration: Application-driven technological achievements and guidelines," in *Proc. Int. Electron Devices Meeting (IEDM)*, 2017, pp. 3.1.1–3.1.4.
[3] M. Vinet *et al.*, "Monolithic 3D integration: A powerful alternative to classical 2D scaling," in *Proc. SOI-3D Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, 2014, pp. 17–19.
[4] P. Batude *et al.*, "3DVLSI with CoolCube process: An alternative path to scaling," in *Proc. Symp. VLSI Technol.*, Kyoto, Japan, 2015, pp. T48–T49.
[5] G. R. K. Triantopoulos *et al.*, "Thermal effects in 3D sequential technology," in *Proc. Int. Electron Devices Meeting (IEDM)*, 2017, p. 7.
[6] H. Riel, L. E. Wernersson, M. Hong, and J. A. Del Alamo, "III–V compound semiconductor transistors—From planar to nanowire structures," *MRS Bull.*, vol. 39, no. 8, pp. 668–677, 2014.
[7] J. A. Del Alamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, 2011.
[8] C. B. Zota, C. Convertino, Y. Baumgartner, M. Sousa, D. Caimi, and L. Czornomaz, "High performance quantum well InGaAs-On-Si MOSFETs with sub-20 nm gate length for RF applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2018, pp. 39.4.1–39.4.4.
[9] C. B. Zota *et al.*, "InGaAs-on-insulator MOSFETs featuring scaled logic devices and record RF performance," in *Proc. IEEE Symp. VLSI Technol.*, 2018, pp. 165–166.
[10] C. B. Zota, F. Lindelow, L.-E. Wernersson, and E. Lind, "InGaAs tri-gate MOSFETs with record on-current," in *Proc. Int. Electron Devices Meeting (IEDM)*, 2016, pp. 3.2.1–3.2.4.
[11] X. Sun *et al.*, "High performance and low leakage current InGaAs-on-silicon FinFETs with 20 nm gate length," in *Proc. Symp. VLSI Technol.*, 2017, pp. 40–41.
[12] J. Micout *et al.*, "High performance low temperature FinFET with DSPER, gate last and self aligned contact for 3D sequential integration," in *Proc. Int. Electron Devices Meeting (IEDM)*, 2017, pp. 32.2.1–32.2.4.
[13] V. Deshpande *et al.*, "Demonstration of 3-D SRAM cell by 3-D monolithic integration of InGaAs n-FinFETs on FDSOI CMOS with interlayer contacts," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4503–4509, Nov. 2017.
[14] V. Deshpande *et al.*, "Three-dimensional monolithic integration of III–V and Si(Ge) FETs for hybrid CMOS and beyond," *Jpn. J. Appl. Phys.*, vol. 56, no. 4S, Apr. 2017, Art. no. 04CA05.
[15] V. Deshpande *et al.*, "First demonstration of 3D SRAM through 3D monolithic integration of InGaAs n-FinFETs on FDSOI Si CMOS with inter-layer contacts," in *Proc. Symp. VLSI Technol.*, 2017, pp. T74–T75.
[16] C. Convertino, C. B. Zota, D. Caimi, M. Sousa, and L. Czornomaz, "InGaAs FinFETs 3D sequentially integrated on FDSOI Si CMOS with record performance," in *Proc. 48th Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2018, pp. 162–165.
[17] H. Hahn *et al.*, "A scaled replacement metal gate InGaAs-on-Insulator n-FinFET on Si with record performance," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2017, pp. 17.5.1–17.5.4.
[18] X. Zhou *et al.*, "Scalability of InGaAs gate-all-around FET integrated on 300mm Si platform: Demonstration of channel width down to 7nm and Lgdown to 36nm," in *Proc. Symp. VLSI Technol.*, 2016, pp. 1–2.
[19] N. Waldron *et al.*, "Gate-all-around InGaAs nanowire FETS with peak transconductance of 2200μS/μm at 50nm Lg using a replacement Fin RMG flow," in *Tech. Dig. Int. Electron Devices Meeting (IEDM)*, 2015, pp. 31.1.1–31.1.4.
[20] V. Djara, V. Deshpande, M. Sousa, D. Caimi, L. Czornomaz, and J. Fompeyrine, "CMOS-compatible replacement metal gate InGaAs-OI FinFET with ION = 156 μA/μm at VDD = 0.5 V and IOFF = 100 nA/μm," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 169–172, Feb. 2016.
[21] M. L. Huang *et al.*, "In 0.53Ga0.47As MOSFETs with high channel mobility and gate stack quality fabricated on 300 mm Si substrate," in *Proc. Symp. VLSI Technol.*, 2015, pp. T204–T205.
[22] S. Barraud *et al.*, "Scaling of Ω-gate SOI Nanowire N- and P-FET down to 10nm gate length: Size- and orientation-dependent strain effects," in *Proc. Symp. VLSI Circuits*, 2013, pp. 230–231.
[23] L. Czornomaz *et al.*, "An integration path for gate-first UTB III-V-on-insulator MOSFETs with silicon, using direct wafer bonding and donor wafer recycling," in *Tech. Dig. Int. Electron Devices Meeting (IEDM)*, 2012, pp. 517–520.
[24] C. Convertino *et al.*, "InGaAs-on-insulator FinFETs with reduced off-current and record performance," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2018, pp. 39.2.1–39.2.4.
[25] T. A. Karatsori *et al.*, "Static and low frequency noise characterization of InGaAs MOSFETs and FinFETs on insulator," in *Proc. 48th Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2018, pp. 166–169.