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Robust Gate Driver on Array Based on Amorphous IGZO Thin-Film Transistor for Large Size High-Resolution Liquid Crystal Displays

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ABSTRACT Amorphous IGZO thin-film transistors (TFTs) in an etch stop layer (ESL) structure was processed on 2500 mm × 2200 mm size substrate. The fabricated devices exhibit enhancement mode characteristics, and excellent uniformity over large area. The presented good operational stabilities under both positive gate bias temperature stress (PBTS) and negative gate bias temperature stress (NBTS) tests can well meet the requirements for pixel switching. However, considering even threshold voltage shift under long term positive bias stress might affect proper operation of the gate driver on array (GOA), a design with a pulse gating scheme is proposed, consisting of 13 TFTs and 1 capacitor, to avoid long term continuous bias stressing of the TFT. With the proposed GOA design, a 32-inch QUHD (7680×4320) high-resolution liquid crystal display (LCD) panel with a 7 mm wide bezel is achieved. The reliability of the GOA circuit is well proved through standard aging tests.

INDEX TERMS Thin-film transistor, IGZO, gate driver, stability.

I. INTRODUCTION

The amorphous indium gallium zinc oxide (a-IGZO) TFT has been regarded as a promising backplane technology for developing large size high resolution displays, including liquid crystal displays (LCDs) and organic light emitting diode (OLED) displays [1], [2]. Compared to amorphous silicon TFTs, the a-IGZO TFT owns much improved mobility and operational stability, while maintaining similar processing complexity and device uniformity suitable for large area and low-cost manufacturing [3], [4]. Such amorphous metal oxide semiconductor TFTs may also exhibit attractive features of ultra-low off-state leakage and steep subthreshold swing for developing low power displays with lower frame rate and reduced scanning voltage [5], [6].

To achieve high resolution displays with narrow bezel, the gate driver circuits need to be integrated on the panel with the pixel array based on the TFT technology, so called gate driver on array (GOA) [7]. With the a-IGZO TFT, the GOA circuits become much easier to be implemented compared to that with a-Si TFTs. However, the non-ideal characteristics of a-IGZO TFTs still bring design challenges. Firstly, the depletion mode characteristics of a-IGZO TFTs with large leakage current at zero gate to source bias (V_{GS}) cause large power consumption and even malfunction with the conventional GOA circuit design. Many designs have thus been proposed to address this issue [8]–[10]. Secondly, the operation of GOA circuits needs more stable and uniform TFTs compared to that of pixel switches, especially for large size TV applications [11]. Small threshold voltage variation of a-IGZO TFTs induced by processes or long-term operation might result in deterioration of the circuits [12], [13]. To address these issues, many circuit designs have been proposed in the past, which, however, increase the circuit complexity and thus the layout area [14]–[17]. Moreover, very few of

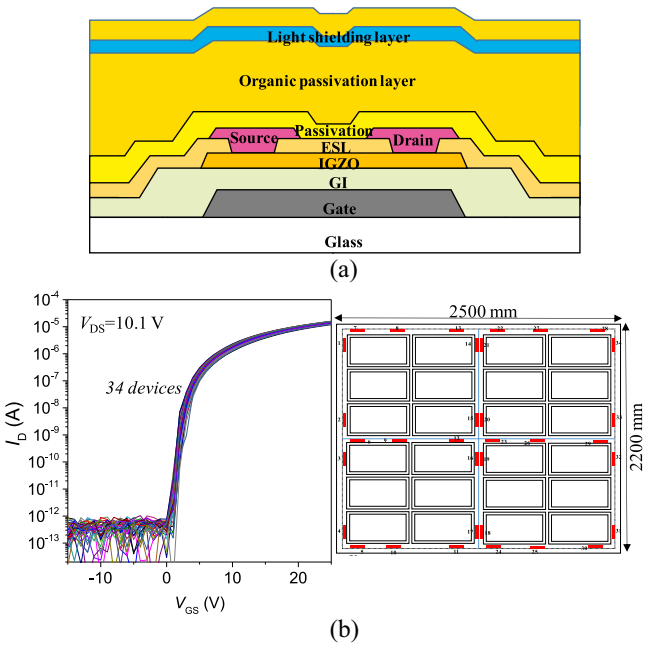

FIGURE 1. **(a) Schematic of the cross-sectional structure of the fabricated a-IGZO TFTs in an inverted stagger structure with an etching stop layer (ESL), and (b) the measured transfer characteristics (I_D-V_{GS}) of 34 devices with the channel width of 25 μm and the channel length of 8 μm at V_{DS} = 10.1 V over a 2500 × 2200 nm size substrate.**

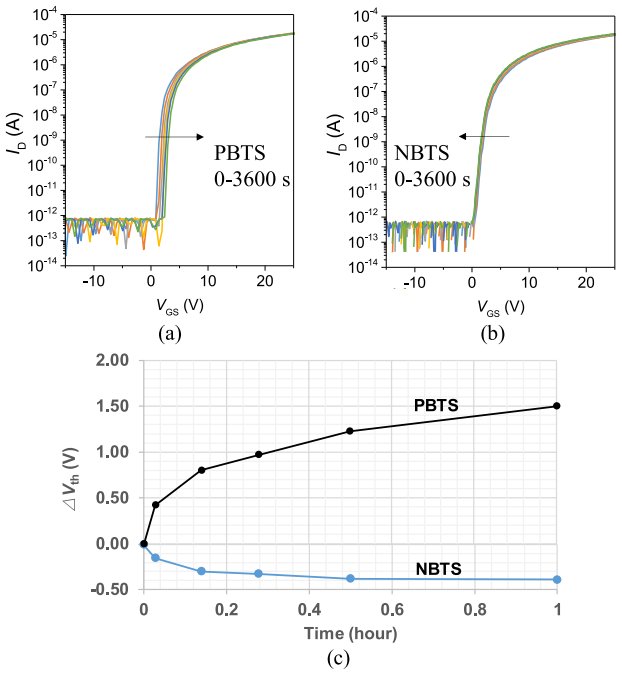

FIGURE 2. **The measured transfer characteristics (I_D-V_{GS}) at V_{DS} = 10.1 V under (a) positive bias temperature stress (PBTS) and (b) negative bias temperature stress (NBTS) at 60 °C for 3600s. (c) The extracted V_{th} shifts over the stress time under PBTS and NBTS.**

these designs were realized with large area manufacturing processes, and their functionalities were not verified through standard reliability tests.

In this work, the etch stop layer (ESL) structure was adopted for processing a-IGZO TFTs because of its robustness to variations of process conditions and capability of achieving higher device performance than the back-channel etch (BCE) structure. The fabricated devices exhibit enhancement mode characteristics, and excellent uniformity over a 2500 mm×2200 mm size Gen 8 large area substrate. The presented good operational stabilities under both positive gate bias temperatures stress (PBTS) and negative gate bias temperature stress (NBTS) can well meet the requirements for pixel switching. However, considering even slight V_{th} shift under long term bias stress might still affect proper operation of the GOA circuits, a GOA design with a pulse gating scheme is proposed, consisting of 13 TFTs and 1 capacitor, to avoid long term continuous bias stress of the TFT. With the proposed GOA design, a 32-inch QUHD (7680×4320) high resolution liquid crystal display (LCD) panel with a 7 mm wide bezel is achieved. The reliability of the GOA circuit is well proved through standard aging tests.

II. DEVICE STRUCTURE AND PERFORMANCE

Fig. 1(a) shows the cross-sectional structure of the fabricated a-IGZO TFTs in an inverted stagger structure with an ESL to protect the channel in the processes. The source, drain and gate electrodes are formed with copper. A light shielding structure is adopted to reduce the effects of light illumination. The measured transfer characteristics (I_D-VGS) of 34 devices over a 2500 mm×2200 mm size substrate as given in Fig. 1(b), showing excellent uniformity. The channel width and length are 25 μm and 8 μm, respectively. The average mobility is 9 cm^2/V·s. Fig. 2(a) and (b) present the measured ID-VGS at VDS=10.1 V under positive bias temperature stress (PBTS) and negative bias temperature stress (NBTS) at 60 °C for 3600s. The PBTS was carried out at V_{GS} = 30 V and V_{DS} = 0, and the NBTS was with V_{GS} = −30 V and V_{DS} = 0. The extracted Vth shifts over the stress time under PBTS and NBTS are given in Fig. 2(c). It can be seen that, after 1 hour continuous stress, there was a V_{th} shift of about 1.5 V with PBTS and about 0.4 V with NBTS. The stability of devices is good enough for pixel switches. However, the operation of GOA circuits is more sensitive to the V_{th} variation.

III. GOA CIRCUIT DESIGN

In a basic GOA circuit design, as illustrated in Fig. 3(a), the pull-up TFT M2 needs to be of a relatively large channel width-to-length ratio to provide enough current driving capability for charging the gate line (G(n)), resulting in large gate to drain parasitic capacitor of M2 (C_{GD}). During the OFF state of M2, transition of the clock signal (CLK) will cause a voltage coupling to the gate of M2 (netA(n)) with clock feedthrough via C_{GD} of TFT1. If the induced voltage change is larger than V_{th} of M2, abnormal outputs to the gate line will occur. By using a larger boot-trap capacitor (C_b), clock feedthrough can be reduced, but the charging/discharge speed will be affected. An effective approach is to add a circuit

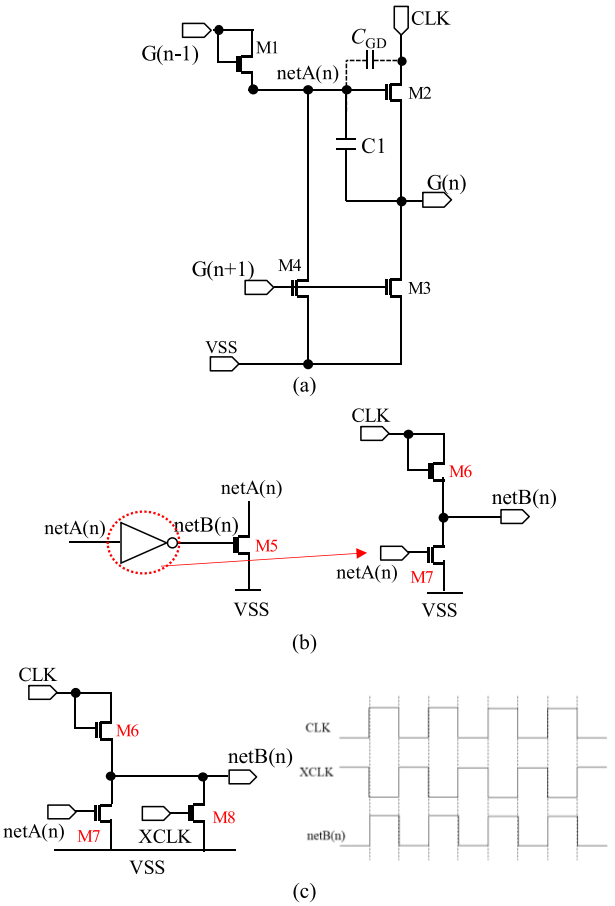

FIGURE 3. **(a) Schematic of the basic GOA circuit design. (b) Schematic of a circuit unit being added in the GOA circuit in (a) to stabilize the voltage at netA(n). (c) Schematic of the circuit design to replace the inverter in (b) for pulse gating of M5.**

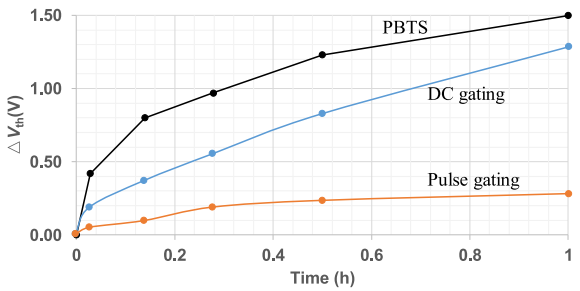

FIGURE 4. **Comparison of the measured V_{th} shifts under the DC and pulse gating methods with the PBTS test results for the fabricated IGZO TFT.**

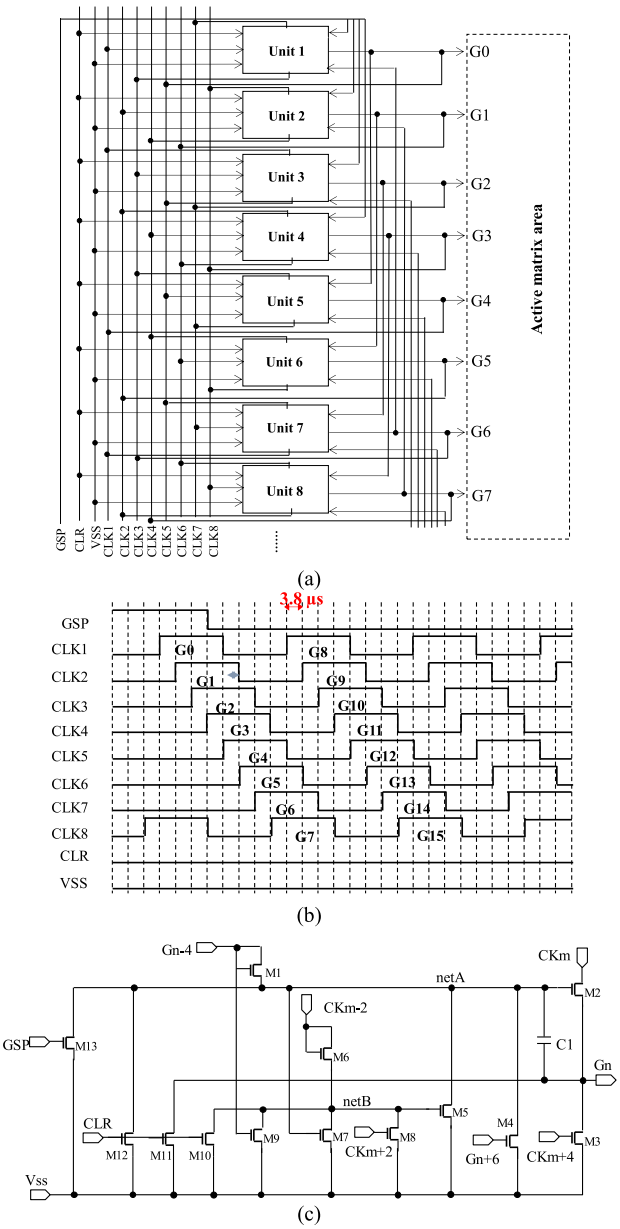

FIGURE 5. **(a) Illustrate of the implemented 8 clock GOA architecture. (b) Timing of all the input control signals. (c) Diagram of the unit GOA circuit composed of 13 TFTs.**

unit to stabilize the voltage at netA(n), as shown in Fig. 3(b). The circuit consists of an inverter and a pull-down TFT M5. Once netA (n) is high, netB (n) will go low, thus turning M5 off to maintain the voltage level at netA(n). NetA (n) and G (n) are discharged to VSS, when netA (n) is low and netB (n) is high. However, because during most time of each frame, netA(n) is low and netB(n) is high, the holding TFT M5 will be under nearly continuous positive bias stress (DC gating) over long operation time. As a result, a certain positive shift will occur. With a too positive V_{th}, M5 will not be able to sufficiently discharge netA(n), causing noise at G(n) and risk of failure for the circuits.

To address this issue, a pulse gating method is used as shown in Fig. 3(c). An additional TFT M8 is added in the circuit, and controlled by the clock signal XCLK, which is complementary to CLK. Since M6 and M8 are alternately turned on under control of CLK and XCLK, respectively, the voltage level at netB(n) becomes periodically high, effectively reducing the bias stress time at M5. Fig. 4 compares the measured V_{th} shifts under the two different methods with that obtained under PBTS. It can be seen with M8 and its control clock XCLK, the pulse gating method can help to effectively decrease V_{th} shift of M5 over long time operation.

TABLE 1. Values of the design parameters of the TFTs (M1-M13) and the capacitor (C1) in the circuit (Fig. 5c) (for TFTs, the given value is channel width/channel length in μm).

M1	M2	M3	M4	M5	M6	M7
210/8	2400/8	52.5/8	25/8	210/8.5	5/20	30/8
M8	**M9**	**M10**	**M11**	**M12**	**M13**	**C1**
5/8	10/8	5/8	36/8	5/8	10/8	1 pF

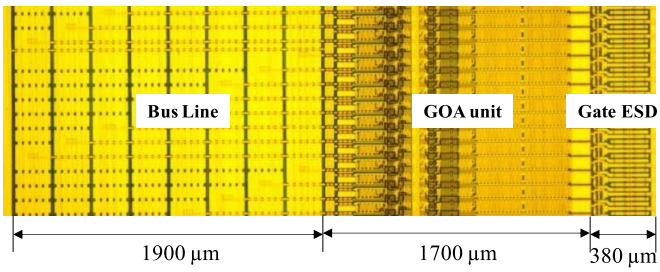

FIGURE 6. Photo image of the overall GOA including the bus line and ESD protection parts.

IV. IMPLEMENTATION OF THE GOA

Based on this design, an 8 CLK GOA architecture, as depicted in Fig. 5 (a), is implemented in a 32 inch QUHD LCD panel. The operation timing of all the input control signals is given in Fig. 5(b). The pulse width of the gate output waveform is designed to be 15.2 μs. More clock signals can help to reduce the parasitic capacitance on each CLK line, and thus decrease RC delay. For the 32 inch QUHD display, the row selection time is quite short, and thus such an 8 CLK design is needed. For lower resolution displays, design with less CLK signals can be used. The multi-clock design is also able to reduce the power consumption. The unit circuit, as shown in Fig. 5(c), adopts the pulse gating method, consisting 13 TFTs and 1 capacitor. In the circuit, additional TFTs M9/M10/M11/M12/M13 are added to clear the critical node charges before the circuit starts to operate. The design parameters of the TFTs and the capacitor are listed in Table 1. The photo image of the overall GOA including the bus line and ESD protection parts is given in Fig. 6 with the total width less than 4 mm.

With this GOA, a 32 inch QUHD (7680 RGB $\times$ 4320) high resolution LCD panel with a 7 mm wide bezel was achieved. The measured power consumption of the GOA is about 360.3 mW. To verify the reliability of the GOA, the whole panel was placed under standard aging tests, including storage at high temperature (70°C) and low temperature ($-$20°C) for 240 hours, operation at high temperature (60°C) and low temperature ($-$20°C) for 240 hours, storage and operation at high temperature (60°C) and high humidity (RH of 90%) for 24 hours, being turned ON/OFF for 30000 cycles, and ESD test at 15 kV. After all the aging tests, the display can work normally without any defects as shown in Fig. 7. The measured output voltage waveform of the 4320th gate line (G4320) is given in Fig. 8, indicating proper operation of the GOA. The results can well prove that designed GOA has good enough reliability for large area high resolution LCDs.

Specifications	Value
Panel Size	712 mm×406 mm (32 inch)
Resolution	7680 RGB×4320 (QUHD)
Bezel width	7 mm

FIGURE 7. Photo image of the 32 inch QUHD LCD panel using the designed GOA after aging tests and the specifications of the panel.

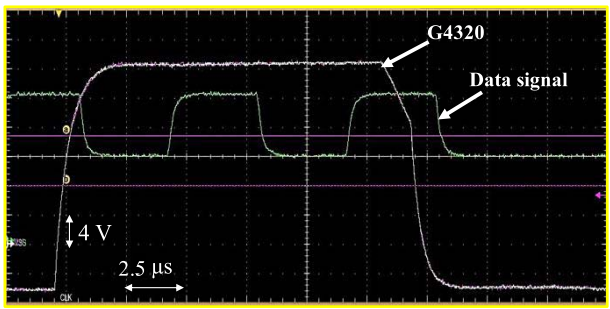

FIGURE 8. The measured output voltage waveform of the 4320th gate line (G4320) of the fabricated 32 inch QUHD LCD panel.

V. CONCLUSION

In summary, GOA was designed and implemented based on the a-IGZO TFT processed on Gen 8 substrate. The TFT devices exhibited excellent uniformity over large area. To improve the robustness of the GOA to long term operation, a pulse gating scheme is adopted to avoid the TFTs to be operated with long term bias stress. The GOA was integrated to achieve a 32 inch QUHD (7680 RGB $\times$ 4320) high resolution LCD panel with a narrow bezel. Good reliability was well proved through standard aging tests.

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