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A Trench LDMOS Improved by Quasi Vertical Super Junction and Resistive Field Plate

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ABSTRACT An improved trench lateral double-diffused MOSFET (T-LDMOS) is proposed. It has a quasi vertical super junction (QVSJ) drift region and adopts a resistive field plate (RFP) to help QVSJ satisfy charge-balance. The realization of RFP barely complicates the device fabrication, but it motivates QVSJ to significantly improve the relationship between breakdown voltage (BV) and specific on-state resistance ($R_{ON,SP}$). The simulation results show that compared with the conventional QVSJ T-LDMOS, the proposed one gains the $R_{ON,SP}$ reduced by about 79% under the same BV requirement of about 500 V. It therefore presents an excellent figure of merit (FOM) (FOM = $BV^2/R_{ON,SP}$, Baliga's FOM) up to 29.8 MW/cm^2, which is superior to the prior art and exhibits a bright prospect of saving energy.

INDEX TERMS Trench LDMOS (T-LDMOS), quasi vertical super junction (QVSJ), resistive field plate (RFP).

I. INTRODUCTION

As a famous power device, the lateral double-diffused MOSFET (LDMOS) is widely used in power ICs since its coplanar electrodes facilitate the system integration on one chip. However, to sustain enough voltage between the surface electrodes in the off-state, it usually requires a fairly wide drift region, which leads to a strained relationship between the breakdown voltage (BV) and the specific on-resistance ($R_{ON,SP}$). This finally leads to enormous power loss [1].

To make LDMOS more efficient, a kind of trench LDMOS (T-LDMOS) is developed [2]–[3]. It uses a deep and narrow trench filled with dielectric to sustain most of the surface voltage. Since the trench equivalently increases the drift region length in the bulk silicon and the dielectric usually has a much stronger breakdown strength than silicon, the device width can be considerably reduced for a target BV. As a result, the value of $R_{ON,SP}$, which is calculated as the on-state resistance multiplied by the chip area, is able to be reduced.

Based on the common structure of T-LDMOS, many improved structures are proposed [4]–[12], such as the ones with vertical field plates in the trench [7]–[9], and the ones with variable-k trench-dielectric [10]–[12]. Recently, many studies start applying a well-known technique of super junction (SJ) to the LDMOS [13]–[16], as well as to the T-LDMOS [17]–[20], such as the T-LDMOS with a quasi vertical (QV) SJ structure [17], [19], [20] and that with a lateral SJ structure at the trench bottom [18]. However, because the trench acts as a capacitor in the off-state and disturbs the surface electric-field (e-field) distribution [19], a QVSJ structure in T-LDMOS is hard to satisfy the important charge-balanced condition and, therefore, cannot be fully used to improve the device performance. Although some studies have paid attention to deal with that, they mostly rely on some costly process to realize the complex structures, such as the drift region with the variation vertical doping [19] and the trapezoidal trench [20].

In this paper, a new QVSJ T-LDMOS is proposed and studied by simulation. It features a resistive field plate (RFP) which is embedded in the trench and surrounded by the QVSJ drift region. Since RFP can modulate the surface e-field distribution [16], [21]–[24] and eliminate the impact of the trench capacitor, the QVSJ region in this device is able to satisfy the charge-balanced condition. Moreover, because

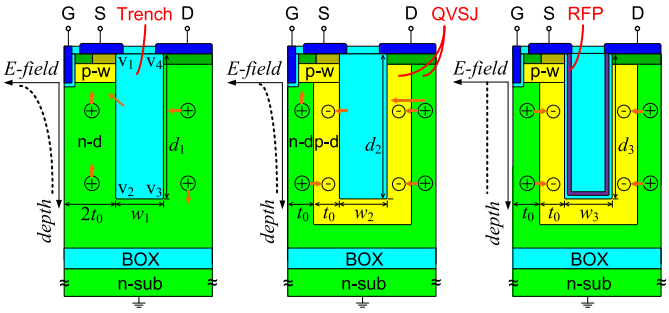

FIGURE 1. Cross section views of (a) the common T-LDMOS (TLD) and (b) the conventional one with QVSJ (TLD+QVSJ) and (c) the proposed one with QVSJ and RFP (TLD+QVSJ+RFP). The points of v_1, v_2, v_3 and v_4 are the trench vertexes. The symbols of "⊕" and "⊙" stand for some ionized donors and acceptors, respectively. The orange arrows show directions of some important e-flux. The e-field distributions are that on the left side of the trench.

the realization of RFP does not need any additional mask, the fabrication process is barely complicated. The structure and theory for the proposal will be described in the following.

II. STRUCTURE AND THEORY

Fig. 1(a) shows the common T-LDMOS (TLD), which is implemented on a silicon-on-insulator (SOI) substrate. Under the buried oxide layer (BOX), an n-type substrate (n-sub) is always connected to the ground. Above the BOX, a trench filled with dielectric is embedded into the middle of an n-type drift region (n-d). On the left of the trench, there are a p-type well region (p-w) and two electrodes of gate (G) and source (S). On the trench right, there is an electrode drain (D).

In the off-state, D is connected to the highest voltage while S and G are both grounded. Most of the surface voltage between D and S (V_{DS}) is sustained by the trench. Since the dielectric in the trench, e.g., SiO_2 or benzocyclobutene (BCB), has much stronger breakdown strength than silicon, the device width (w_1) can be pretty small. On the other hand, V_{DS} is also sustained in the bulk silicon along the path of $v_1 \rightarrow v_2 \rightarrow v_3 \rightarrow v_4$. Compared with a traditional LDMOS without the trench, the drift region length is equivalently increased, which enables TLD to sustain more reverse voltage within the same device width.

However, TLD has two disadvantages. First, the doping concentration of n-d ($N_{dn\text{-}1}$) has to be prudentially controlled for a target BV. According to Poisson equation, $N_{dn\text{-}1}$ mainly determines the slope of the surface e-field distribution which is along the path of $v_1 \rightarrow v_2 \rightarrow v_3 \rightarrow v_4$. A higher $N_{dn\text{-}1}$ is commonly associated with a more sloped e-field distribution as well as a smaller BV. Second, the trench produces not only benefits but also forfeits. It acts as a capacitor (C_{trench}) taking the adjacent semiconductor regions as the plates. In TLD, the negative plate is p-w and the positive one is the n-d on the right side of the trench. When the device is in the off-state, C_{trench} expropriates the electric flux (e-flux) emitted by the ionized donors in the positive plate and sends it to p-w via the left n-d. Therefore, the e-field peak beside p-w is further increased and BV is impaired. To obtain enough BV, TLD has to increase w_1 with the purpose of reducing C_{trench} and decrease $N_{dn\text{-}1}$ to flat the surface e-field distribution, which both lead to an increase in $R_{ON,SP}$.

Fig. 1(b) shows the conventional QVSJ T-LDMOS (TLD+QVSJ), where the drift region is a QVSJ structure consisting of n-d and a p-type layer (p-d). In the off-state, QVSJ is depleted. If it is charge-balanced, namely the e-flux emitted by the ionized donors in n-d is fully absorbed by the ionized acceptors in p-d, the surface e-field distribution will no longer be threatened by the doping concentration of n-d ($N_{dn\text{-}2}$). Unfortunately, due to the aforementioned impact of C_{trench}, QVSJ here is hard to realize charge-balance. In Fig. 1(b), the negative plate of C_{trench} contains the p-d on the left of the trench. The e-flux transited by C_{trench} is partly absorbed by the ionized acceptors in the left p-d. This hinders the left p-d from compensating the left n-d. Moreover, since the voltage applied on C_{trench} is vertically varying, from that as high as V_{DS} on the surface to that being very small at the trench bottom, C_{trench} impacts the e-flux flowing with different intensity at different depth. As a result, if QVSJ is controlled to be charge-balanced at one depth and one side of the trench, it is undoubtedly charge-imbalanced at another depth or another side. Thus, although TLD+QVSJ can have an enhanced $N_{dn\text{-}2}$ due to the charge compensation effect and can have a reduced e-field peak beside p-w, it needs adequate trench width (w_2) to weaken the impact of C_{trench} as well as the degree of charge-imbalance.

Fig. 1(c) shows the proposed device (TLD+QVSJ+RFP), which features an additional RFP layer. Due to the excellent ability to modulate the e-field distribution, RFP has been widely used in power devices for many years [21]. Most of the RFP films are implemented by semi-insulating poly-crystalline silicon (SIPOS), which can be deposited with uniform thickness and uniform resistivity [22]. In the proposed device, the both ends of RFP are connected to the surface electrodes. When the device sustains a reverse voltage, a current is flowing from D to S along RFP. Since the resistivity of SIPOS is usually within the range of 1×10^8 to $1\times10^{10}\Omega\cdot$cm [21], the current is so weak that it barely increases the power loss. But the current is able to produce a uniform potential distribution on the RFP layer, which modulates the surface e-field distribution to be flat and protects the QVSJ structure from the impact of C_{trench}. Therefore, in the design of the proposed device, people can reduce the trench width (w_3) and increase the doping concentration of n-d ($N_{dn\text{-}3}$) as far as possible in theory. The advantages of the trench and the SJ techniques are accordingly furthest promoted. Fig. 2 extracts some characteristic e-flux lines from the simulation results which will be expounded later. It verifies the above analyses and demonstrates that the impact of C_{trench} is fully restrained by the application of RFP.

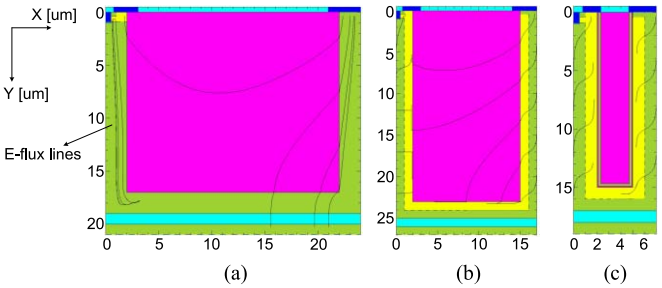

FIGURE 2. Characteristic e-flux lines in the off-state in (a) TLD, (b) TLD+QVSJ and (c) TLD+QVSJ+RFP, where the e-flux lines are extracted by simulation.

TABLE 1. Optimized parameters for 500-V T-LDMOS studied in this work.

Sym.	Meaning	Value
w_1	trench width for TLD	20 μm
w_2	trench width for TLD+QVSJ	13 μm
w_3	trench width for TLD+QVSJ+RFP	3 μm
d_1	trench depth for TLD	17 μm
d_2	trench depth for TLD+QVSJ	23 μm
d_3	trench depth for TLD+QVSJ+RFP	15 μm
t_0	n-d and p-d thickness	1 μm
t_1	BOX thickness	2 μm
N_{sub}	n-sub doping concentration	5.0×10^{14} cm^{-3}
$N_{dn\text{-}1}$	n-d doping concentration for TLD	2.8×10^{15} cm^{-3}
$N_{dn\text{-}2}$	n-d doping concentration for TLD+QVSJ	1.6×10^{16} cm^{-3}
$N_{dp\text{-}2}$	p-d doping concentration for TLD+QVSJ	1.4×10^{16} cm^{-3}
$N_{dn\text{-}3}$	n-d doping concentration for TLD+QVSJ+RFP	2.2×10^{16} cm^{-3}
$N_{dp\text{-}3}$	p-d doping concentration for TLD+QVSJ+RFP	2.1×10^{16} cm^{-3}

III. SIMULATION AND OPTIMIZATION

The devices are studied by 2D simulation in Medici and Sentaurus with four models of (ANALYTIC/CONMOB), FLDMOB, SRFMOB2, and IMPACT.I [25]–[28]. The trench dielectric is defined as BCB [27]–[28]. RFP is defined as SIPOS with the thickness of 200 nm. On top of that, some basic parameters, such as the BOX thickness (t_1), the substrate doping concentration (N_{sub}) and the thickness of n-d and p-d (t_0), are fixed as listed in Table 1. All the devices are optimized under the BV requirement of be larger than 500 V.

Fig. 3 shows the optimization for TLD. In this figure, the values of $N_{dn\text{-}1}$ and d_1 have been optimized in advance. They are selected for each w_1 from a substantial number of simulation results, under the requirement that BV is larger than 500 V and with the objective of getting $R_{ON,SP}$ as small as possible. From Fig. 3, it can be observed that the allowed $N_{dn\text{-}1}$ which satisfies the requirement of BV is increased with w_1. This is exactly due to that the impact of C_{trench} is restrained by the increase in w_1. However, it can also be observed that when w_1 is larger than 20 μm, although the allowed $N_{dn\text{-}1}$ continues to increase with w_1, $R_{ON,SP}$

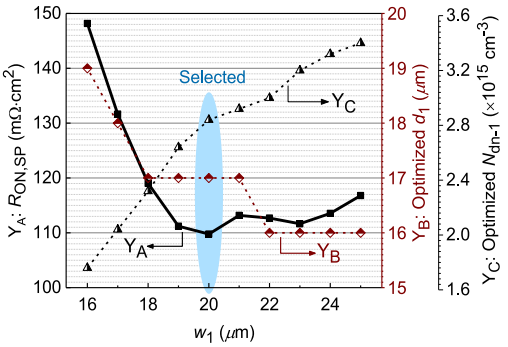

FIGURE 3. The parameters associated with the lowest $R_{ON,SP}$ are selected for TLD, where $N_{dn\text{-}1}$ and d_1 have been optimized for each w_1 to guarantee 500-V BV.

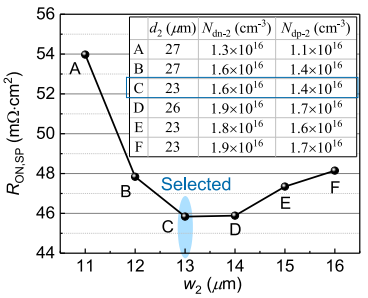

FIGURE 4. The parameters associated with the lowest $R_{ON,SP}$ are selected for TLD+QVSJ, where d_2, $N_{dn\text{-}2}$ and $N_{dp\text{-}2}$ have been optimized for each w_2 to guarantee BV larger than 500 V. The inset lists the specific values for them.

begins to increase as well. This is because the increased w_1 leads to an increase in chip area and total drift length, which produces influence on $R_{ON,SP}$ stronger than that produced by the increase in $N_{dn\text{-}1}$ at this time. According to the simulation results, the parameters associated with the lowest $R_{ON,SP}$ are selected for the following study. TLD with these parameters presents $R_{ON,SP}$ of about 110 mΩ·cm^2 and BV of about 502 V.

For TLD+QVSJ, a similar but more complex preliminary optimization is executed to select the values of the trench depth (d_2), doping concentration of p-d ($N_{dp\text{-}2}$) and $N_{dn\text{-}2}$ for each w_2. Then, the parameters associated with the lowest $R_{ON,SP}$ are selected as shown in Fig. 4. As the change trend of $R_{ON,SP}$ as a function of w_2 is similar to that has been revealed in Fig. 3, it is not repeated here. After the optimization, TLD+QVSJ presents $R_{ON,SP}$ of about 46 mΩ·cm^2 with BV of about 501 V.

As analyzed before, RFP enables TLD+QVSJ+RFP to own a uniform surface e-field distribution, so w_3 can be pretty small in theory. However, in terms of the practical fabrication, w_3 is retained to 3 μm and the trench depth (d_3) is set to 15 μm. Such a trench is able to be etched and filled with high quality [29]–[32]. When $N_{dn\text{-}3}$ is set to be 2.2×10^{16} cm^{-3}, BV can be larger than 500 V while the resistivity of RFP (ρ_{RFP}) is varying within a wide range. However, as shown in Fig. 5, With the decrease in ρ_{RFP},

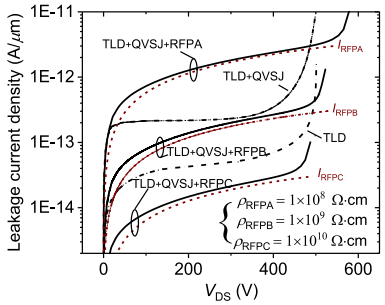

FIGURE 5. Reverse leakage current density vs. V_{DS} for TLD, TLD+QVSJ and TLD+QVSJ+RFP with different ρ_{RFP}. When ρ_{RFP} is set to be 1×10^{9} Ω·cm, the proposed TLD+QVSJ+RFP presents a satisfactory BV and a suitable reverse leakage current density which approximates that of TLD+QVSJ.

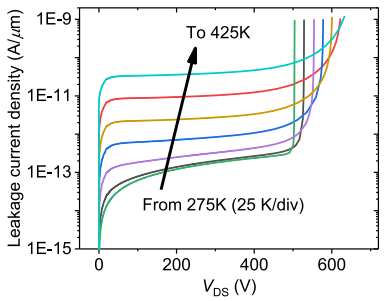

FIGURE 6. Reverse leakage current density vs. V_{DS} for TLD+QVSJ+RFP working at different temperatures. With the increase in temperature, the breakdown voltage and the reverse leakage current density are both increased.

the effect of RFP is enhanced and BV is increased, but I_{RFP} is increased as well. When ρ_{RFP} equals 1×10^{9} Ω·cm, the density of the leakage current through RFP (I_{RFP}) is about 10^{-13} A/μm, approximating to the leakage current density of TLD+QVSJ. Hence, in terms of a trade-off between BV and I_{RFP}, ρ_{RFP} is selected to be 1×10^{9} Ω·cm. Moreover, the contacts between RFP and the electrodes should be noticed [33]. There usually is a difference between the simulation and the realistic situation in the metallization effect [34]. If the practical metallization is not performed well, an immensely increased contact resistance will reduce I_{RFP} and impair the benefits brought by RFP. The above simulations are executed assuming that the devices are working at room temperature. If the working temperature changes, the device performance will be accordingly varied. As shown in Fig. 6, BV of TLD+QVSJ+RFP presents a positive temperature coefficient, which is similar to that of an ordinary MOSFET. This is due to the suppressed avalanche breakdown in high temperature and makes the device more stable. Finally, the proposed TLD+QVSJ+RFP with the parameters listed in Table 1 obtains $R_{ON,SP}$ of only 9.36 mΩ·cm^2 with BV of 528.5 V. This BV is larger than the target, so a better $R_{ON,SP}$ can be expected by increasing $N_{dn\text{-}3}$. However, a higher $N_{dn\text{-}3}$ enhances the field strength between n-d and p-d, which impairs the ability of the device to resist various process errors. As a trade-off between performance and reliability, the parameters not associated with the best performance are

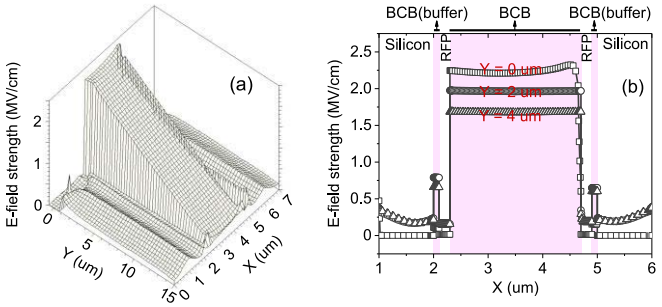

FIGURE 7. Critical e-field distribution in the trench of TLD+QVSJ+RFP. (a) 3D distribution. The trench is located in (x: 2~5) and (y: 0~15). (b) 1D distribution along some lateral tangents. The maximum e-field in BCB, whether inside RFP or in the buffer layer between RFP and silicon, is about 2.3 MV/cm.

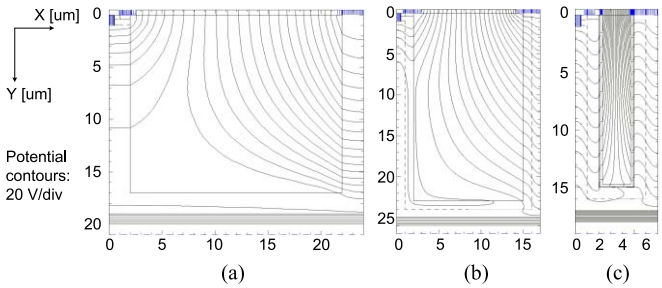

FIGURE 8. Comparison of potential distribution in the case of critical breakdown. (a) For TLD which maintains the enough BV through increasing the trench width and meanwhile decreasing the doping concentration of the drift region. (b) For TLD+QVSJ. Although a quasi SJ technique is applied to enhance the doping concentration of the drift region, the charge-imbalance due to the effect of trench capacitor seriously damages the potential distribution and limits the benefit from SJ; (c) For TLD+QVSJ+RFP. A uniform potential distribution is obtained in the QVSJ region attributed to the protection of RFP.

selected for the following study. Fig. 7 shows the critical e-field distribution in the trench of the proposed device. The e-field strength sustained by the trench dielectric, including the BCB inside RFP and the BCB acting as the buffer layer between RFP and silicon, does not exceed 2.3 MV/cm. This is smaller than the allowed 5.3 MV/cm [28], [35].

IV. COMPARISON OF PERFORMANCE

Fig. 8 compares the potential distribution when the devices are all in the case of critical breakdown. For TLD, w_1 is very large while $N_{dn\text{-}1}$ is very small, but its potential distribution is not uniform as shown in Fig. 8(a). This is exactly attributed to the impact of C_{trench}. In the right n-d, C_{trench} extracts some e-flux emitted by the ionized donors and improves the potential distribution there. However, on the left, C_{trench} sends some e-flux to p-w via n-d and worsens the potential distribution there. For TLD+QVSJ, the application of QVSJ decreases w_2 to be 13 μm and increases $N_{dn\text{-}2}$ as large as 1.6×10^{16} cm^{-3}. However, because of the impact of C_{trench}, the QVSJ structure on the left of the trench is obviously charge-imbalanced, as shown in Fig. 8(b). For the proposed TLD+QVSJ+RFP, RFP eliminates the impact of C_{trench}.

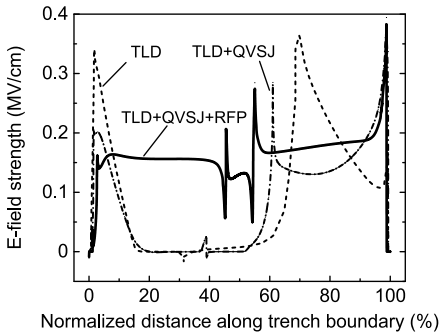

FIGURE 9. Comparison of electric field distributions along the trench boundary in the case of critical breakdown. The trench boundary starts from the point v_1 as marked in Fig. 1(a) and then extends along the path of $v_1 \rightarrow v_2 \rightarrow v_3 \rightarrow v_4$, and finally ends at the point v_4. For a clear comparison, the abscissa is normalized as the distance away from v_1 divided by the total length of v_1-v_2-v_3-v_4. Due to the application of RFP, the QVSJ region in the proposed device satisfies the charge-balanced condition and obtains a uniform e-field distribution.

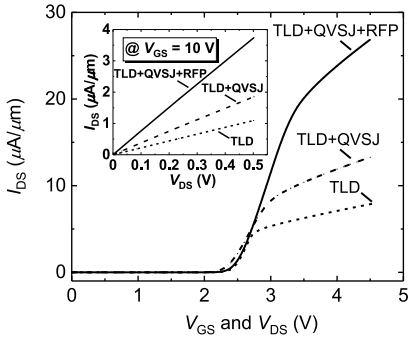

FIGURE 10. Comparison of forward *I-V* characteristics. The three devices present the same threshold voltages which approximate 2.3 V. In the comparison, the proposed device exhibits a smaller on-resistance than the others. The inset details the output *I-V* curves when the devices are working at V_{GS} = 10V.

A uniform potential distribution is therefore obtained when w_3 is only 3 μm and $N_{dn\text{-}3}$ is as large as 2.2×10^{16} cm^{-3}, as shown in Fig. 8(c). Fig. 9 further verifies the advantage of the proposal by comparing the surface e-field distribution. In order to provide a clear view, the abscissa is normalized as the distance away from v_1 divided by the total drift region length. It is obvious that due to the combined application of QVSJ and RFP, the proposed device gains more uniform surface e-field distribution on both sides of the trench.

Fig. 10 compares the forward performance. When G and D are both connected to an increased voltage ($V_{GS} = V_{DS}$), the current flowing from D to S (I_{DS}) is accordingly increased. It is observed that the threshold voltages for the three devices all approximate to 2.3 V but the proposed one has the current increasing more rapidly. The inset shows the output *I-V* curves when V_{GS} is biased at 10 V. At the V_{DS} of 0.5 V, I_{DS} for the TLD, TLD+QVSJ and TLD+QVSJ+RFP are about 1.09, 1.85 and 3.73 μA/μm, respectively. Combined with the device width listed in Table 1, their $R_{ON,SP}$ are calculated to be about 110, 46 and 9.36 mΩ·cm^2, respectively. In comparison with TLD+QVSJ, the proposed TLD+QVSJ+RFP

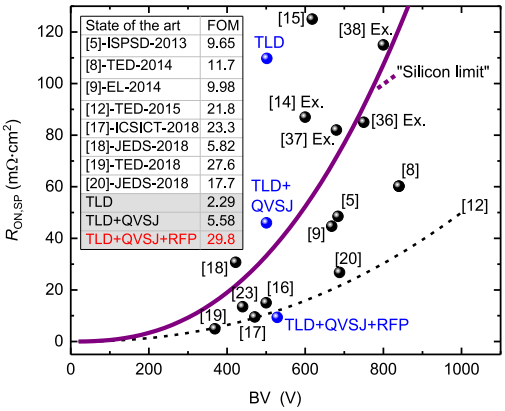

FIGURE 11. Comparison of the BV ~ $R_{ON,SP}$ relationship between this work and the prior art of LDMOS which consists of some simulated and experimental (Ex.) results reported recently. Due to the combined application of QVSJ and RFP in T-LDMOS, the proposed device obtains a more improved relationship than the prior art. The inset lists the FOM (all with the unit of MW/cm^2) for some state-of-the-art T-LDMOS and for this work.

has the $R_{ON,SP}$ reduced by about 79% under the same BV requirement.

Fig. 11 compares the BV ~ $R_{ON,SP}$ relationship between this work and the prior art of LDMOS, which includes some experimental results [14], [36]–[38]. Although the conventional TLD+QVSJ studied in this work adopts the SJ technique, its performance is worse than the silicon limit, which reveals the impact of C_{trench}. As the proposed device gets the help of RFP, its performance not only breaks the silicon limit but also be superior to the other techniques. To quantify the BV~$R_{ON,SP}$ relationship, a classic figure of merit (FOM) is introduced, which equals $BV^2/R_{ON,SP}$ [4]–[20]. The inset lists the FOM of some T-LDMOS reported recently. Because the impact of C_{trench} is eliminated by RFP and the advantage of SJ is fully developed, the proposed device obtains the FOM up to 29.8 MW/cm^2, which is better than the state-of-the-art.

To study the dynamic performance, the three devices are tested by a typical circuit as shown in Fig. 12(a), where the device area, the inductance current and the duty cycle are set to be 5 mm^2, 2 A, and 50%, respectively. Fig. 12(b) presents the turn-on process, where G is triggered by a 1-ns rising edge at the time of 0 ns. Fig. 12(c) presents the turn-off process, where G is triggered by a 1-ns falling edge at the time of 0 ns. Because TLD+QVSJ+RFP contains more cells under the same area and has a more heavily doped drift region, its gate is harder to drive while more charge need be stored and released during the switching process. Therefore, TLD+QVSJ+RFP presents a longer switching time and dissipates more energy. From this point of view, the proposal seems to be not efficient, but energy-wasteful instead. However, actually the total average-power (P_{total}) consumed by the device consists of four parts, i.e., that from the turn-on and turn-off process, that from the off-state (P_{off}) and that from the on-state (P_{on}). P_{off} is usually ignored because the reverse

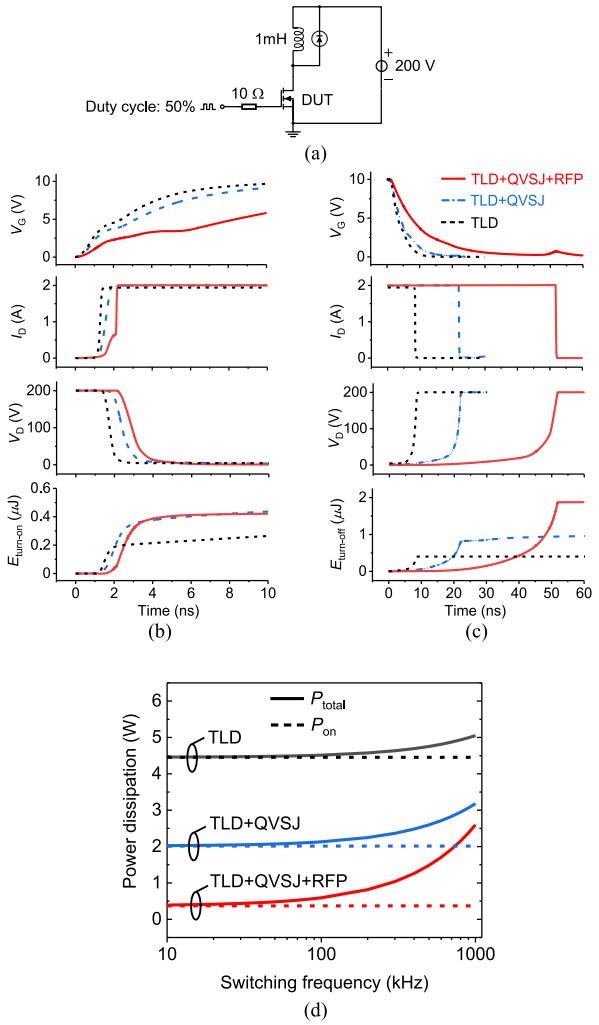

FIGURE 12. **Comparison of the dynamic performance. (a) The circuit used for simulation, where DUT are the devices under test. (b) When G is triggered by a 1-ns rising edge at the time of 0 ns, the devices enter into the turn-on process. (c) When G is triggered by a 1-ns falling edge at the time of 0 ns, the devices enter into the turn-off process. (d) Comparison of the average-power dissipated by the devices working at various frequencies. Since P_{on} of the proposed TLD+QVSJ+RFP is significantly reduced, a considerable reduction of P_{total} can be observed at the frequency range of 10∼200 kHz.**

leakage current is quite small. P_{on} for TLD, TLD+QVSJ and TLD+QVSJ+RFP operating in this circuit are 4.45, 2.01 and 0.37 W, respectively, as shown in Fig. 12(d). The wide gap of P_{on} stems from the aforementioned distinction of FOM and, as a result, TLD+QVSJ+RFP exhibits a much smaller P_{total} than the others, especially at the frequency of 10∼200 kHz which is usually adopted in a switching mode power supply (SMPS) [1].

V. DISCUSSION ON FABRICATION

A brief process flow is designed for the proposal. It starts from an SOI substrate as shown in Fig. 13(a). Then, as shown in Fig. 13(b) and Fig. 13(c), the silicon is etched and an QVSJ structure is formed probably by the traditional thermal diffusion or the angle ion-implantation [39].

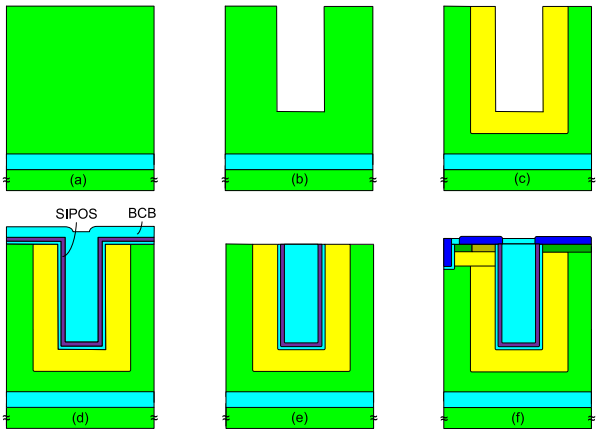

FIGURE 13. **Brief process flow for the fabrication of the proposed device. (a) An SOI substrate prepared for the manufacture. (b) Trench etching. (c) Formation of an QVSJ structure. (d) Deposition of a buffer layer, an RFP layer and the trench dielectric in sequence. (e) CMP process. (f) CMOS-compatible process to form the p-w, trench gate, source and drain active regions.**

After that, a thin buffer layer of BCB, an RFP layer of SIPOS, and the trench dielectric of BCB are deposited in sequence as shown in Fig. 13(d). Finally, a process of Chemical Mechanical Polishing (CMP) is executed to obtain a smooth surface as shown in Fig. 13(e) and some common CMOS-compatible processes are performed to realize the p-w, trench gate, source and drain active regions, contacts, metal and so on, as shown in Fig. 13(f). The above process flow can also be used to fabricate TLD+QVSJ as long as RFP is not deposited in Fig. 13(d). In the fabrication process of TLD+QVSJ+RFP, the RFP layer coats wafer without distinction and is pruned by CMP without masks, so the realization of it barely complicates the process compared with that for TLD+QVSJ.

During the fabrication, there are at least two process errors should be attached great importance to. First is that happening in the formation of QVSJ. If the amounts of the impurities in n-d and p-d deviate from the preliminary design, QVSJ will fall into the status of charge-imbalance. Fig. 14 shows the influence of the deviation of N_{dn} and N_{dp} on BV. When the deviation range is ±2%, BV is decreased by about 18.7% for TLD+QVSJ, and only by about 1.5% for TLD+QVSJ+RFP. The latter has an excellent ability to resist the impact of charge-imbalance, which also benefits from the effect of RFP. Second is the process error possibly appearing at the deposition of RFP. Except the influence of the variation of ρ_{RFP} and the contact of RFP which have been discussed before, the variation of the thickness of RFP (t_{RFP}) would impact BV as well. If RFP is uniform, it is not difficult to speculate that a larger t_{RFP} would benefit the surface e-field distribution and result in an increased BV as well as an increased I_{RFP}. If RFP is not uniform, the difference between the t_{RFP} at the trench bottom and that on the trench sidewall will vary the potential distribution on RFP. Fig. 15 compares the potential distribution of the proposed device with different RFP step-coverages, where

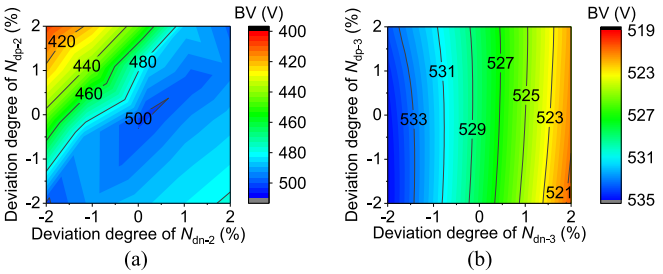

FIGURE 14. **When the doping concentration of the QVSJ structure is deviated from the preliminary design, the influence of charge imbalance on BV. (a) For TLD+QVSJ, if N_{dn-2} and N_{dp-2} are both varied in a range of ±2%, the minimum BV is about 407 V. (b) For the proposed TLD+QVSJ+RFP, if N_{dn-3} and N_{dp-3} are both varied in the range of ±2%, its BV maintains to be larger than 520 V.**

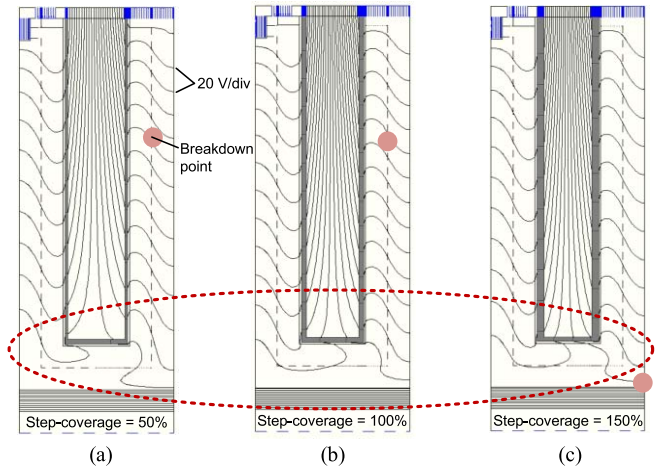

FIGURE 15. **Influence of the RFP step-coverage on the potential distribution in the case of critical breakdown. (a) When the RFP step-coverage is 50%, namely the RFP thickness at the trench bottom is 200 nm while that on the trench sidewall is 100 nm, BV is about 479 V. (b) When the step-coverage is 100%, the highest BV of about 528 V is obtained. (c) When the step-coverage is 150%, BV is about 486 V. With the increase in the step-coverage, the RFP on the trench sidewall becomes thicker and more reverse voltage will be sustained by the RFP at the trench bottom, which changes the surface e-field distribution as well as the location of the breakdown point.**

the step-coverage is defined as the ratio of the sidewall thickness to the bottom thickness [40]. With the increase in step-coverage, RFP at the bottom sustains more voltage than that on the sidewall, and the potential distribution becomes not uniform which impacts BV and changes the breakdown point. According to the simulation results, even when the step-coverage varies in a wide range of ± 50%, BV of the proposed device is still larger than 479 V, which should be acceptable in a practical fabrication.

VI. CONCLUSION

In this paper, the T-LDMOS is improved by the QVSJ and RFP techniques. Due to the effect of RFP, the device width and the doping of QVSJ are both greatly optimized, which contributes to an excellent device performance verified by simulation. Moreover, the fabrication of the proposed device is discussed. Compared with the conventional QVSJ T-LDMOS, the addition of RFP barely increases the process complexity. This work is therefore believed to be appealing to the field of power electronics.

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