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Test System for Thin Film Transistor Parameter Extraction in Active Matrix Backplanes

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ABSTRACT Thin film transistor (TFT) active matrix backplanes are used in large area electronic systems, such as displays and image sensors. With backplanes being fabricated on wearable and flexible substrates, the possibilities of operational faults in backplanes have increased. These faults could either be hard faults, such as line opens or shorts or could be softer faults, such as time dependent variations in the TFT transfer characteristics. Real time diagnosis of these faults require built-in-self-test systems. While many such systems have been demonstrated to diagnose hard faults, an easily realizable system to identify soft faults, such as variations in transistor transconductance remain an open challenge. In this paper, we discuss a system that extracts the transconductance by charging and then discharging the pixel capacitor at various gate voltages for an active matrix liquid crystal display backplane. This permits a plot of the time averaged current versus the gate voltage from which the spatial variation of transconductance can be extracted. The details of the design are discussed and a proof of concept with a 3×4 amorphous silicon backplane is demonstrated.

INDEX TERMS Thin film transistor, large area electronics, faults, testing, built-in-self-test

I. INTRODUCTION

The recent years have seen a surge in the use of flexible and wearable electronics for applications such as healthcare, energy harvesting, displays and image sensors [1]–[2]. These systems either use thin film transistor (TFT) based integrated circuits or hybrid systems having TFT circuits along with packaged integrated circuits [3]–[4]. A key advantage of TFT based integrated circuits is the ability to achieve circuits over large areas. Many systems such as displays and image sensors rely on this advantage and use an active matrix backplane array [5].

Active matrix arrays are composed of several rows and columns of pixels with each pixel accessed by a pixel select TFT that acts as a switch as shown in Fig. 1. The pixel select TFT is controlled via orthogonally routed 'data lines' and 'gate lines' that are connected to the drain and gate terminals of the TFT, respectively. Depending on whether it is a sensor array (e.g., image sensors) or a display, the pixel select TFT is used to read data from or write data into the pixel, respectively [6]–[7]. Fig. 1 shows the typical architecture of an active matrix liquid crystal display backplane. During operation, the gate lines are sequentially addressed turning on (closing) the pixel select TFTs of the corresponding row. Data is written onto the storage capacitors of the pixels in the row being addressed via the data lines. Once data is written, pixel select TFTs for the row are opened and the subsequent row is addressed. This operation continues and periodically cycles through the rows at a certain refresh rate [8], [9].

Active matrix systems are prone to fabrication and operation related faults in interconnects and TFTs [10]–[11]. Interconnect faults such as opens and shorts cause pixels to become inaccessible. More subtle faults are related to variation in TFT parameters such as mobility (μ), contact resistance, insulator capacitance per unit area (C_i), channel width (W), channel lenght (L), and threshold voltage (V_T) that is also affected by bias dependent charge trapping. These parameters influence the TFT transconductance via the parameter $\beta = \mu\gamma^{2-\alpha}C_i^{\alpha-1}(W/L)$. Here the parameter $\alpha = 2T_c/T$ depends on the disorder in the semiconductor resulting in states in the band gap having a characteristic

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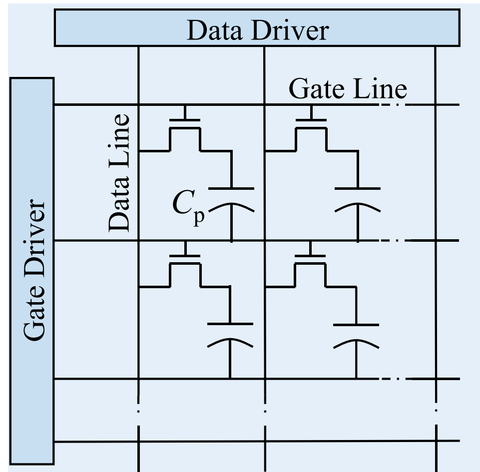

FIGURE 1. Architecture of active matrix backplane for liquid crystal displays.

temperature T_c and with T being the ambient temperature. In the absence of defects $\alpha = 2$. The parameter γ has the dimensions of charge per unit area. Variations in β and the leakage current affects the on and off resistance of the switch.

Backplane calibration and testing is an important aspect of any active matrix system [12]–[13]. Several schemes have been designed for backplane testing. Commonly used non-contact schemes are voltage imaging [14], [15], [16], optical charge sensing [17] and electron beam testing [18]. The common contact based techniques are charge feedthrough readout [19], transfer admittance technique [20] and the modified built in driver technique [11]. While the above discussed techniques for backplane testing have their unique advantages, they are mostly applied to identify hard faults such as opens and shorts and cannot directly be used to extract softer faults such as TFT parameter variation.

In this work, we discuss the development of a test system and test algorithm that not only identifies interconnect related faults but also characterizes the pixel select TFT for an active matrix liquid crystal display backplane. The test algorithm, procedure to extract TFT parameters and the key challenges in parameter extraction are discussed. Using a 3×4 amorphous hydrogenated silicon (a-Si:H) TFT based backplane, parameters extracted by the test system are compared with those extracted using a Keithely 4200 Semiconductor Parameter Analyzer with good corroboration. The methodology and system architecture demonstrates a proof of concept for the possibility of a built-in-self-test (BIST) that can be integrated with backplane drivers for real time diagnostics.

II. THE TEST SYSTEM

A. TEST ALGORITHM

The testing scheme aims to write data onto the storage capacitor of the TFT-capacitor pixel circuit and subsequently read the average current through the TFT during capacitor discharge with the TFT gated at a specific gate voltage. Ultimately, the test system records a sequence of n time averaged currents through the TFT, $(\tilde{I}_1, \tilde{I}_2 ... \tilde{I}_j ... \tilde{I}_n)$, corresponding to an increasing sequence of n applied gate voltages $(V_{g1}, V_{g2} ... V_{gj} ... V_{gn})$ (Fig. 2). The TFT parameters are extracted from this plot of $\tilde{I}_j$ versus V_{gj}. It must be noted that although this plot is an indicator of the transfer characteristics it is not identical to the transfer characteristics. This is because the current being read out for a given gate voltage is not the current at a constant drain-source voltage but is the average current for the time varying drain-source voltage (due to the capacitor discharging).

B. OPERATION

Testing based on the above approach is achieved using a test unit that is integrated with the backplane driver as shown in Fig. 2. The unit has five main circuit blocks - the Write circuit, the Gate Drive circuit, the Read circuit, the Controller and the Power Supply Unit. The Power Supply Unit is not necessary for battery driven systems integrated on wearable or flexible substrates. Both the Write and Read circuits are connected to the data lines of the backplane via a switch and can be disconnected from the data lines when required. To accomplish the above discussed test algorithm the test system uses a sequence of Write, Hold and Read operations performed (Fig. 2(a)) by the Write circuit and Read circuit with co-ordination from the Gate Drive circuit.

During the Write operation, the Read circuit is kept disconnected from the array. The row being addressed is provided a constant gate voltage to turn on the pixel select TFTs of the row. The pixel select TFTs of the other rows remain open. A constant known data voltage, V_d, is written onto the storage capacitors of the selected row. During Write, it is ensured that the gate voltage is large enough to keep the pixel select TFTs in linear mode operation. It is to be noted that during the Write operation, the data line and any parasitic capacitances on the data line are also charged to V_d.

The Hold operation is a brief event that follows the Write operation and is used to separate the Write and Read operations. During the Hold event, the Write circuit is disconnected from the data line. The Read circuit also continues to remain disconnected while the gate voltage for the row being addressed is held at the value used for the Write operation. Therefore during Hold, the pixel is electrically isolated from the Read and Write circuit while the storage capacitor retains the voltage V_d (excepting for leakage into the other pixels).

After the first Write-Hold operations, the first Read operation is performed by setting the gate of the pixel select switch to a voltage V_{g1}, the first voltage in the sequence of gate voltages described in the test algorithm. The charge on the pixel capacitor is then read out by the Read circuit using a charge amplifier. The Read operation lasts for a time interval T_r and the charge measured is used to obtain the average current, $\tilde{I}_1$ through the TFT. The read out time, T_r, should be large enough to ensure large signal to noise ratio (SNR) while at the same time not so large as to saturate the

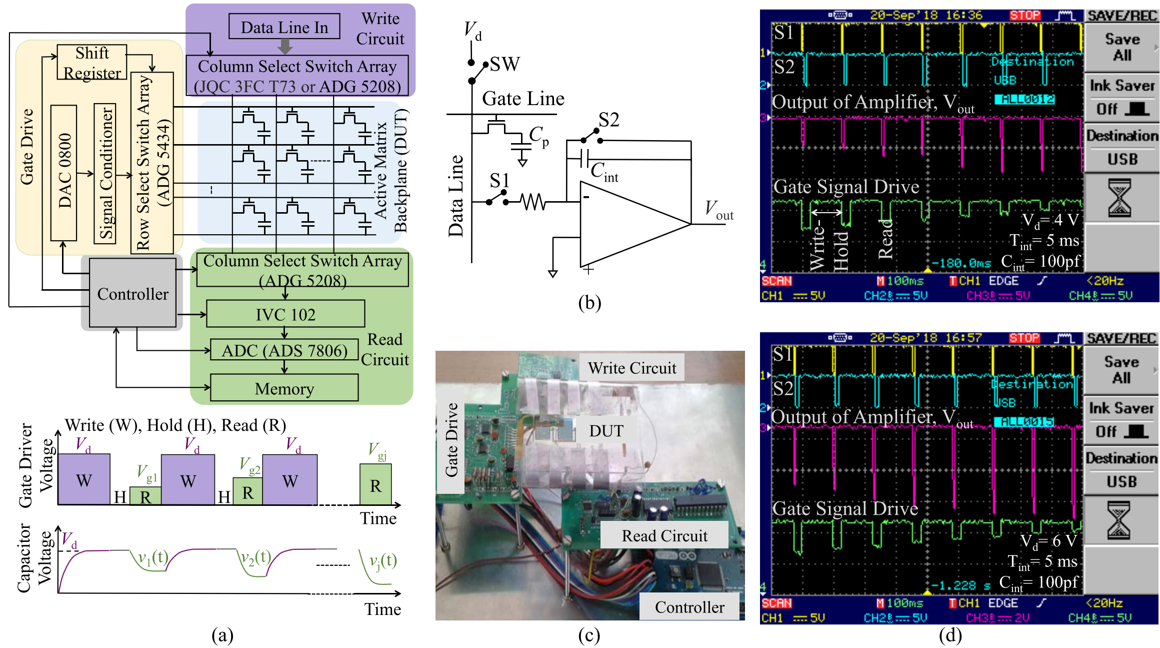

FIGURE 2. Design and operation of the test system.

read out amplifier or completely drain the pixel capacitor. After the first Read operation, the second Write-Hold operations are performed during which the pixel capacitor is once again charged to V_d. Subsequent to the second Write-Hold operations, the second Read operation happens by setting the gate voltage at V_{g2} during which the average current $\tilde{I}_2$ is recorded. This sequence of Write-Hold-Read operations continue till the final Read operation is performed with the gate of the pixel select TFT set at V_{gn} (the largest gate voltage in the sequence) and the corresponding average current of $\tilde{I}_n$ is read. This sequence of operations is illustrated in Fig. 2(a). The parameters of the TFT are then extracted from the corresponding time averaged current versus gate voltage characteristics, i.e., the $\tilde{I}_j$ versus V_{gj} characteristics.

C. DESIGN AND HARDWARE

The details of the hardware comprising the test unit is shown in Fig. 2a. The Write circuit consists of a line having voltage V_d and a switch bar comprised of the ADG5208 switches. The ADG5208 has a low on resistance of typically 160 Ω and a low leakage current of typically 5 pA at maximum drain-source voltage.

The Gate drive circuit controls the gate voltages of the TFT during testing. The gate signals are communicated to the selected row via an ADG5434 switch array. Each ADG5434 package contains a quad SPDT high voltage switch with a low on resistance of typically 16 Ω. The input to the switch was provided by the DAC0800 8-bit bi-directional digital to analog converter (DAC). The DAC supplies the gate voltage for the Write operation as well as the sequence of gate voltages ($V_{g1}, V_{g2} \cdots V_{gj} \cdots V_{gn}$) for the Read operation. The addressing of the switch array was done with a shift register that permitted the gate voltage to be supplied to the different rows of the active matrix backplane in sequence. The ability of the DAC0800 to drive bipolar signals (range ±18 V) allows for the possibility of testing backplanes having n or p channel pixel select TFTs.

The Read circuit was also connected to the data lines of the array via the ADG5208 switch matrix. The key component of the Read circuit is the IVC102 precision switched transimpedance amplifier. The amplifier measures input currents in the range of $\pm 100\mu$A thereby making them ideal for measuring TFT current. The architecture of the amplifier is shown in Fig. 2b. During the Read operation, the current through the pixel select TFT from the discharing pixel storage capacitor is used to charge the feedback capacitor of the IVC 102. The charge amplifier is controlled by two low leakage PMOS switches S1 and S2. Closing S1 permitted the integration of the charge on the feedback capacitor of capacitance, C_{int} (maximum 100 pF). The charge injection due to the closing of S1 was about 1 pC and was much smaller than the signal charge. The switch S2 was open during integration and readout and was closed to reset the integration capacitor once readout was complete. To obtain an accurate readout, the output of charge amplifier was recorded twice, the first just before closing S1 and the second at the end of the Read operation, i.e., after time T_r has elapsed since closing S1. The voltage output of the amplifier was the difference between these two values. The output of the IVC102 was submited to a 12 bit bipolar analog to digital converter, ADS7806, and subsequently stored in memory.

Fig. 2c shows the system used for experiments. Fig. 2d shows oscilloscope waveform captures highlighting the

readout event as well as the typical readout during the read sequence ($V_{g1}, V_{g2} \cdots V_{gj} \cdots V_{gn}$) for two different V_d (4 V and 6 V).

III. PARAMETER EXTRACTION

A. AVERAGED CURRENT MEASURED AFTER READOUT

During the jth Write-Hold operation, the pixel storage capacitor of capacitance C_p, is charged to V_d. During Read, the gate of the pixel select TFT is set to V_{gj}. The drain voltage of the TFT is defined by the voltage of the pixel storage capacitor and the source voltage of the TFT is set at the pseudo ground of the charge amplifier. The pixel capacitor therefore begins to discharge through the TFT. We define the time instance $t = 0$ at the beginning of the Read operation. We also let $i_j(t)$ and $v_j(t)$ define the instantaneous current through the TFT and voltage on the pixel capacitor at time t, respectively with $i_j(t) = -C_p(dv_j/dt)$. Since the charge being readout is equal to charge lost by the storage capacitor during the discharge, the time averaged current can be defined as

$$\tilde{I}_j = \frac{C_p\left(V_d - v_j(t = T_r)\right)}{T_r} = \frac{\int_0^{T_r} i_j \mathrm{d}t}{T_r} \tag{1}$$

Ideally, the voltage output of the charge amplifier is $-(1/C_{int}) \int_0^{T_r} i_j(t)\mathrm{d}t = -\tilde{I}_j T_r / C_{int}$. The value of $\tilde{I}_j$ can therefore be obtained by measuring the output of the charge amplifier. However, the charge integrated on the charge amplifier is not only due to i_j but also includes the leakage current, i_{leak}, as well. This leakage is a combination of leakage currents through the switch matrix of the Write circuit as well as leakage from the pixel being read to the other pixels along the same data line. This leakage current appears as an offset in output voltage of the charge amplifier as $-(1/C_{int}) \int_0^{T_r} (i_j(t) + i_{leak})\mathrm{d}t$. Therefore, the value of $\tilde{I}_j$ extracted from the measurement of charge amplfier output will contain this offset which needs to be ignored.

B. $\tilde{I}_J$ VERSUS V_{GJ} PLOT

To relate $\tilde{I}_j$ to V_{gj}, Eq. (1) needs to be solved. Depending on whether it is biased in saturation or linear mode during readout, the current through the pixel select TFT using a disordered semiconductor is defined as,

$$i_j = \begin{cases} (\beta/\alpha)\left(V_{gj} - V_T\right)^\alpha & \text{sat} \\ (\beta/\alpha)\left(\left(V_{gj} - V_T\right)^\alpha - \left(V_{gj} - V_T - v_j\right)^\alpha\right) & \text{lin} \end{cases} \tag{2}$$

As defined earlier, V_T is the threshold voltage, $\beta = \mu\gamma^{2-\alpha} C_i^{\alpha-1}(W/L)$ with μ the mobility, γ the charge density per unit area, C_i the insulator capacitance per unit area, W the channel width and L the channel length. The parameter $\alpha = 2T_c/T$ where T_c is the characteristic temperature of the tail states of the disordered semiconductor and T the ambient temperature. In most modern diordered semiconductors, $T_c \approx 300$ K (in a-Si:H, $T_c \approx 325$ K) and for all practical purposes, $\alpha \approx 2$. For this special case, we define $\beta = \mu C_i(W/L)$. Moreover, V_T in most disordered semiconductor based TFTs is bias dependent and time varying. This time dependence typically has a time constant of a few hours. Therefore, here we assume that V_T is a constant and does not vary significantly during the Read operation. Based on this, the current voltage characteristics of the TFT is approximated to a square law in above threshold operation. Depending on whether the TFT is biased in saturation ($0 < V_{gj} - V_T \leq v_j$) or linear ($V_{gj} - V_T > v_j$) region, the TFT current, $i_j(t)$ is given by,

$$i_j = \begin{cases} (\beta/2)\left(V_{gj} - V_T\right)^2 & \text{sat} \\ (\beta/2)\left(2\left(V_{gj} - V_T\right) - v_j\right)v_j & \text{lin} \end{cases} \tag{3}$$

If $V_{gj} \leq V_T$, the TFT would operate is subthreshold mode. However, the subthreshold region is not used for extracting β and is therefore not discussed.

Substituting Eq. (3) in Eq. (1), $\tilde{I}_j$ can be calculated for a given V_{gj}. However, depending on the value of T_r, there arises another case to be considered. If the V_{gj} is such that the TFT is biased in linear operation, it will continue to remain so during the read out operation. However, if the TFT is biased in saturation mode ($V_{gj} - V_T \leq V_d$), it is important to note if T_r is large enough to permit the TFT to enter linear bias. The time taken for the capacitor to discharge sufficiently for the TFT to move from saturation to linear bias is $T_{0j} = ((V_d - (V_{gj} - V_T))C_p)/((\beta/2)(V_{gj} - V_T)^2)$. If $T_r > T_{0j}$, the TFT biased in saturation at $t = 0$ will eventually move into linear operation. On the other hand, if $T_r \leq T_{0j}$, the TFT will continue to remain in saturation bias throughout the read out operation. It can be shown that,

$$\tilde{I}_j \sim \begin{cases} \frac{\beta}{2}\left(V_{gj} - V_T\right)^2 & \text{sat}, T_r \leq T_{0j} \\ \frac{C_p V_d}{T_r}\left(1 - \frac{2(V_{gj}-V_T)e^{\frac{-(T_r - T_{0j})}{\tau_j}}}{V_d\left(1 + e^{\frac{-(T_r - T_{0j})}{\tau_j}}\right)}\right) & \text{sat}, T_r > T_{0j} \\ \frac{C_p V_d}{T_r}\left(\frac{(2(V_{gj}-V_T)-V_d)\left(1-e^{\frac{-T_r}{\tau_j}}\right)}{2(V_{gj}-V_T)-V_d\left(1-e^{\frac{-T_r}{\tau_j}}\right)}\right) & \text{lin} \end{cases} \tag{4}$$

where $\tau_j = C_p/(\beta(V_{gj} - V_T))$. The plot of $\tilde{I}_j$ versus V_{gj} can now be obtained from Eq. (4).

C. EXTRACTION OF PARAMETER β

The parameter β is estimated by estimating τ_j from Eq. (4). Since β is expected to be constant during the readout, all values of τ_j (i.e., corresponding to all values of V_{gj}) must yield the same β. If β is to be extracted using saturation mode operation, there always remains the ambiquity of as to whether $T_r \leq T_{0j}$ or not. Therefore, it is preferable to extract β when the TFT is in linear mode operation, i.e., using those regions of the $\tilde{I}_j$ versus V_{gj} plot where V_{gj} is the highest (i.e., when $j = n$ and nearby). From the linear

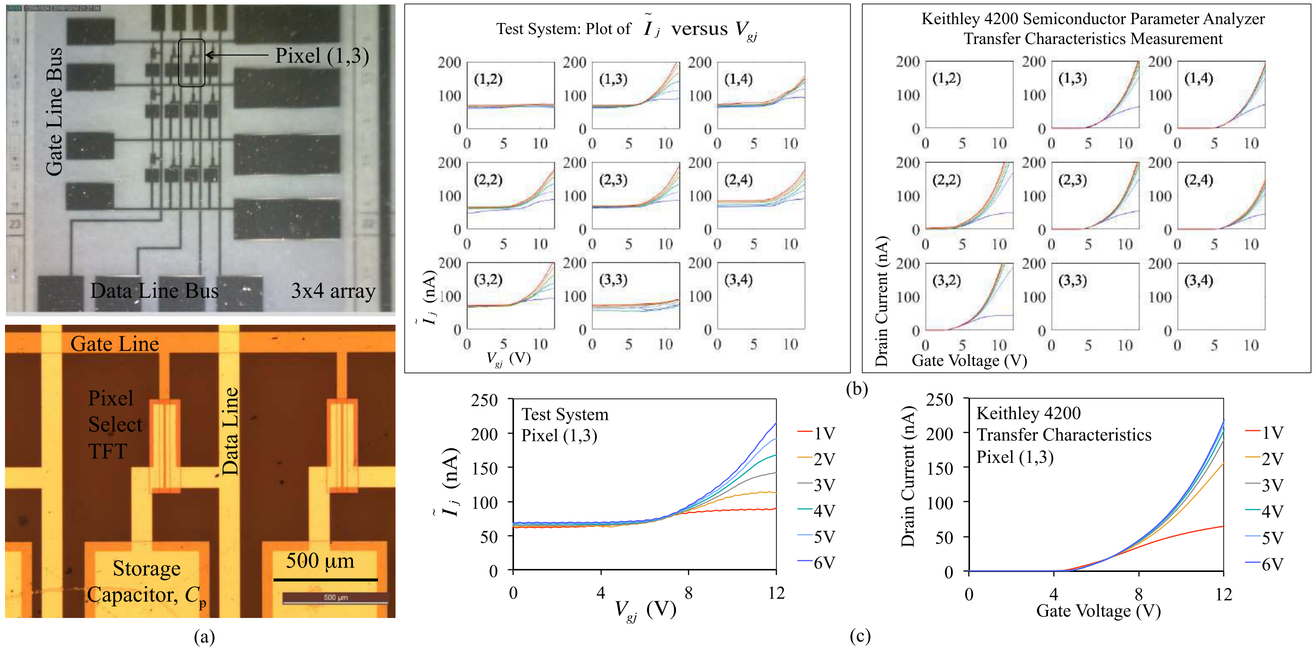

FIGURE 3. (a) a-Si:H TFT 3x4 active matrix backplane. Defects are purposefully introduced. Column 1 is defective and the pixels cannot be accessed thereby rendering the backplane to be effectively 3x3. Pixels (1,2)and (3,3) in the array were made defective by shorting the plates of the pixel capacitor. Pixel (3,4) was given a defective pixel TFT. (b) Test of the backplane using the test system showing the plot of $\tilde{I}_j$ versus V_{gj} for all pixels. Also shown alongside is the transfer characteristics of all TFTs of the corresponding pixels as measured (individual TFTs were probed) using a Keithley 4200 Semiconductor Parameter Analyzer. (c) Comparison of the $\tilde{I}_j$ versus V_{gj} plot for pixel (1,3) as measured by the test system compared to the transfer characteristics of the TFT in pixel (1,3) as measured with the Keithley 4200 Semiconductor Parameter Analyzer.

region of operation as described in Eq. (4), β is found to be,

$$\beta = \frac{C_p}{T_r(V_{gj} - V_T)} \ln\left(\frac{1 + \frac{\tilde{I}_j T_r}{C_p(2(V_{gj}-V_T)-V_d)}}{1 - \frac{\tilde{I}_j T_r}{C_p V_d}} \right). \quad (5)$$

IV. EXPERIMENTS

A. BACKPLANE FABRICATION

For experiments, an a-Si:H TFT based active matrix backplane with 3x4 pixels was fabricated and is shown in Fig. 3a. The TFT deposition involved an e-beam deposition of Cr gate metal followed by a PECVD deposition of a 200 nm silicon nitride insulator layer and 100 nm amorphous hydrogenated silicon layer. The source drain contacts were created using n-doped amorphous silicon followed by a 100nm Cr/200nm Al metal deposited by e-beam. The pixel circuit was designed with a pixel select TFT in series with a pixel storage capacitor as showin in Fig. 1a. The pixel select TFT was designed with $L = 10\ \mu$m, $W = 400\ \mu$m and 20 μm gate-source/drain overlap. The pixel storage capacitor was 500 μm by 500 μm and had a capacitance of $C_p \approx 70$ pF.

Defects were purposely introduced into the backplane. Each row of the array had minor differences in the length of the interconnect forming the gate of the pixel select TFT. The first column of the array was made defective rendering the backplane to effectively have 3 × 3 accessible pixels. Pixels (1,2) and (3,3) in the array were made defective by shorting the plates of the pixel capacitor. Pixel (3,4) was given a defective pixel TFT. This backplane was then tested with the test system.

B. BACKPLANE TESTING

During test, the backplane was connected to the test system using probes and triaxial connectors. This connection added constant but a significant amount of parasitic capacitance of about 140 pF in parallel with the pixel storage capacitance. Thus, the effective capacitance being charged to V_d was about 210 pF. Considering this, the integration time during read was set at 5 ms with the integration capacitor being 100 pF.

The backplane was tested with several values of V_d ranging from 1 V to 6 V. The plot of $\tilde{I}_j$ versus V_{gj} was measured by sweeping V_{gj} from 0 V to 12 V. This plot as extracted for the array is shown in Fig. 3b. Since no data was extracted from the defective column 1 of the 3x4 array, only a 3x3 subset of the array was accessible. The defective pixels (i.e., (1,2), (3,3) and (3,4)) do not show the expected characteristics.

The transfer characteristics of the TFTs of the backplane were also measured using a Keithley 4200 Semiconductor Parameter Analyzer as shown in Fig. 3b. Here three points must be noted. First, the measurement with the parameter analyzer was not an automated backplane test like the test system with a Write-Hold-Read sequence. Instead the TFTs of each pixel were probed and measured separately. This avoided leakage from the back plane and external circuits as

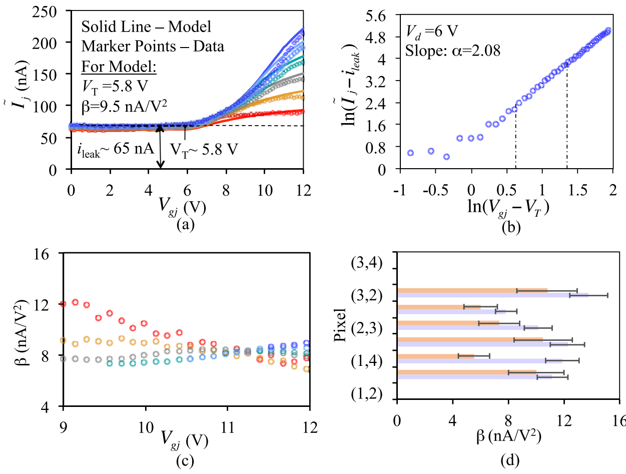

FIGURE 4. Extraction of the parameter β. (a) Plot of $\tilde{I}_j$ versus V_{gj} of pixel (1,3) measured by the test system (marker points) plotted along with the model of Eq. (4) using the extracted values of $V_T = 5.8$ V and $\beta = 9.5$ nA/V^2. (b) Extraction of α from the saturation region using $V_d = 6$ V. A value of $\alpha \approx 2.08$ was observed. (c) Extraction of β from the linear region using Eq. (5) for different V_d. The average value of $\beta = 9.5$ nA/V^2 is used for the model in Fig. 4(a). (d) The spatial map of extracted parameter β as extracted by the test system (red bars) compared with values extracted using the transfer characteristics of the TFTs measured by the Keithley 4200 Semiconductor Parameter Analyzer (blue bars).

was experienced by the test system. Second, the measurement was that of the instantaneous current at a fixed drain voltage. The measurement was therefore the true transfer characteristics and not $\tilde{I}_j$ versus V_{gj}. The transfer characteristics of the individual TFTs were made by sweeping the gate voltage from 0 V to 12 V with the drain-source voltage varied from 1 V to 6 V. Third, the characteristics of defective pixel (3,4) is not shown since the TFT is faulty. The TFTs in the defective pixels (1,2) and (3,3) however could be characterized by the Keithley as the defect was with regards to the shorted pixel capacitors. Fig. 3c compares the $\tilde{I}_j$ versus V_{gj} characteristics of pixel (1,3) obtained by the test system with the transfer characteristics of the pixel select TFT of the same pixel as measured by the Keithely. As mentioned earlier, the plots are not expected to look alike since the measurements are of different parameters, i.e., the test system measures the time averaged current at a varying drain voltage with leakage currents from several sources while the Keithely 4200 measures the instantaneous current at a constant drain voltage with no external sources for leakage currents (i.e., the true transfer characteristics).

C. EXTRACTION OF β FROM EXPERIMENT

We use the $\tilde{I}_j$ versus V_{gj} plot of pixel (1,3) shown in Fig. 3c to describe the procedure for extracting β. The plot is redrawn as Fig. 4a and the following observations are made. First, it is observed that $(1/T_r)\int_0^{T_r} i_{leak}\mathrm{d}t \approx 65$ nA. Second, it is seen that the current saturates at large values of V_{gj}. This is a natural consequence of averaging the current. As seen in Eq. (4), as $V_{gj} - V_T$ gets larger the plot of $\tilde{I}_j$ versus V_{gj} saturates and corroborates with experimental observation. The threshold voltage, V_T, can be estimated in the conventional manner by looking at the V_{gj} intercept of the $\tilde{I}_j - i_{leak}$ versus V_{gj} plot. This is so since V_T represents the V_{gj} when the current just becomes $\geq i_{leak}$. This definition can be quantified by considering Eq. (4). In context of this discussion, Eq. (4) assumes $i_{leak} = 0$ and therefore effectively represents the $\tilde{I}_j - i_{leak}$ versus V_{gj} plot. If $V_{gj} - V_T = 0$ in linear mode or saturation mode operation in Eq. (4), $\tilde{I}_j = 0$ and represents the onset of conduction. Hence, from the V_{gj} intercept of the $\tilde{I}_j - i_{leak}$ versus V_{gj} plot, $V_T \approx 5.8$ V. Based on the above analysis, β is extracted from experimental data using Eq. (5). Fig. 4b shows the parameters α extracted from the saturation mode transfer characteristics. Here the data for the highest value of V_d is used to ensure that the TFT has the best chance to be in saturation. It was seen that $\alpha \approx 2.08$ thereby justifying the use of Eq. (5). Fig. 4c plots the plots the extracted value of β for different V_d. The average value of $\beta = 9.48$ nA/V^2. Using these extracted parameters, the models (solid lines) based on Eq. (4) are compared with the measured data (marker points) in Fig. 4a. Fig. 4d compares the parameter β for all pixels of the array as extracted by this procedure using the test system (red bars) to those extracted by the measurement of transfer characteristics from the Keithley 4200 (blue bars). The values of extracted β are a reasonably good match and the map of the spatial variation in β is reasonably accurate (with the exception of pixel (1,4)). If the parameter α is significantly > 2, more computation and post processing would be needed to estimate β.

V. DISCUSSION

This work discussed the design and operation of a TFT backplane calibration system that allowed the measurement of the TFT characteristics. The system can therefore not only detect hard faults such as interconnect opens or faulty TFTs, but also detect soft faults such as TFT transconductance variations across the backplane.

The system operation differs from a conventional TFT transfer characteristics measurement since the system measures the time averaged TFT current with a time varying drain-source voltage. This methodology adds a little computational complexity for the extraction of TFT transconductance but offers the advantage of using simple off the shelf components permitting a straightforward intergration with the layout and operation of a conventional backplane. If developed, this approach has the potential of providing a real time built-in-self-testing of backplanes in applications that may not permit frequent access to the system (e.g., wearable electronics). A map of the soft faults as produced by the system can also be used as a feedback for process flow modifications during TFT growth and backplane fabrication.

A major problem in the system is parasitic capacitance. Since the system operates by charging the pixel capacitor and then subsequently discharging it through the pixel select TFT, the drain-source voltage dynamics plays an important role in the extraction of TFT transconductance. Since this dynamics depends on the effective line and other parasitic

capacitances lying in parallel with the pixel capacitor, compensating for the parasitics is important. If this parasitic capacitance is constant (as seen in this work), the compensation is easily achieved. However, if the parasitic capacitance is time variant, the parameter extraction technique will show errors. Other hidden parameters such as the contact resistance cannot be extracted by the test system measurements as shown in Fig. 4 alone. Therefore any impact of contact resistance is subsumed in the current voltage characteristics and would reflect as a poor value for β. However, this is true for the Keithley as well. In order to extract the contact resistance, it is necessary to make more measurements – be it with the test system or the Keithley – for example characteristics extracted from TFTs with different channel lengths. Another challenge that arises in parameter extraction is that due to bias dependent defect creation. Disordered semiconductor based TFTs are known to experience a bias dependent threshold voltage shift with time. If the shift is slow and is practically zero during the measurement, it poses no problems. However, if the shift is very rapid and the threshold voltage changes significantly during measurement, there will be an error in the parameter extracted. Once again, in most modern semiconductors, the threshold voltage shift is gradual due to either better materials or better driving techniques (e.g., bias flipping).

In general, the system is intended to provide a relative map of the parameters of the TFT from one pixel to the other and provide a reasonably good measure of these parameters. It does this task well. This paper presents this simple and yet useful system that serves as a valuable tool in TFT backplane development.

VI. CONCLUSION

The paper discussed the development of a backplane test system that aided the extraction of the TFT parameters, particularly β, for the pixel select TFT. The test algorithm was discussed, the test system developed and tested on an amorphous hydrogenated silicon TFT backplane for a proof of concept. The performance of the test system was compared with TFT parameters extracted with a Keithley 4200. In conclusion, the test system can be expected to provide a reasonably accurate spatial map of the parameters of the pixel select TFT in all pixels. If only a relative comparison of parameters is sought, the test system proves to be quite reliable. Such a map is expected to be of value in backplane calibration and testing and also serve as a tool to provide feedback to the TFT process flow and also as a tool for reliability studies.

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