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Atomistic Study of Lateral Charge Diffusion Degradation During Program/Erase Cycling in 3-D NAND Flash Memory

JIXUAN WU [1,2], JIEZHI CHEN [1] (Senior Member, IEEE), AND XIANGWEI JIANG [2] (Member, IEEE)

1 Institute of School of Information Science and Engineering, Shandong University, Jinan 266237, China
2 Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China

CORRESPONDING AUTHORS: J. CHEN AND X. JIANG (e-mail: chen.jiezhi@sdu.edu.cn; xwjiang@semi.ac.cn)

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ABSTRACT Impacts of lateral charge diffusion on the retention characteristics of charge-trapping (CT) 3-D NAND flash memory are comprehensively studied in this paper. Atomistic study through ab initio calculation is carried out to understand the correlations between P/E stress induced shallow trap generations and pre-existing traps in Si_3N_4. It is shown that more shallow traps will be generated with a combination of electron/hole injections and free hydrogen (H) during P/E cycling. Our results strongly suggest that process optimizations to control free H in Si_3N_4 CT layer could be a key point for robust retention characteristics.

INDEX TERMS Silicon nitride, 3D NAND, charge trapping, lateral charge diffusion, shallow trap.

I. INTRODUCTION

The digital world generating oceans of data which must be stored, managed, and protected, cause an urgent need of ultra-high storage capacity. It is known that the scaling of planar NAND flash memory is facing many challenges from physical limitations, such as the cell-to-cell interference, edge fringing field effect, patterning, the physical dimension of the inter-poly dielectric (IPD), and the channel coupling [1]–[6]. 3D NAND flash memory has become the mainstream of non-volatile memory with its ultra-high storage density and low bit-cost [7]–[9]. The first Triple Level Cell (TLC) 3D BiCS flash memory used 32 layers was demonstrated in 2015 [10], and then it reached 64 layers in 2017 [11], [12]. It is fabricated by depositing multi-stacked gate and dielectric layers, punching thorough whole stacks, and then forming oxide-nitride-oxide stacks and channel in the holes. Compared with planer (2D) NAND flash, 3D NAND has a physically larger cell size, but a smaller effective area due to the stacking of multiple layers. Although charge-trapping (CT) 3D NAND flash memory with Si_3N_4 CT layer shows a lot of merits in comparison to its 2D planar counterpart, 3D NAND flash memory has some special reliability problems. Especially, it has a shared CT layer and lateral charge diffusion between neighbor cells will result in worse data retention [13]–[15]. Considering the cell size scaling and the higher program voltage in the development of future 3D NAND, the lateral charge loss will be much more critical.

It has been proposed in previous experimental studies that the fast charge loss within a few seconds is mainly related to the shallow trapped electrons, and the lateral charge loss is also obvious through the comparison between checked board pattern and solid pattern [14], [16]. There is research shows that lateral migration accounts for a larger percentage of charge loss as the channel length reduces, indicating that the lateral migration is a critical issue in high-density and high-reliability design of 3D CT memories [17]. Furthermore, in 2D NAND, P/E stress induced tunneling layer degradation is the most important reason for worse date retention (DR) after cycling. While in 3D NAND, it is still unclear whether the P/E stress will cause additional DR degradation during P/E cycling.

In our previous experimental study on TLC 3D NAND flash memory, we analyzed the transient error bits from retention after program [18]. Considering that the error bits from threshold voltage (Vth) negative-shift (G to F, F to E,

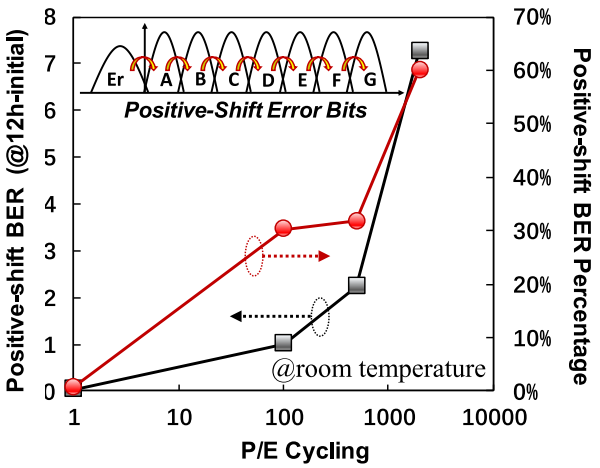

FIGURE 1. The error bits from Vth positive-shift in TLC 3D NAND Flash [18]. After 12hours retention at room temperature, Vth positive shift (charge accrual) turns to be the dominant mechanism of error bits in data retention after P/E cycling.

E to D) could be caused by both vertical charge loss and the lateral charge loss, we focused on the error bits from Vth positive-shift (Er to A, A to B, B to C, C to D) that are mainly caused by lateral charge accrual from neighbor space and cells [19]–[20]. It is well known that high level cells tend to lost more and more electrons in long-term retention and cells' V_{th} will have negative shifts. However, things are different for short-term retention in 3D NAND flash memory. As shown in Fig. 1, with focus on the transient error bits in 12 hours' retention at room temperature, it is observed that V_{th} positive-shift caused error bits turn to be the dominant part (60.1%) of total transient error bits in retention after 2000 P/E cycling. In other words, in short-term retention, although high level cells lost electrons and have negative shifts, middle-low level cells will have positive shifts and cause more error bits [18]. This was explained by the degradation of lateral charge diffusion from shallow traps generation under repeated P/E stress. In our previous study on the relationship of shallow traps and the lateral charge diffusion [21], it was found that the oxygen (O) in Si_3N_4 nearby the SiO_2/Si_3N_4 interface could form shallow traps and cause lateral charge diffusion. It has also been reported in [22]–[24] that the O-related defects could cause the collapse of a Si_3N_4 layer. However, up to nowadays, the impacts of P/E stress on lateral charge diffusion has not been well studied. In this work, the atomistic study of lateral charge diffusion is comprehensively investigated with the main focus on the correlations between pre-existing traps and P/E stress induced shallow trap generations.

II. CALCULATION APPROACH

In this work, atomistic defects in Si_3N_4 CT layer are calculated by DFT with plane wave pseudopotential as implemented in the GPU accelerated PWmat package [25]. A 280-atom rectangular super-cell is built-up to simulate the bulk β-Si_3N_4. The lattice length of A, B, C is 12.9879, 14.9971, and 14.3566 Å respectively. Generalized-gradient approximation (GGA)-PBE exchange correlation functional is used in the geometry optimization with a residual force of 0.01eV/Å as the convergence criteria. And the Hybrid functional HSE is used for self-consistent calculations with the Fock parameter of $\alpha = 0.1$ to achieve the correct band gap of 5.3eV [26]. The energy cut-off is set at 50 Ry.

The formation energy of a defect α in the charge state q are described by the following formula [27]:

$$\Delta H_f(\alpha, q) = \Delta E(\alpha, q) + \sum n_i \mu_i + qE_F + q\Delta V \quad (1)$$

where $\Delta E(\alpha, q) = E(\alpha, q) - E(host) + \Sigma n_i E(i) + q\varepsilon_{VBM}(host)$, with n_i the number of atoms of type i removed from the supercell, μ_i the chemical potential of constituent i referenced to elemental solid/gas with energy $E(i)$, q the number of electrons transferred from the supercell to the reservoirs in the formation of the defect, $E(\alpha, q)$ the total energy of system with a defect α in the charge state q, $E(host)$ the total energy of the system without defect (host), E_F the Fermi level with reference to the valence band maximum of the host ($\varepsilon_{VBM}(host)$). The chemical potential of the atom i, μ_i, dependson the experimental conditions. Under the Si-rich condition, to avoid precipitation of the Si elements, the chemical potential is limited by $\mu_{Si}^{max} = \mu(\text{Si bulk}) = 0$. In addition, μ_{Si} and μ_N are limited to the value of maintaining Si_3N_4. For impurity atoms like H atom and O atom, their chemical potentials are limited by the formation of SiH_4 and SiO_2. The electrostatic potential correction ΔV is included to align the potential of the defects' super-cell with the host [28]. Considering the large supercell and the dispute on the overcorrection, the image charge correction is not included in this work [29].

III. RESULTS AND DISCUSSION

As aforementioned, P/E stress impacts on shallow traps generation is a critical concern in 3D NAND reliabilities. P/E stress can break the hydrogen bonding at the interface and in the bulk Si_3N_4, as we clarified in [21].

As shown in Fig. 2, at the program state, the gate voltage is positive and electrons (e^-) are injected into the silicon nitride layer from the substrate (Si-sub). For the erase state, a negative voltage is applied to the Gate and holes (h^+) are injected into the silicon nitride layer from the Si-sub. Quantities of H atoms are introduced during the process of Si_3N_4 deposition and the H passivation in the annealing process [30]. The free H can trap the e^- or h^+ forming the H^- or H^+ and diffuse under the extra electric field effect. Both neutral and charged H are considered in the work. The movement of free H finally causes the H with different charged states to aggregate at the interface of the blocking layer or the tunneling layer, affecting the defects at the interface. These free H will affect pre-existing defects and possibly form new defects. In addition, charge injection will also influence the final detects' structure and make things more complex, as shown in Fig. 3. The final structure of defects combined the free H could be different with the electron/hole injection.

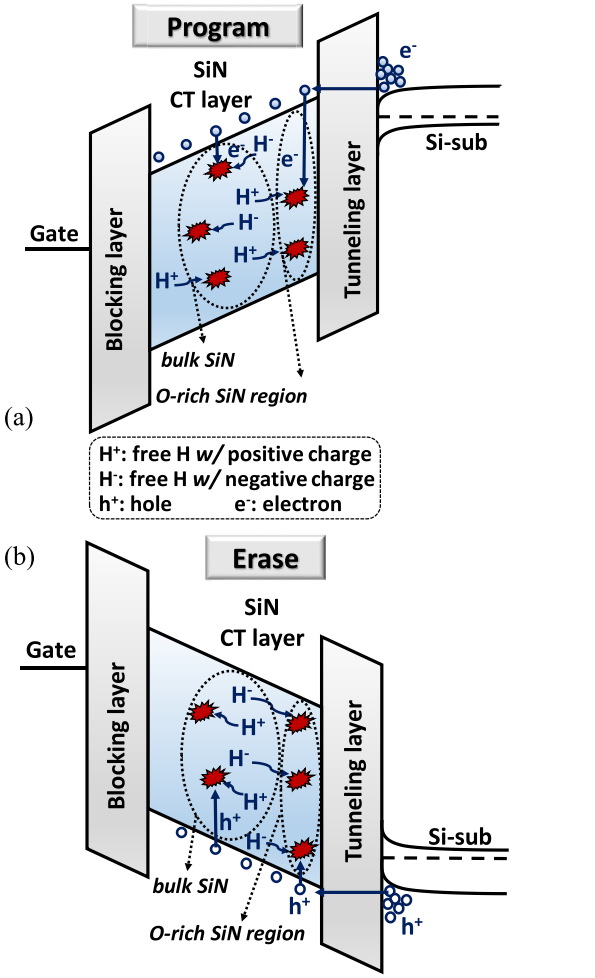

FIGURE 2. The free H with a positive charge or negative charge will drift to different directions under (a) program operation with a large amount of electrons' injection and (b) erase operation with a large amount of holes' injection.

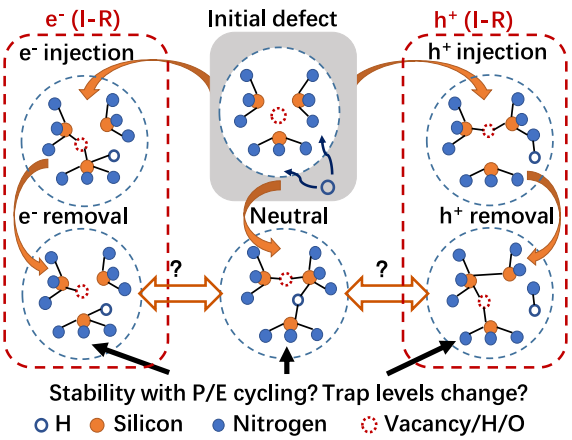

FIGURE 3. The final structure of defects combined the free H could be different with the electron/hole injection and removal cycles (e^-/h^+ I-R). Stability and conversion between them are discussed.

For further understandings of H release during P/E cycling, we studied their effects on the pre-existing defects with charge injection. Stability and conversion between them are

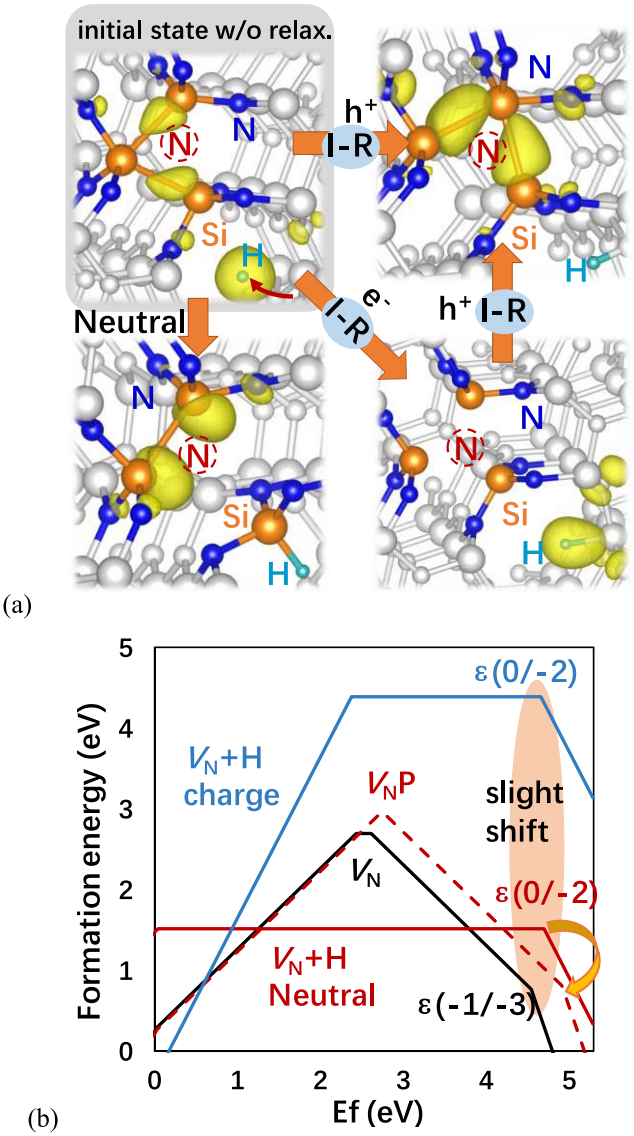

FIGURE 4. (a) H atom drags the nearby Si atom and forms a puckered structure at a neutral state. (b) Formation energies of V_N, V_N+H, and V_NP defect. Slight shift on the electron trap level between V_N and V_N+H, while the V_NP defect performs as a shallow trap level.

discussed. Considering our previous calculation results [21] that the nitrogen vacancy (V_N) defect has the lowest formation energy, the H substitute N (H_N) defect has the similar trap level with the experimental results, and the O atom cause shallow traps, we focus on the defects of V_N, H_N, and O incorporation in this work. All of the following atom structures are relaxed at the neutral state or after the electron/hole (e^-/h^+) injection-removal cycle (I-R), as shown in Fig. 3.

In the case of V_N defect, from Fig. 4(a) on can found that the free H will drag the nearby Si atom and form a puckered structure at the neutral state. However, for the charged state, the puckered structure could not be formed. The atom structures' transfer and those trap levels' wave function are shown in Fig. 4(a). From the wave function, we can see the

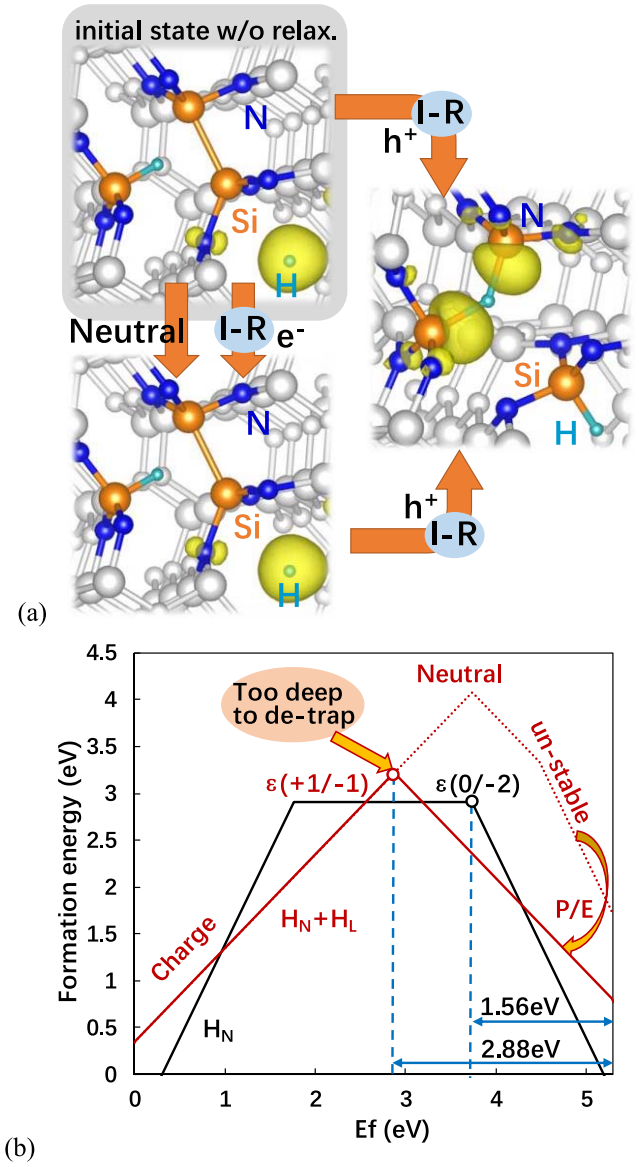

FIGURE 5. The free H getting close to H_N through the 12-ring (H_N+H_L): (a) atom structure, (b) formation energy. The stable final defects have a much deeper electron trap level than H_N. The density of effective electron trap center decrease and the device storage capacities degrade.

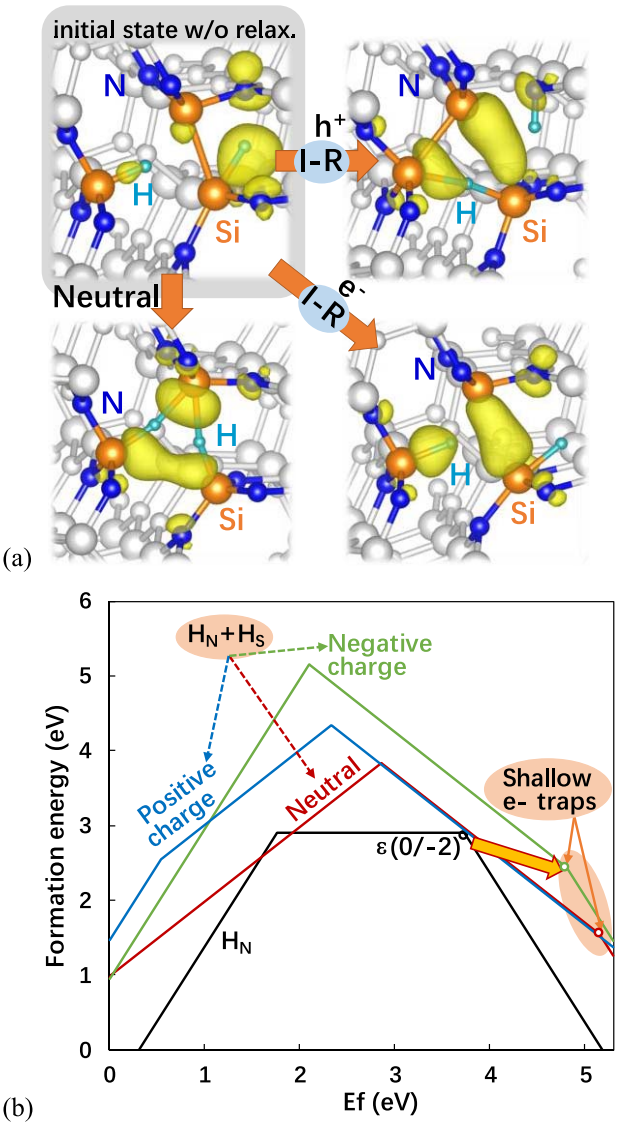

FIGURE 6. The free H getting close to H_N through the 8-ring (H_N+H_S): (a) atom structure, (b) formation energy. Generated defects show shallow electron trap levels.

electron density located nearby the free H turns to locate nearby the silicon atom. From the formation energy shown in Fig. 4(b), we get that there is only a slight shift on the electron trap levels. So these fresh V_N+H defects have no significant influence on the charge trapping. However, since the Si-H bonding energy is so small that the Si-H bond broken will form the puckered V_N (V_NP) which performs as a shallow trap level as shown in Fig. 4(b). As a result, the free H atom's combination and release cause an unstable and switching trap behaviors.

However, for H passivated V_N (H_N), charge trap levels are obviously changed with another H combination. Here, two different approaching paths are considered when the free H getting close to H_N defect: through the 12 atoms-ring (H_N+H_L) and through the 8 atoms-ring (H_N+H_S). For the H_N+H_L condition shown in Fig. 5(a), the relaxed structure at the neutral state and negative charged state is unstable and will be changed to the stable structure (left figure) with hole injection. The relaxed structure at positive state is still stable after the charge injection and removal cycling. From their formation energies shown in Fig. 5(a), one can found that the final stable defect has a trap level of 2.88 eV reference to CBM. It has much deeper electron trap levels than H_N which has a trap level of 1.56 eV. The electrons trapped by very deep trap levels are difficult to de-trap. That is to say, the very deep trap level has no contribution to the Vth shift. So, because of the free H combination and P/E cycling, the effective charge trap density is decreased.

For the H_N+H_S condition, from the initial state at neutral, positive charged, and negative charged, the structure will be

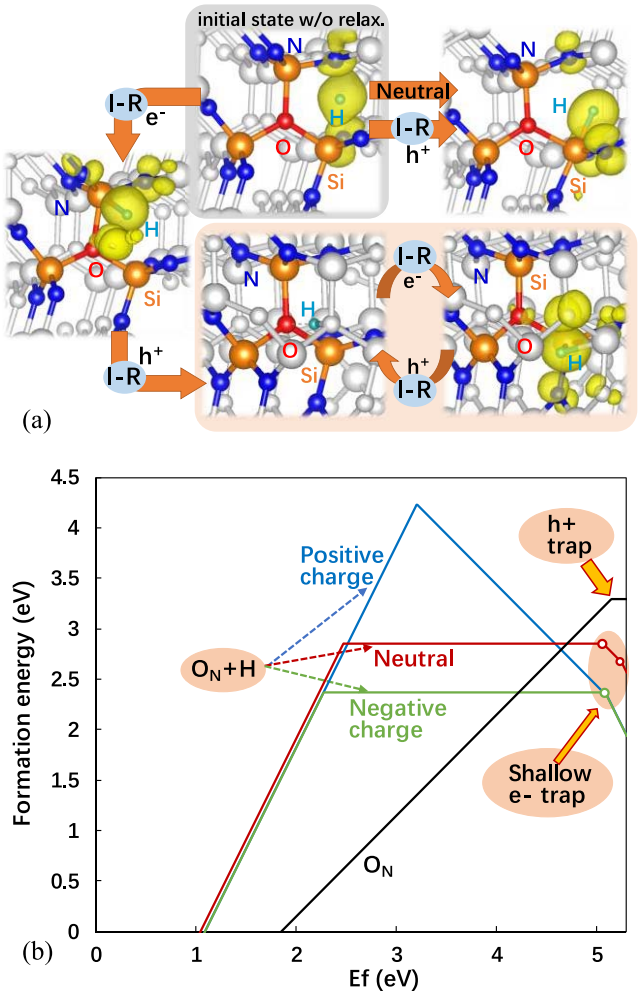

FIGURE 7. **(a) Atom structures: the free H atom combines the O_N defect forming three different defects at different initial charge state. (b) Formation energy: the pre-existing O_N defect can only trap holes. With the free H combination, O_N+H shows shallow electron trap levels.**

TABLE 1. **Summaries of P/E cycling stress-induced defects' and trap levels' transition in Si_3N_4 CT layer.**

Defect type	Initial	P/E cycling
V_N+Hi	2.45 $(+1/0)_h$ 2.67 $(0/-1)_e$ 0.74 $(-1/-3)_e$	Q0: 0.58 $(0/-2)_e$ Q+: 2.39 $(+2/0)_h$ 0.62 $(0/-2)_e$
H_N+H_S	1.77 $(+2/0)_h$ 1.56 $(-2/0)_e$	Q0: 2.44 $(+1/-1)_h$ 0.14 $(-1/-2)_e$ Q+: 0.54 $(+2/+1)_h$ 2.96 $(+1/-1)_e$ Q-: 3.20 $(+2/-1)_h$ 0.48 $(-1/-2)_e$
H_N+H_L	1.77 $(+2/0)_h$ 1.56 $(-2/0)_e$	2.88 $(+1/-1)_e$
O_N+Hi	5.15 $(+2/0)_h$	Q0: 2.47 $(+2/0)_h$ 0.23 $(0/-1)_e$ 0.05$(-1/-2)_e$ Q+: 2.09 $(+1/-1)_e$ 0.19 $(-1/-2)_e$ Q-: 2.28 $(+2/0)_h$ 0.23 $(0/-1)_e$ 0.19 $(-1/-2)_e$
V_N-Oi+Hi	5.10 $(0/-1)_e$ 0.18 $(-1/-2)_e$	2.93 $(+1/-1)_e$ 1.09 $(-1/-2)_e$

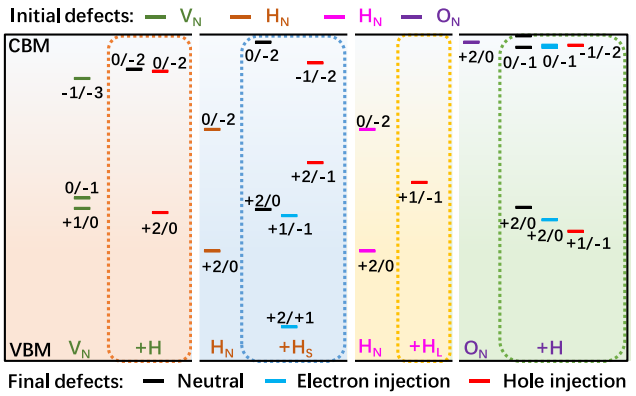

FIGURE 8. **The initial trap levels before the free H combination and the stable trap levels after the free H combination. It shows more shallow traps after the free H combination.**

stabilized at three different final structures respectively, as shown in Fig. 6(a). Each final structure is stable during P/E cycling. From their formation energies shows in Fig. 6(b), it is found that shallow electron traps are generated, which means that trapped electrons in those defects can be easily de-trapped to the conduction band and then cause the lateral charge diffusion.

As for O incorporated defect that exists nearby the SiO_x/Si_3N_4 interface, it is known that the interstitial O atom (V_N+O_i defect) performs as the shallow electron trap center and O atom substituted N atom (O_N defect) performs as the hole trap center [21]. In this work, the free H combination together with electron/hole injection is investigated. For the V_N+O_i defect induced shallow traps, they will be changed to deep traps with the free H combination and this will be stable even with charge injection. However, for the O_N defect, we can find that the free H gets closer to O_N defect and forms different defects at different initial charge states (Fig. 7(a)). For the neutral and positive charged initial states, the relaxed structures of free H combination are stable (right top). For the negative charged initial state, the relaxed structure is not stable and will be changed when electron injection. O_N defect will be changed from the hole trap to the electron trap with the free H combination (O_N+H), as shown in Fig. 7(b). The important thing is, the O_N+H defect will also generate shallow electron traps and will contribute to lateral charge diffusions. So, for the free H atom's combination of O_N defect, it will transfer from the hole trap center to both hole and electron trap center. However, the electron trapped by O_N+H defect is very easy to de-trap which will cause larger lateral charge diffusion.

Above calculation results are summarized in Fig. 8 and Table 1. From Fig. 8, the trap levels in the gap are described. It shows that, in most cases, when the free H and charge injection are combined with pre-existing defects, shallow traps could be generated and will result in worse retention via lateral charge diffusion. Especially for the O_N defect which performs a hole trap center, there show extremely electron trap levels after the free H atom combination. That means the H aggregation at the bottom or top interface of the Si_3N_4 layer will cause the more shallow traps and degrade the data retention performance.

IV. CONCLUSION

The correlations between program/erase stress induced shallow trap generations and pre-existing traps in Si_3N_4 of 3D NAND flash memory are systematically studied in this work. Based on our calculations, it shows that with injected electrons/holes under program/erase operation, the free H will assist shallow traps generation and result in more serious charge diffusion. Our results are important to the process optimizations aiming at high endurance 3D NAND flash memories with robust reliabilities.

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