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Tunnel Field-Effect Transistor With Segmented Channel

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ABSTRACT A tunnel field-effect transistor with segmented channels (Seg-TFET) on a corrugated substrate is proposed. The Seg-TFET takes advantage of using three stripes and the selective contact configuration to define the direction of current, and thereby its device performance can be improved. Furthermore, the process flow of the Seg-TFET demonstrates a substantiation of the new device structure. Consequently, its current flow is simply defined by adjusting the appropriate contact configuration at metal-zero-level without any additional front-end-of-line process.

INDEX TERMS Tunnel FET, tunneling, corrugated substrate.

I. INTRODUCTION

Tunnel field effect transistor (TFET) is a promising device for low power applications such as Internet of things (IoT) [1]–[6]. Because of non-scaled thermal voltage, the subthreshold swing (SS) of conventional metal oxide semiconductor field effect transistor (MOSFET) does not reach to sub-60-mV/decade at room temperature. However, as the operational principle of TFET is involved with the band-to-band tunneling (BTBT) process at the interface between source and channel, the TFET can overcome the physical limit of SS, i.e., SS can be lower than 60-mV/decade at 300 K. In spite of the feature of sub-60-mV/decade SS for low power applications, a conventional TFET (i.e., p-i-n TFET) is characterized by several problems such as low device performance (e.g., insufficient on-state drive current and average SS) and unidirectional current flow (intrinsically caused by its asymmetric device structure). Although several previous studies have been proposed to improve device performance by exploiting small band-gap materials in the source region of p-i-n TFET [4]–[10] and/or to alleviate unidirectional current issue by symmetrical device structure, which has bidirectional current flow [11]–[12], there still exists room to improve the device performances of TFET (e.g., I_{ON}/I_{OFF} ratio and SS).

In this study, a TFET with segmented channels (Seg-TFET) is proposed and investigated using technology computer aided design (TCAD) simulation tool. A process flow scheme for the Seg-TFET is provided in Section II. To improve the device performance, a low bandgap semiconductor (e.g., germanium) is used in the stripes of the Seg-TFET. In particular, we provide a new method of defining source and drain regions, to determine the source-to-drain current flow in TFET.

II. DEVICE DESIGN AND FABRICATION

Figure 1(a) shows a bird's eye-view of the Seg-TFET on a corrugated substrate [13]. L_G is the physical gate length. The gate oxide and shallow trench isolation (STI) consist of HfO_2 and SiO_2, respectively. The total channel width (W_G) of the active region, including the stripe height and width is 96 nm (i.e., $W_G = 6 \times (H_{RECESS} - H_{VSTI}) + 3 \times W_{STRIPE}$). Note that the layout width of the active region is labeled as W_{ACTIVE}. Figs. 1(b) and 1(c) illustrate the cross-sectional view and the top view of the Seg-TFET, respectively. W_{STRIPE} and W_{VSTI} indicate the layout width of the stripe and that of very shallow trench isolation (VSTI), respectively [13]. Three stripes are labeled as Stripe_1, Stripe_2, and Stripe_3, as shown in Fig. 1(c). The source and drain regions are heavily doped with different types of dopants (i.e., 6×10^{19} cm^{-3} for p-type sources, and 1×10^{19} cm^{-3} for n-type drains), and the channel region is lightly doped (i.e., 5×10^{15} cm^{-3}, and n-type). H_{VSTI}, H_{Ge}, and H_{RECESS} represent the height (or thickness) of VSTI, the height of Ge stripe, and the height from the

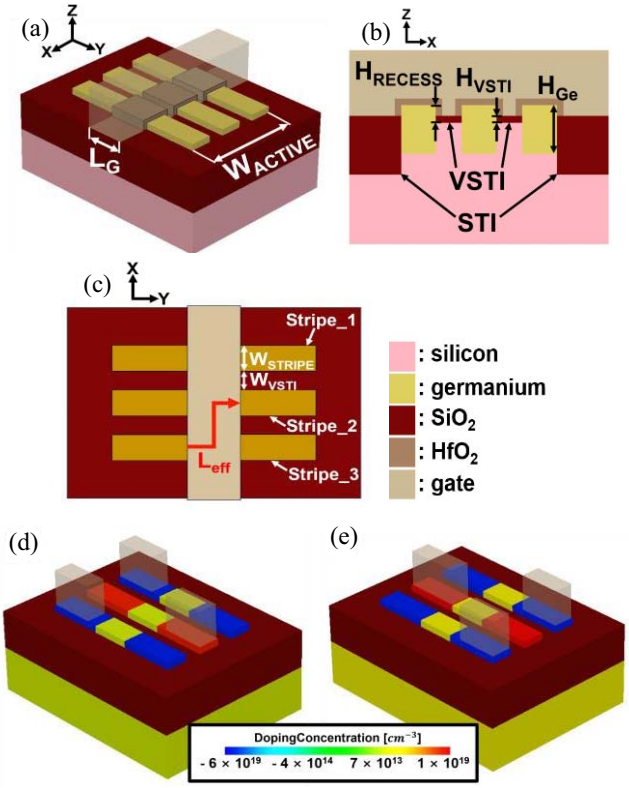

FIGURE 1. **(a) Bird's eye-view, (b) cross-sectional view, and (c) top view of the Seg-TFET. Note that each stripe has an equal source/drain width of 20 nm (= W_{STRIPE}). Each W_{VSTI} is 15 nm. The contact configurations for defining current of Seg-TFET: (d) type-I contact configuration and (e) type-II contact configuration. Note that the gate and gate oxide are removed for clarity.**

TABLE 1. **Device parameters of the optimized SEG-TFET.**

Parameter	Value	Parameter	Value
Substrate, Stripe_2	n-type	H_{VSTI} (nm)	4
Stripe_1, Stripe_3	p-type	H_{Ge} (nm)	28
L_G (nm)	35	Equivalent oxide thickness (nm)	0.76
W_G (nm)	96	H_{RECESS} (nm)	10
W_{ACTIVE} (nm)	90	Φ_M (eV)	4.05

top of the stripe down to the bottom of VSTI, respectively. The work function of metal gate is labeled as Φ_M. Note that the specific values of device parameters used in this study are summarized in Table 1.

The silicon-based corrugated substrate with germanium (Ge) stripes would be used to enhance the performance of the Seg-TFET. At first, to form the Ge stripes, Si stripes in a silicon-corrugated substrate may be selectively etched to the depth of H_{Ge} [see Fig. 1(b)], and then an *in-situ* phosphorus doped Ge (n-type, $N_C = 5 \times 10^{15}$ cm^{-3}) could be filled. Using high density plasma chemical vapor deposition (HDPCVD), STI and VSTI regions can be identified, and then chemical mechanical planarization (CMP) would be used/followed to flatten the surface. A dummy gate stack around the channel region of the device may be then used. To fabricate the dummy gate stack, the dummy gate material is deposited and then patterned. To form the heavily-doped Ge source and drain regions in the stripes (i.e., Stripe_1, 2, and 3) except for the channel region, the source/drain regions can be removed through the highly selective and isotropic etching process. Then, *in-situ*-doped p-type Ge would be selectively grown on Stripes_1 and 3 before growing *in-situ*-doped n-type Ge on Stripe_2 [15]–[17]. Finally, after removing the dummy gate stack, the gate oxide and metal gate may be fabricated by atomic layer deposition (ALD) and chemical vapor deposition (CVD).

The current flow in Seg-TFET cannot be changed once the contact configuration at metal-zero (M0)-level [previously known as contact layer, which is located right below metal-one-level in back-end-of-line (BEOL)] is set. At the M0-level, the Seg-TFET has two types of contact configurations [see Figs. 1(d) and (e)]. Fig. 1(d) depicts the type-I contact configuration, and Fig. 1(e) depicts the type-II contact configuration. (1) Type-I contact configuration: When the two contacts on the left side of the gate are chosen as the source region (of course, a contact on the right side is selected as the drain region), the electrons that are supplied by BTBT can flow from left (source) to right (drain) [see Fig. 1(d)]. (2) Type-II contact configuration: On the contrary, if the two contacts on the right side of the gate are chosen as the source region (of course, a contact on the left side is selected as the drain region), the tunneled electrons from the source region can flow to the left (drain) contact through the channel region. Therefore, these selective contact configurations at M0-level can determine the direction of drain-to-source current. This means that the proposed Seg-TFET can possibly determine the desired current direction of the device (i.e., either left to right or right to left) at the M0 contact level.

III. DEVICE SIMULATION

To investigate the device performance of Seg-TFET, both dynamic nonlocal path BTBT model and dynamic nonlocal path TAT model are used: (1) the dynamic nonlocal path BTBT model can take into account the gradient of the energy band along the total tunneling path at the source-to-channel interface in the Seg-TFET. Furthermore, this model is appropriate for abrupt heterojunctions with non-uniform electric field. Carriers (i.e., electrons or holes) are nonlocally generated at the end of the tunneling path, and thereafter, the tunneling generation rate can be calculated by integrating the tunneling path. Using Kane's and Keldysh's model [18]–[20], two coefficients (i.e., A and B parameters) that were theoretically calculated are utilized [21] and summarized in Table 2. (2) Based on the Schenk's model [23], the dynamic nonlocal path trap-assisted tunneling (TAT) model is used to address the impact of defects (e.g., dislocation) at the hetero-interface (i.e., at

TABLE 2. Theoretically calculated parameters for the nonlocal path BTBT model. The unit of A and B is $cm^{-3} \cdot s^{-1}$ and $V \cdot cm^{-1}$, respectively [21].

		Silicon	Germanium
Direct BTBT	A_{dir}	1.35×10^{20}	1.46×10^{20}
	B_{dir}	101×10^{6}	6.04×10^{6}
Indirect BTBT	A_{ind}	3.29×10^{15}	1.67×10^{15}
	B_{ind}	23.8×10^{6}	6.55×10^{6}

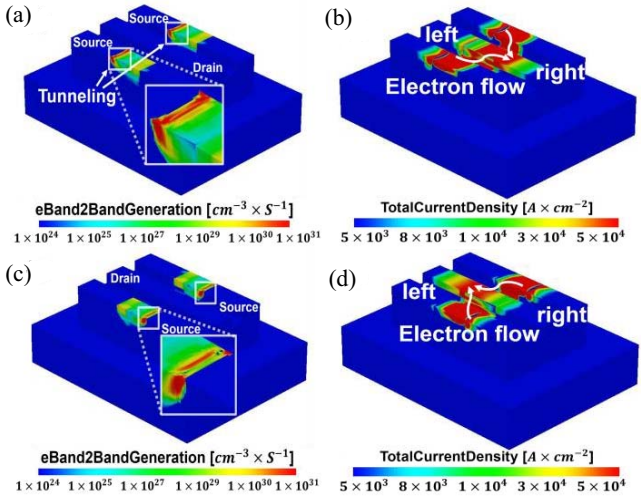

FIGURE 2. Band-to-band tunneling generation rate of electrons in the Seg-TFET for (a) type-I contact configuration and (c) type-II contact configuration. Total current density plot for the Seg-TFET: (b) type-I contact configuration and (d) type-II contact configuration.

the Si/Ge interface) [24]. Unlike Si, there is generally a slight difference between the direct bandgap of 0.8 eV at the Γ valley and the indirect bandgap of 0.66 eV at the L valley in Ge. Therefore, the simulation includes the direct and phonon-assisted tunneling process, so that reliable simulation results are obtained. Finally, the Shockley–Read–Hall recombination, drift-diffusion carrier, and doping-dependent band-gap narrowing model are activated.

IV. RESULTS AND DISCUSSION

The electron BTBT generation rate [see Figs. 2(a) and 2(c)] and total current density [see Figs. 2(b) and 2(d)] are illustrated in case of type-I and type-II contact configuration in the Seg-TFET. At the M0-level in the BEOL process, it is possible to have both types of contact configurations [see Figs. 1(d) and (e)]. When the type-I contact configuration is adopted, electrons are generated by BTBT at the interfaces of the source-to-channel region, and then the electrons can form the drain current from the left to the right of the Seg-TFET [see Figs. 2(a) and (b)]. On the other hand, when the type-II contact configuration is chosen, this configuration can allow the current to flow from the right to the left of the Seg-TFET [see Figs. 2(c) and (d)].

To investigate how the electrons in the proposed Seg-TFET move, Fig. 3 shows the step-by-step processes of electrons' flow, when the type-I configuration is adopted. First, electrons are generated by BTBT at the interfaces of

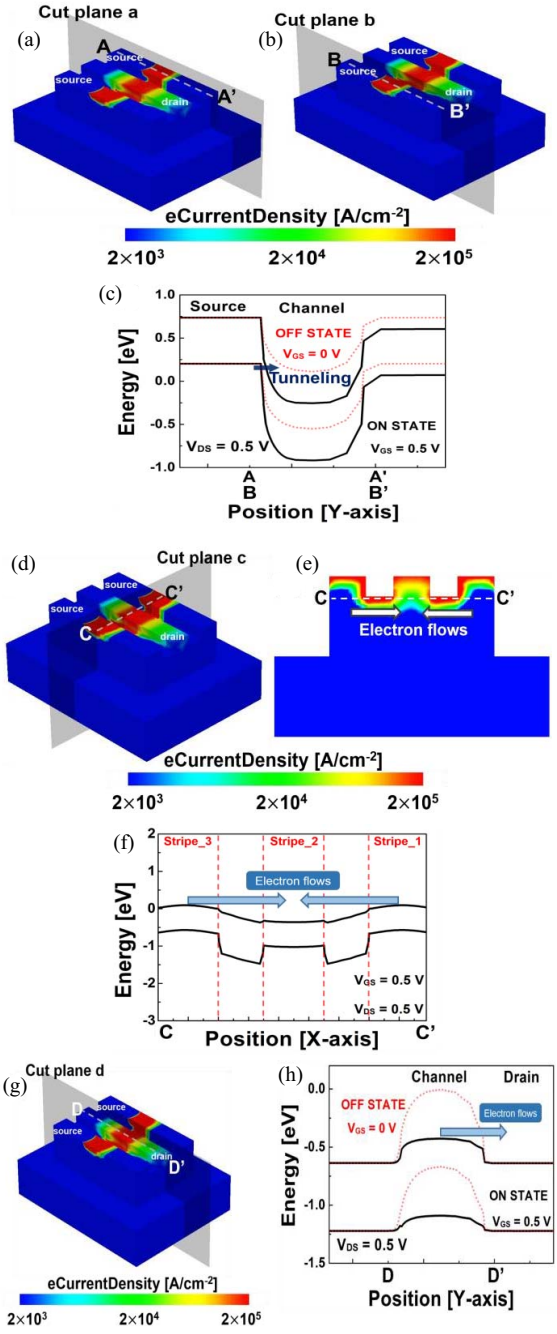

FIGURE 3. The flow process of electrons in the Seg-TFET: (a), (b), (d) and (g) electron current density in the Seg-TFET at the on-state. (c) Energy band diagrams of the Seg-TFET at on-/off-states along A-A′ or B-B′. (e) Cross-sectional view along the cut plane C-C′ without STI and VSTI regions. (f) Energy band diagrams of the Seg-TFET at on-state along C-C′. (h) Energy band diagrams of the Seg-TFET at on-/off-state along D-D′.

the source/channel in both the stripe_1 and stripe_3 [see Figs. 3(a), (b) and (c)]. Fig. 3(c) indicates the energy band diagrams at on-/off-state along the cut-line A-A' or B-B'. Second, the electrons, which are tunneled from the source regions (in both the stirpe_1 and the stripe_3), are moving towards the stripe_2 through the channel region [see Figs. 3(d), (e) and (f)]. Fig. 3(f) indicates the energy band

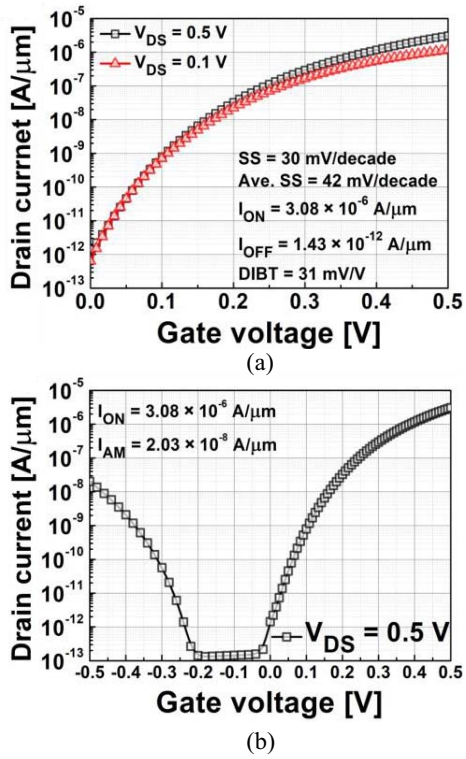

FIGURE 4. Simulated I_{DS} versus V_{GS}: (a) for V_{DS} of 0.5 V and 0.1 V (b) for V_{DS} of 0.5 V. The threshold voltage (V_{TH}) is measured when I_{DS} is 1×10^{-8} A/μm. The minimum SS is 30 mV/decade at 300K, and the average SS in the range from 0 V to V_{TH} at 300 K is 42 mV/decade. The DIBT (Drain-Induced Barrier Thinning) is 31 mV/V. The on-state drive current (I_{ON}) is 3.08 μA/μm, the off-state leakage current (I_{OFF}) is 1.43 pA/μm, and the ambipolar-state current (I_{AM}) is 2.03×10^{-2} μA/μm at $V_{GS} = -0.5$ V and $V_{DS} = +0.5$ V. Note that the power supply voltage (V_{DD}) is 0.5 V.

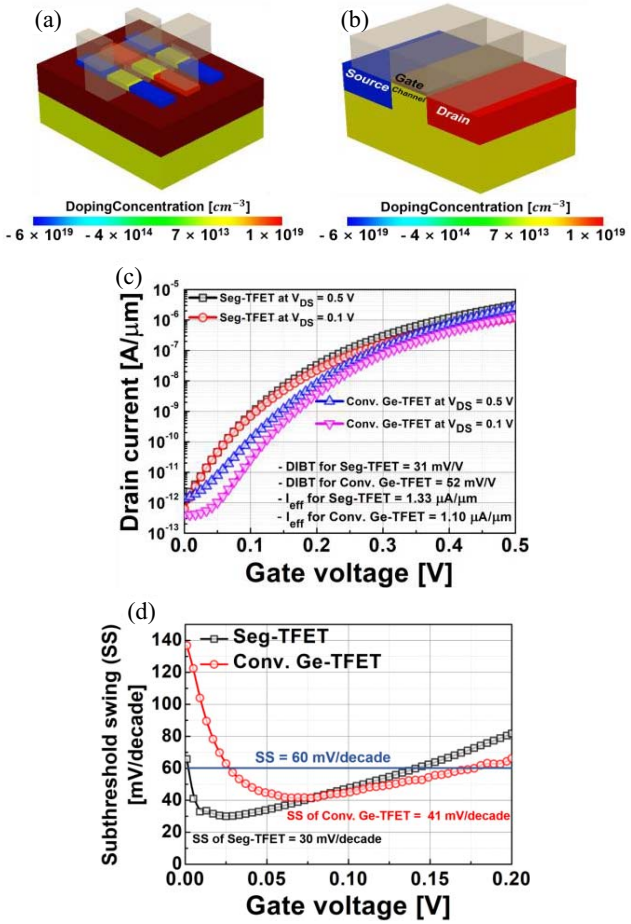

FIGURE 5. Bird's-eye view of (a) the proposed Seg-TFET and (b) the Conv. Ge- TFET. Comparisons of the Seg-TFET vs. the Conv. Ge-TFET: (c) simulated I_{DS} versus V_{GS} curves with the values of effective drive currents (I_{eff}) and DIBT, (d) subthreshold swing (SS) for the two TFETs.

diagram in on-state along the cut-line C-C'. In the end, the electrons, which come into the stripe_2, are collected by the drain contact [see Figs. 3(g) and (h)]. Fig. 3(h) indicates the energy band diagrams in on-/off-state along the cut-line D-D'. Similarly, the current flow direction can be understood, in case of the type-II contact configuration.

Figure 4 shows the simulated I_{DS} versus V_{GS} of the Seg-TFET at $V_{DS} = 0.5$ V or 0.1 V. V_{GS} is swept from 0 V to $+ V_{DD}$ (= 0.5 V) for Fig. 4(a), while V_{GS} is swept from $-V_{DD}$ to $+ V_{DD}$ for Fig. 4(b) to investigate an ambipolar current. As shown in Fig. 4(a), the Seg-TFET has an off-state leakage current (I_{OFF}) of $\sim$ 1 pA/μm and an on-state drive current (I_{ON}) of $\sim$ 3 μA/μm at $V_{DS} = 0.5$ V. The threshold voltage (V_{TH}) is defined as the V_{GS} when the drain current is 1×10^{-8} A/μm. The minimum SS is 30 mV/decade at 300 K, and the average SS, which is calculated in the range from 0 V to V_{TH}, is 42 mV/decade at 300 K. Because the Seg-TFET used a unique corrugated-substrate with some advantages [13]–[14], its lower aspect ratio of stripes in the device (i.e., the multi-striped device can be wide and short while the fin of FinFET must be narrow and tall) can suppress short-channel effects. Furthermore, because the Seg-TFET has its own VSTI regions in-between stripes, the gate-to-channel controllability can be improved because of the fringing electric fields through the VSTI regions. As a result, the drain-induced barrier thinning (DIBT) is relatively low (i.e., DIBT of the Seg-TFET is 31 mV/V). As shown in Fig. 4(b), the Seg-TFET has an ambipolar-state current (I_{AM}) of $\sim 2 \times 10^{-2}$ μA/μm at $V_{GS} = -0.5$ V and $V_{DS} = +0.5$ V. If V_{GS} is biased negatively, an ambipolar current should be appeared, where the tunneling is occurred between the stripe_1 and the stripe_2 or between the stripe_3 and the stripe_2. Herein, it is noteworthy that the ambipolar current is even lower than I_{OFF} ($\sim$ 1 pA/μm), when V_{GS} is swept down to −0.2 V.

Figure 5 shows the comparisons between the proposed Seg-TFET and a Ge-based conventional p-i-n TFET with bulk substrate (named as Conv. Ge-TFET). Herein, the Conv. Ge-TFET means an intrinsic conventional TFET (which has a well-matched physical geometry with the Seg-TFET, e.g., identical channel length [i.e., L_G for the Seg-TFET, which was indicated in Fig. 1(a)], width, and source/drain (S/D) length, etc. [see Fig. 5(b)]). Note that the active regions (i.e., source, channel and drain) for the TFET are filled with Ge but the other regions are filled with Si. Fig. 5(c) shows the

simulated I_{DS} versus V_{GS} of the two TFETs at $V_{DS} = 0.5$ V or 0.1 V. As shown in Fig. 5(c), the Seg-TFET demonstrates the improved device performance, electrostatic integrity, and benefits in terms of DIBT (e.g., the DIBT value of the Conv. Ge-TFET is 52 mV/V, while that of the Seg-TFET is 31 mV/V) and an effective drive current (I_{eff}), e.g., I_{eff} of the Conv. Ge-TFET is 1.10 μA/μm, while that of the Seg-TFET is 1.33 μA/μm. Note that I_{eff} is estimated using $I_{eff} = (I_H + I_L)/2$, where $I_H = I_{DS}$ at $V_{DS} = V_{DD}/2$ & $V_{GS} = V_{DD}$, and $I_L = I_{DS}$ at $V_{DS} = V_{DD}$ & $V_{GS} = V_{DD}/2$. Fig. 5(d) depicts the SS values for the two TFETs. Because of the aforementioned advantages of the Seg-TFET, the Seg-TFET can suppress short-channel effects as well as enhance gate-to-channel controllability through its own device structure. Furthermore, the Seg-TFET has another advantage of having a longer effective channel length (L_{eff}), due to its unique current path. As shown in Fig. 1(c), L_{eff} is defined as follow: $L_{eff} = L_G/2 + W_{STRIPE}/2 + W_{VSTI} + W_{STRIPE}/2 + L_G/2 = 70$ nm. It is noteworthy that L_{eff} is twice longer than the physical gate length ($L_G = 35$ nm). As a result, as shown in Fig. 5(d), the subthreshold swing (SS) value of the Seg-TFET is relatively reduced by the enhanced BTBT at a low gate voltage condition, i.e., the minimum SS of the Seg-TFET is 30 mV/decade, while that of the Conv. Ge-TFET is 41 mV/decade. Therefore, the proposed TFET demonstrates that its structure is more suitable for low power application.

V. CONCLUSION

A novel device structure called Seg-TFET is proposed and studied to improve its device performance for dealing with the intrinsic problems of conventional p-i-n TFET (e.g., low on-state drive current and pre-defined current direction). The Seg-TFET consists of three Ge stripes on a Si-based corrugated substrate, such that two types of contact configurations can be applied for determining the current direction in the TFET. The Seg-TFET ensures that a simple adjustment of the contact configuration at the M0-level can determine the current direction of the device, irrespective of doping process (since the location of doping for each stripe in the Seg-TFET has been pre-located).

To substantiate the structure of the novel device, a process flow scheme and a supplementary procedure for current flow were discussed. Furthermore, because all the source/drain contacts of Seg-TFET on the corrugated substrate are separately formed on different stripes and the gate-to-channel controllability is improved, the DIBT value is significantly low, e.g., DIBT $\sim$ 31 mV/V. This indicates that the drain current and the BTBT generation rate are well controlled by the gate voltage (not the drain voltage).

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