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A New Dual-Direction SCR With High Holding Voltage and Low Dynamic Resistance for 5 V Application

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ABSTRACT Dual-directional silicon-controlled rectifiers (DDSCRs), which provide both positive and negative electrostatic discharge (ESD) surge paths, are ESD protection devices with an excellent area efficiency. However, DDSCRs have a low holding voltage for use in 5 V-class applications, with a relatively high on-state resistance because of the elongated ESD surge path compared to unidirectional SCRs. In this paper, we propose a novel DDSCR with a higher holding voltage and a better ESD tolerance than conventional low-triggering DDSCRs (LTDDSCRs), realized by operating two additional parasitic bipolar transistors. The proposed ESD protection device was developed through a 0.18-μm CMOS process, and a timeline pulse system was used to verify its properties. The measurement results show that the proposed ESD protection device exhibits an improved tolerance and a high holding voltage and is expected to be reliable in 5 V-class applications

INDEX TERMS SCR, DDSCR, ESD protection device, high holding voltage, low dynamic resistance, on-resistance, current driving capability.

I. INTRODUCTION

With the increase in the requirements of low-voltage (under 5 V) applications, such as AI systems, IoT, and wearables, and with the development of semiconductor processing technology, chip area has become confined because of the high level of integration. In addition, more instances of electrostatic discharge (ESD) have been reported because of the reduction in the oxide film thickness and junction depth, resulting in more defects due to overvoltage, overcurrent, and heat generation [1], [2]. A silicon-controlled rectifier (SCR) is an ESD protection device in which both NPN and PNP parasitic bipolar transistors are latched to provide excellent current driving capability, making SCRs widely popular [3], [4]. During ESD, there are four types of discharge modes the positive-to-VSS (PS-mode), the negative-to-VSS (NS-mode), the positive-to-VDD (PD-mode), the negative-to-VDD (ND-mode), with respect to VDD, VSS, and the pad depending on the polarity (positive or negative charge) [5], [6]. As conventional SCRs are unidirectional, they are vulnerable to ESD with a negative charge. To provide protection, the protection circuit must be designed with two devices considering the polarity of the ESD, and a reverse protection diode must be included to avoid mutual interference during operation. Consequently, ESD protection circuits comprising unidirectional devices have a relatively large area. This leads to another problem in that these chips with confined areas cannot satisfy the requirement of high ESD tolerance in low-voltage applications [7]. To solve this problem, previous studies have proposed a dual-directional SCR (DDSCR)-based ESD protection device [8]–[10]. However, conventional DDSCRs have a high trigger voltage and a low holding resistance, making them unsuitable for actual IC applications. In addition, because of the elongated ESD surge path due to structural characteristics, including additional well regions, DDSCRs have a greater on-state resistance than unidirectional SCRs. Researchers have

proposed a low-triggering DDSCR (LTDDSCR) device wherein a P+ bridge region is included to reduce the high trigger voltage of the DDSCR [11], [12]. However, this device cannot ensure latch-up immunity in 5 V-class applications because of the low holding voltage. Studies have also proposed a method to increase the holding voltage by adjusting the base region of the parasitic bipolar transistor in SCR structures. Unfortunately, this further elongates the ESD surge path, thereby increasing the on-state resistance and reducing the effective ESD tolerance.

II. A NEW DUAL-DIRECTION SCR

The structures of the conventional LTDDSCR and the proposed ESD protection device are shown in Figure 1. And Figure 2 shows their equivalent circuits. As a DDSCR structure is symmetrical, it provides the same ESD surge path for both positive and negative ESD surges. Typical LTDDSCRs help lower the avalanche breakdown and reduce the trigger voltage by forming an additional P+ bridge region between the well regions. When a positive ESD is applied to terminal A, an ESD surge path is formed through the latch-mode of the two parasitic bipolar transistors (Qnpn1 and Qpnp). The proposed ESD protection device uses two PMOS structures to minimize the base region of the PNP parasitic bipolar transistor through a gate, giving it a relatively short discharge path.

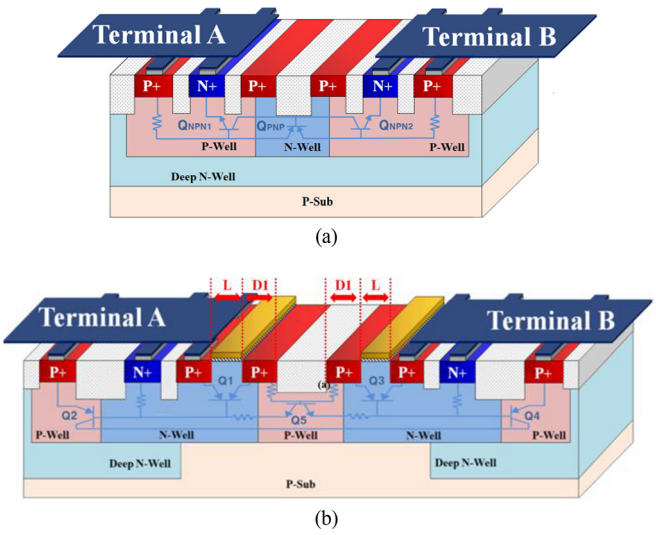


FIGURE 1. Structure of (a) low-triggering DDSCR (LTDDSCR) and (b) proposed ESD protection circuit.

The operation principles of the proposed structure are as follows. When a positive ESD surge is applied to terminal A, an avalanche breakdown occurs in the left N-well region/P+ bridge region, and the potential of the middle P region increases. If the increase in the voltage is sufficient, the forward junction of the right P+ bridge region/N-well region is turned on, and the parasitic bipolar transistor (Q1, Q2, Q3, Q5) is also turned on as a structural characteristic, thereby forming an ESD surge path. The Q2 parasitic bipolar transistor operates in parallel with the existing PNP parasitic bipolar transistor Q1 to reduce the overall on-state resistance of the ESD protection device, whereas the Q3 parasitic bipolar transistor is located on the ESD surge path and helps increase the voltage drop across the terminals A and B in the ESD mode, thereby increasing the holding voltage of the ESD protection device. Likewise, when a positive ESD surge is applied to terminal B, the four parasitic bipolar transistors will be tuned on (Q1, Q3, Q4, Q5), and an ESD surge path is formed through the same method.

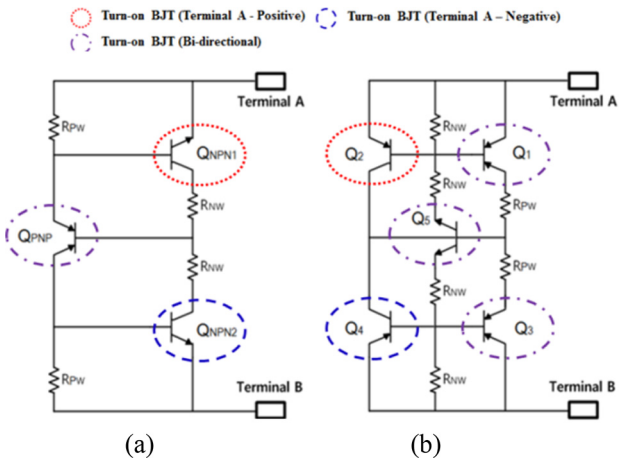
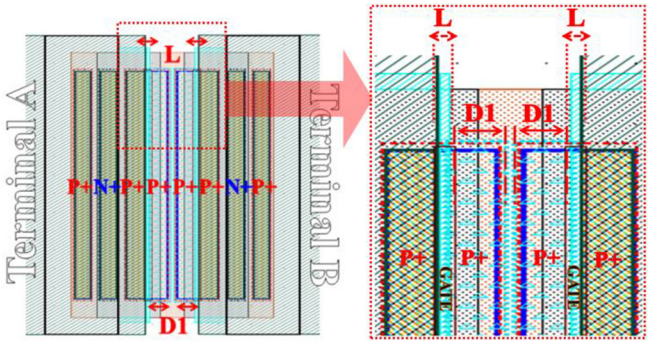
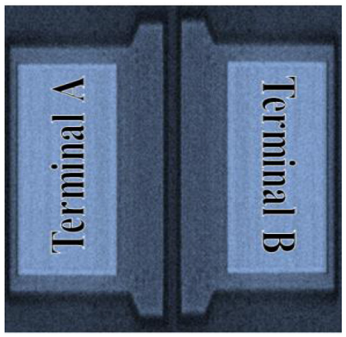


FIGURE 2. Equivalent circuit of (a) LTDDSCR and (b) the proposed ESD protection circuit.

Figure 3 shows the layout and fabrication results of the proposed ESD protection device, including the design variables. Due to the additional P + implant region formed at each terminal, the proposed ESD protection circuit has an increased area of about 10-12% compared to LTDDSCR in the same width. The proposed design variable D1 represents the length of the two proposed bridge regions the use of this variable is a conventional method of increasing the holding voltage of SCR-based ESD protection devices. The base region of the NPN parasitic bipolar transistor is adjusted to increase the holding voltage [13]. Unfortunately, this method of increasing the base region of an NPN parasitic bipolar transistor has drawbacks in terms of area expansion and significantly reduces the durability. This method increases the high concentration region. Thus, the resistance of the protection circuit is increased by reducing the current driving capability of the PNP parasitic bipolar transistors as the emitter of the PNP parasitic bipolar transistors increases. On the other hand, the design variable L represents the length of the two gates. The proposed ESD protection device can simultaneously increase the lengths of all the effective base regions of the operating PNP parasitic transistors (Q1, Q2, Q3, Q4), thus effectively increasing the holding voltage with a relatively low on-state resistance and a high effective robustness.



(a)



(b)

FIGURE 3. **(a) A layout with design variables and (b) magnified image of the proposed ESD protection circuit.**

III. RESULTS AND DISCUSSION

The proposed dual-directional ESD protection device, DDSCR, and LTDDSCR were fabricated through a 0.18 μm CMOS process.

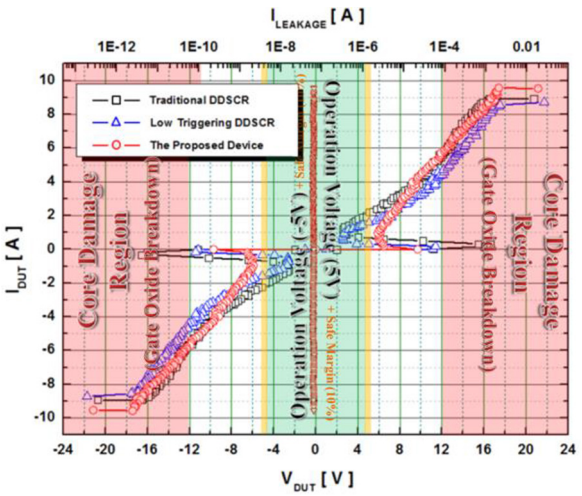


FIGURE 4. **TLP I-V characteristic curves of traditional DDSCR, LTDDSCR and the proposed ESD protection circuit.**

Figure 4 shows the TLP measurement results of the traditional DDSCR, LTDDSCR, and proposed ESD protection device [14]. ESD design window of 5V class application is formed between operating voltage +10% (margin region) and core damage region (gate oxide breakdown = 12V at 5V application). The measurement results show that the proposed ESD protection device has electrical properties suitable for use in the 5 V-class ESD design window with a trigger voltage of 9.7 V and a high holding voltage of 5.9 V in both positive and negative states. In addition, the parallel operation of the Q2 (forward) and Q4 (reverse) parasitic bipolar transistors helps increase the current driving capability, with a very low on-state resistance of 1.15 Ω. Table 1 summarizes the electrical properties of the conventional DDSCR, LTDDSCR, and the proposed ESD protection device.

TABLE 1. **The electrical properties of the DDSCR, LTDDSCR, and the proposed ESD protection device.**

Structures	*Trigger Voltage (Vt1)*	*Holding Voltage (Vh)*	*On-state Resistance (Ron)*
Traditional DDSCR	16.6 V	2.64 V	1.64 Ω
Low-Triggering DDSCR	11.2 V	2.57 V	1.79 Ω
The Proposed Device	9.7 V	5.91 V	1.15 Ω

Figure 5 shows the measurement results with respect to the design variables D1 and L. To compare the increase in the holding voltage and the reduction in the on-state resistance, the TLP measurements were conducted while increasing the D1 and L design variables by 2 μm each. According to the measurement results, compared to the conventionally used design variable D1, the lengths of the effective base regions of the four PNP transistors (Q1, Q2, Q3, Q4) are effectively increased in the case of the design variable L, thus significantly increasing the holding voltage with a very low on-state resistance. Table 2 summarizes the electrical properties according to changes in design variables.

TABLE 2. **Units for electrical properties according to changes in design variables.**

Design Parameters		*Trigger Voltage (Vt1)*	*Holding Voltage (Vh)*	*Effective Robustness*
D1	2 um	9.7 V	5.91 V	5.9 A
	4 um	10.2 V	6.78 V	4.3 A
	6 um	11.3V	7.67 V	2.8 A
L	1 um	9.7 V	5.91 V	5.9 A
	3 um	10.5 V	6.51V	5.2A
	5 um	10.7 V	7.41V	4.5A

Figure 6 shows the thermal reliability measurement results of the proposed ESD protection device and conventional LTDDSCR at 300-500k. The high temperature characteristics

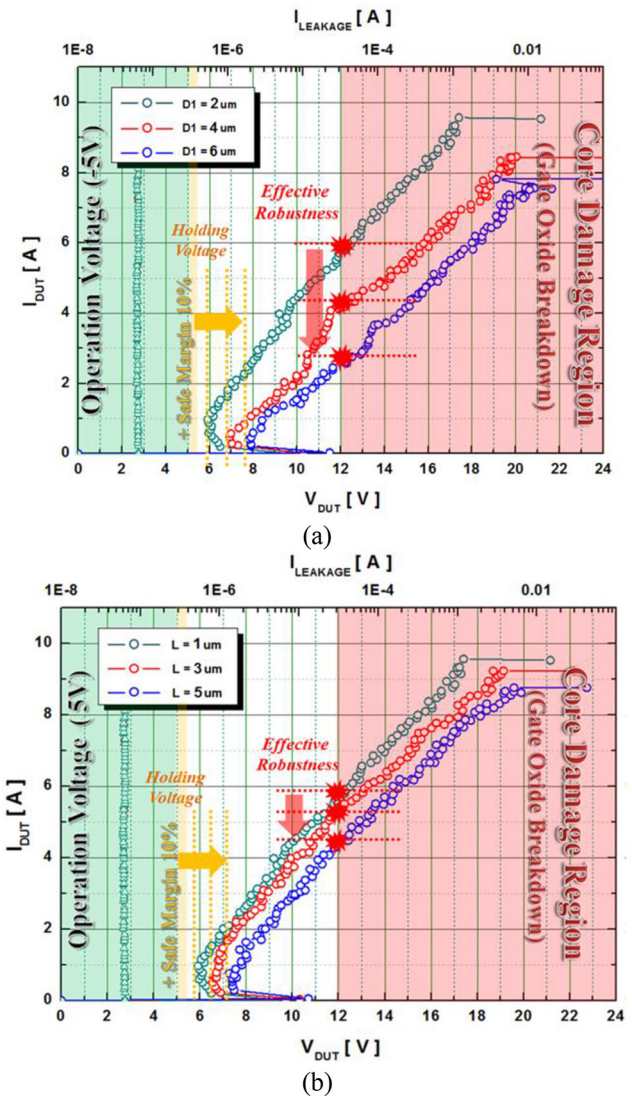


FIGURE 5. When positive ESD serge is applied to terminal A, TLP I-V characteristic curves of the proposed ESD protection circuit according to changes in (a) D1 design and (b) L variables.

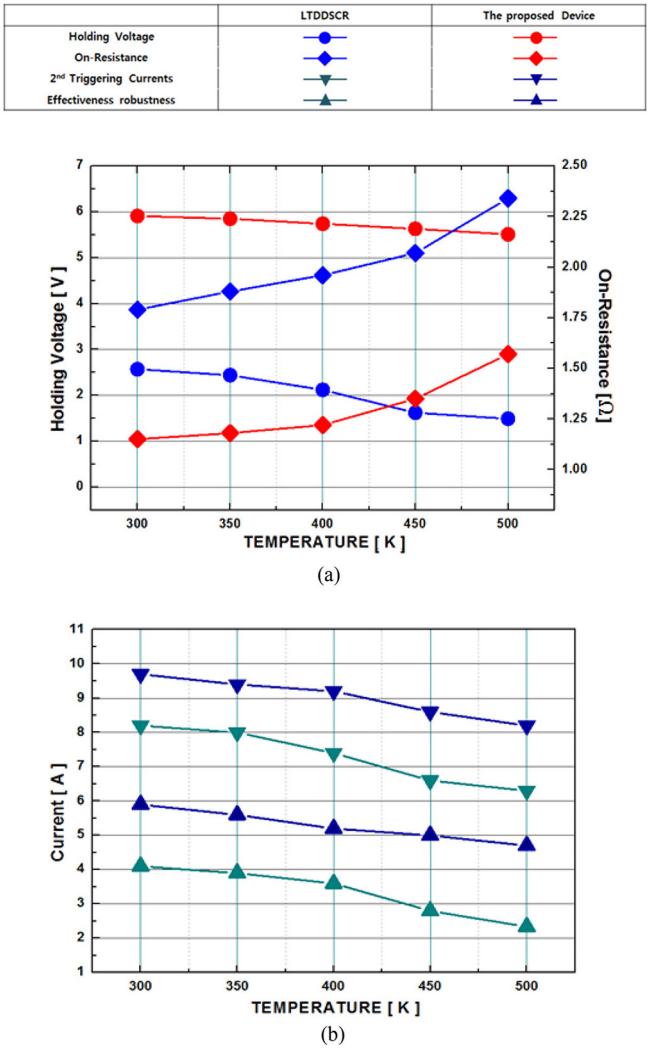


FIGURE 6. Electrical characteristic of conventional LTDDSCR and the proposed ESD protection circuit at high temperature (300 to 500 K) (a) holding voltage and on-resistance, (b) second breakdown current and effectiveness robustness.

are important because they affect the electrical characteristics and It2 of the circuit [15]. Carrier mobility at high temperatures increases the resistance value of the N well and well regions and results in a lower holding current. Also, as the base - emitter voltage (VBE) of the parasitic NPN/PNP BJTs decreases, the holding voltage decreases and heat loss occurs. Therefore, the secondary trigger current and on - resistance decrease. At 500K high temperature, conventional LTDDSCR has a holding voltage of 1.25V and a secondary trigger current of 6.2A. While on the other, the holding voltage of the proposed ESD protection device is 5.5V, still higher than the normal operating range of the internal circuit, and the secondary trigger current has 8.2A. Therefore, the proposed ESD protection device has excellent high-temperature characteristics and thermal reliability compared with conventional LTDDSCR.

IV. CONCLUSION

This paper proposed a novel DDSCR structure with a high holding voltage and a low on-state resistance. Compared to the conventional LTDDSCR, the proposed ESD protection device operates two additional parasitic bipolar transistors; the Q2 and Q4 parasitic bipolar transistors form parallel discharge paths to increase the current driving capability. The on-state resistance in the ESD state is reduced. The Q1 and Q3 parasitic bipolar transistors are both located in the discharge path during positive and negative ESD operations, thus increasing the voltage drop across both the terminals of the device. In addition, the holding voltage is effectively increased with a significantly lower on-state resistance through the design variable L compared to the conventionally used variable D1. Therefore, the proposed DDSCR-based ESD protection device exhibits a high holding voltage, an excellent current driving capability, and an

improved effective ESD tolerance. The proposed device is designed through a 0.18 μm CMOS process to be suitable for the 5 V-class ESD design window and is expected to contribute to area efficiency and reliability in 5 V-class applications.

REFERENCES

[1] M.-D. Ker and K.-C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *IEEE Trans. Device Mater.*, vol. 5, no. 2, pp. 235–249, Jun. 2005. doi: 10.1109/TDMR.2005.846824.

[2] K.-I. Do, B.-S. Lee, and Y.-S. Koo, "Study on 4H-SiC GGNMOS based ESD protection circuit with low trigger voltage using gate-body floating technique for 70-V applications," *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 283–286, Feb. 2019. doi: 10.1109/LED.2018.2885846.

[3] B.-B. Song, K.-I. Do, and Y.-S. Koo, "SCR-based ESD protection using a penta-well for 5 V applications," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 691–695, 2018. doi: 10.1109/JEDS.2018.2817636.

[4] J. Zheng *et al.*, "Robust and area-efficient nLDMOS-SCR with waffle layout structure for high-voltage ESD protection," *Electron. Lett.*, vol. 48, no. 25, pp. 1629–1630, Dec. 2012. doi: 10.1049/el.2012.3548.

[5] Z.-W. Jiang, S.-H. Chen, and M.-D. Ker, "Bi-directional SCR device with dual-triggered mechanism for ESD protection in extended-voltage-swing I/O application," in *Proc. Int. Conf. Solid State Devices Mater.*, 2009, pp. 420–421.

[6] S. Dong, H. Jin, M. Miao, J. Wu, and J. J. Liou, "Novel capacitance coupling complementary dual-direction SCR for high-voltage ESD," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 640–642, May 2012.

[7] B. B. Song and Y. S. Koo, "Low R_{on} and high robustness ESD protection design for low-voltage power clamp application," *Electron. Lett.*, vol. 52, no. 18, pp. 1554–1555, Sep. 2016. doi: 10.1049/el.2016.2391.

[8] Y. Wang, X. Jin, L. Yang, Q. Jiang, and H. Yuan, "Robust dual-direction SCR with low trigger voltage, tunable holding voltage for high-voltage ESD protection," *Microelectron. Rel.*, vol. 55, nos. 3–4, pp. 520–526, Feb./Mar. 2015. doi: 10.1016/j.microrel.2014.12.006.

[9] S. Luo, J. A. Salcedo, J.-J. Hajjar, Y. Zhou, and J. J. Liou, "ESD protection device with dual-polarity conduction and high blocking voltage realized in CMOS process," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 437–439, Apr. 2014. doi: 10.1109/LED.2014.2305634.

[10] J. A. Salcedo, J.-J. Hajjar, S. Malobabic, and J. J. Liou, "Bidirectional devices for automotive-grade electrostatic discharge applications," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 860–862, Jun. 2012. doi: 10.1109/LED.2012.2190261.

[11] J. Guan, Y. Wang, S. Hao, Y. Zheng and X. Jin, "A novel high holding voltage dual-direction SCR with embedded structure for HV ESD protection," *IEEE Electron Device Lett.*, vol. 38, no. 12, pp. 1716–1719. Dec. 2017. doi: 10.1109/LED.2017.2766686.

[12] X. Huang, J. J. Liou, Z. Liu, F. Liu, J. Liu, and H. Cheng, "A new high holding voltage dual-direction SCR with optimized segmented topology," *IEEE Electron Device Lett.*, vol. 37, no. 10, pp. 1311–1313, Oct. 2016. doi: 10.1109/LED.2016.2598063.

[13] Y. S. Koo, K. Y. Lee, K. D. Kim, and J. K. Kwon, "Design of SCR-based ESD protection device for power clamp using deep-submicron CMOS technology," *Microelectron. J.*, vol. 40, no. 6, pp. 1007–1012, 2009. doi: 10.1016/j.mejo.2009.01.001.

[14] E. Grund and M. Hernandez, "Obtaining TLP-like information from an HBM simulator," presented at the EOS/ESD Symp., Anaheim, CA, USA, Sep. 2007, pp. 2A.3-1–2A.3-7. doi: 10.1109/EOSESD.2007.4401737.

[15] Q. Cui, J. A. Salcedo, S. Parthasarathy, Y. Zhou, J. J. Liou, and J. J. Hajjar, "High-robustness and low-capacitance silicon-controlled rectifier for high-speed I/O ESD protection," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 178–180, Feb. 2013. doi: 10.1109/LED.2012.2233708.