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High Current Output Hydrogenated Diamond Triple-Gate MOSFETs

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ABSTRACT Planar-type and novel triple-gate fin-type hydrogenated diamond (H-diamond) metal–oxide–semiconductor field-effect transistors (MOSFETs) were fabricated on a single-crystalline diamond substrate. The ratio between the height of the lateral side and the width of planar side for each fin of the triple-gate MOSFETs was as high as 1.45. The leakage current densities at an electrical field strength of -1.5 MV cm^{-1} for both the planar-type and triple-gate fin-type MOSFETs were around 10^{-6} A cm^{-2}. Both MOSFETs operated well with on/off ratios as high as 10^{10}. The current output maximum normalized by the gate width of the triple-gate H-diamond MOSFET was -271.3 mA mm^{-1}, almost double that of the planar-type MOSFET. The results of this paper are expected to pave the way towards the fabrication of high current out and downscaled H-diamond MOSFETs.

INDEX TERMS Diamond, MOSFET, triple-gate.

I. INTRODUCTION

Thanks to its extraordinary intrinsic properties, wide bandgap semiconductor diamond is a promising material for the fabrication of electronic devices for low power loss, high-power, high-frequency, and high-temperature applications [1]–[3]. Recently, significant progress has been made on the development of *p*-type boron-doped bulk diamond and hydrogenated diamond (H-diamond) surface-channel-based metal-oxide-semiconductor field-effect transistors (MOSFETs) [4]–[10]. Excellent operation characteristics have been demonstrated for all of these MOSFETs. However, since the high activation energy of the boron dopant in the bulk diamond results in a relatively low sheet hole density at room temperature, the current outputs of boron-doped diamond MOSFETs were usually lower than 1.0 mA mm^{-1} [4], [5]. Conversely, the surface sheet hole density of a H-diamond channel layer is in the range of $10^{12} - 10^{14}$ cm^{-2}. The current outputs of the single-crystalline and polycrystalline H-diamond-based MOSFETs were over 200 and 1300 mA mm^{-1}, respectively [6], [7]. Additionally, the operation temperature and breakdown voltage of the single-crystalline H-diamond MOSFETs were reported to be as high as 400 °C and 1700 V, respectively [8], [9].

Although the single-crystalline H-diamond-based MOSFETs show excellent electrical properties, a lack of commercially available large-area wafers is currently preventing them from being used in practical applications. To resolve this issue, some researchers are engaged in growing wafers with diameters of over 2 inches via chemical vapour deposition techniques [11], [12]. Instead, we have tried to enhance the electrical properties of the H-diamond MOSFETs on the small area wafers. Recently, a triple-gate fin-type H-diamond MOSFET was fabricated successfully [13]. Since holes in the fin channel can travel along conducting channels on three sides (under the gate and at both lateral sides), the current output and extrinsic transconductance of fin-type MOSFETs are much higher than those of planar-type MOSFETs with the same device area. This conclusion was also confirmed by the oxygen-terminated diamond-based fin-type MOSFETs [14].

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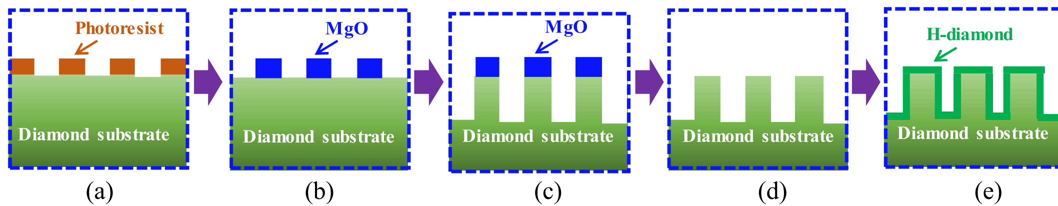

FIGURE 1. Formation process for the fin-type H-diamond epitaxial layer. (a) Fin model formation using a laser lithography system, (b) MgO formation using an evaporator, (c) diamond dry etching using an inductively-coupled plasma reactive ion etching system, (d) acid treatment for the MgO and diamond surface, and (e) H-diamond growth using a microwave plasma-enhanced chemical vapour deposition technique.

However, triple-gate fin-type H-diamond MOSFETs still have some issues that need to be addressed. Their fabrication process is relatively complicated, leading to both a degradation of their electrical properties and issues related to the repeatability of researchers' experiments by other researchers. Additionally, the best previously reported ratio between the height of the lateral side and the width of the planar side for each fin was only 0.57, which means that the fin channels' advantages are not being fully utilized.

In this study, we have simplified the fabrication process for triple-gate fin-type H-diamond MOSFETs and increased the ratio between the height of the lateral side and the width of the planar side for each fin to be 1.45 to further enhance the device current output while keeping the device area the same.

II. EXPERIMENTAL

Planar-type and triple-gate fin-type Al_2O_3/H-diamond MOSFETs were fabricated on the same Ib-type single-crystalline diamond (100) substrate. The fabrication involved several steps consisting of crossed key-patterns and fins formation, H-diamond epitaxial layer growth, mesa-structure formation, ohmic contact metals formation, Al_2O_3 deposition, and gate cover metals formation. The formation process for the fin-type H-diamond epitaxial layer was shown in Fig. 1. The diamond substrate was coated with LOR 5A and AZ 5214E/PGMEA (a volume ratio of 1:1) positive photoresists sequentially. The spin-coater's rotation rate and time were 7000 rpm and 1 s, respectively. The baking temperature and time for the LOR 5A photoresist were 180 °C and 5 min, respectively. Those for the AZ 5214E/PGMEA photoresist were 110 °C and 2 min, respectively. After exposing via a laser lithography system, the sample was developed in a TMAH solution (2.38%) for 2 min to achieve the fin model formation [Fig. 1(a)]. A 150-nm-thick MgO film was formed using an evaporator system [Fig. 1(b)]. The chamber pressure and growth rate were 6.0×10^{-5} Pa and 0.15 nm/sec, respectively. After lifting-off the photoresists, the crossed key-patterns and fins were formed simultaneously using a high-speed inductively-coupled plasma reactive ion etching system in an O_2 gas ambient [Fig. 1(c)]. The etching power, the O_2 flow rate, the chamber pressure, and the etching time were 500 W, 100 sccm, 0.5 Pa, and 10 min, respectively. The crossed key-patterns were used for fin height measurement and position calibration for the subsequent fabrication of the MOSFETs. The MgO and diamond substrate were cleaned in a mixed acid solution (H_2SO_4 and HNO_3 with a volume ratio of 1:1) at 300°C for 3 h [Fig. 1(d)]. A 50-nm-thick H-diamond epitaxial layer was grown using a microwave plasma-enhanced chemical vapour deposition technique on the fin-type diamond substrate [Fig. 1(e)]. The growth temperature, chamber pressure, H_2 flow rate, and CH_4 flow rate were 900–940 °C, 80 Torr, 500 sccm, and 0.5 sccm, respectively. By comparing the previous formation process of the fin-type H-diamond epitaxial layer [13], the new process eliminated the evaporation and etching steps for tungsten metal to make it simpler.

After the H-diamond growth, the fin height was confirmed by measuring the crossed key-pattern using a three-dimensional-measurement laser microscopy system. Mesa-structures for the H-diamond and source/drain electrodes made of Pd/Ti/Au metals for the MOSFETs were formed using a capacitively coupled plasma reactive ion etching system and an evaporation technique, respectively. A 34.5-nm-thick Al_2O_3 gate oxide film was deposited using atomic layer deposition with Ti/Au cover metals. The electrical properties of the planar-type and triple-gate fin-type H-diamond MOSFETs were measured using a MX-200/B prober and a B1500A parameter analyser.

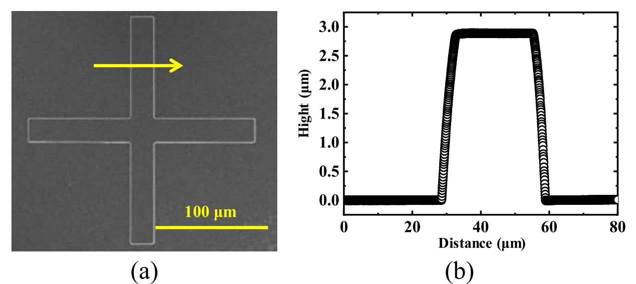

FIGURE 2. (a) Scanning electron microscopy image of the crossed key-pattern and (b) height of the lateral side for the fin-channel as confirmed by measuring the crossed key-pattern using a three-dimensional-measurement laser microscopy system.

III. RESULT AND DISCUSSION

In Figure 2, panels (a) and (b) show scanning electron microscopy image of the crossed key-pattern and height of the lateral side for the fin-channel via measurements of the crossed key-pattern using a three-dimensional-measurement laser microscopy system. The height of the lateral side

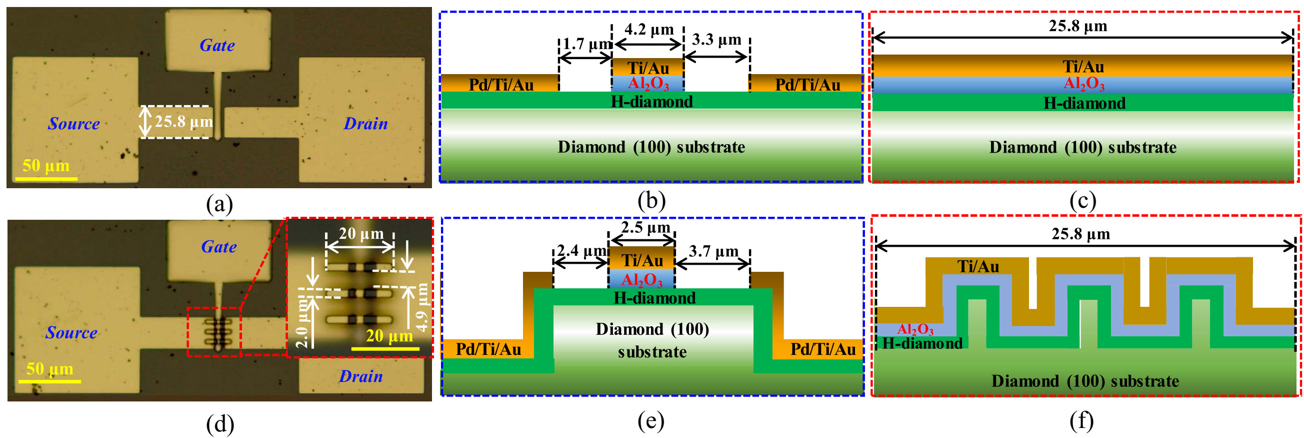

FIGURE 3. (a) and (d) Surface morphologies of the planar-type and triple-gate fin-type H-diamond MOSFETs, respectively. The inset in Fig. 3(d) shows a magnified view of the fin part for the triple-gate MOSFET. (b) and (e) Schematic diagrams of the planar-type and fin part of the triple-gate H-diamond MOSFETs, respectively. (c) and (f) Cross sectional diagrams of the planar-type and the triple-gate H-diamond MOSFETs, respectively.

for the fin-channel is 2.9 μm. The ratio between the height of the lateral side and width of the planar side for each fin were calculated to be 1.45, which is much higher than the previous report of 0.57 [13]. The gate electrode area and average L_G for the triple-gate MOSFET was calculated to be 1.4 $\times$ 10^{-6} cm^2 and 3.3 μm, respectively.

Panels (a) and (d) in Fig. 3 show the surface morphologies of the planar-type and triple-gate fin-type H-diamond MOSFETs, respectively. The inset in Fig. 3(d) shows the magnified fin part for the triple-gate MOSFET. Schematic diagrams for the planar-type and fin part of the triple-gate H-diamond MOSFETs are shown in Fig. 3(b) and (e), respectively. Cross sectional diagrams of them are shown in Fig. 3(c) and 3(f), respectively. The gate width (W_G) of both the planar-type and triple-gate MOSFETs was the same at 25.8 μm. The gate length (L_G), interspace for the gate-to-source, and interspace for the gate-to-drain were 4.2, 1.7, and 3.3 μm, respectively, for the planar-type MOSFET. The gate electrode area of the device was calculated to be 1.1 $\times$ 10^{-6} cm^2. There are three fins for the triple-gate MOSFET. Each fin had a width and length of 2.0 and 20.2 μm, respectively. The interspace between two fins was 4.9 μm. Because of the cover-area non-uniformity of the photoresist layer used during the formation of the gate oxide and cover metals, the L_G, interspace for the gate-to-source, and the interspace for the gate-to-drain were different for the triple-gate MOSFET in the planar and the fin parts. For the planar part, they were the same as those of the planar-type H-diamond MOSFET. For the fin part, they were 2.5, 2.4, and 3.7 μm, respectively.

Figure 4 shows the leakage current density (J) versus electrical field (E) characteristics for the planar-type (red line) and triple-gate fin-type (blue line) H-diamond MOSFETs. J and E were calculated via the gate-to-source leakage current divided by the area of the gate electrode and via the gate-to-source voltage (V_{GS}) divided by the gate oxide thickness

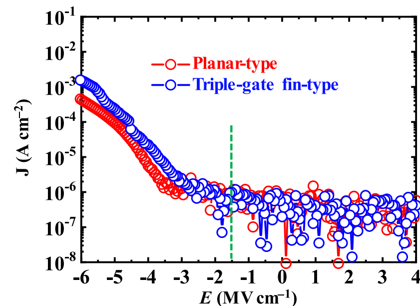

FIGURE 4. The J–E characteristics for the planar-type and triple-gate fin-type H-diamond MOSFETs.

(34.5 nm), respectively. At $E = 4.0$ MV cm^{-1}, there were almost no holes in the H-diamond channels under the Al_2O_3, and both MOSFETs had leakage current densities below 10^{-6} A cm^{-2}. At $E = -6.0$ MV cm^{-1}, hole accumulation in the H-diamond channel layer occurred, and the leakage current density for the triple-gate MOSFET was 1.5×10^{-3} A cm^{-2}, which is higher than that of the planar-type device (4.4×10^{-4} A cm^{-2}). This may potentially be attributed to the existence of fins in the H-diamond channel. The leakage current densities for both MOSFETs were around 10^{-6} A cm^{-2} at $E = -1.5$ MV cm^{-1}, which is around the same order of magnitude as in our previous report on an Al_2O_3/H-diamond MOS capacitor [15]. A low J is promising for achieving good operations with the H-diamond MOSFETs.

In Figure 5, panels (a) and (b) show the drain-to-source current versus voltage ($I_{DS} - V_{DS}$) characteristics for the planar-type and triple-gate fin-type H-diamond MOSFETs, respectively. The V_{GS} for both MOSFETs was varied from -15.0 to 15.0 V in steps of $+2.0$ V. Both MOSFETs show distinct pinch-off and p-type channel characteristics. The linear relationships between I_{DS} and V_{DS} at low voltages indicate good ohmic contacts between the source/drain electrodes

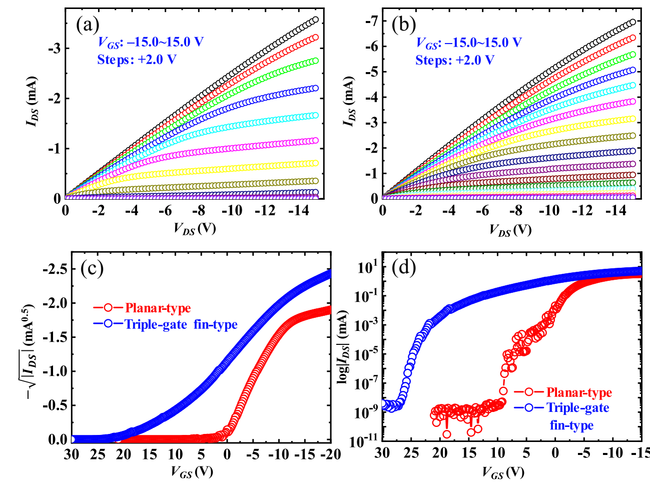

FIGURE 5. (a) and (b) The $I_{DS} - V_{DS}$ characteristics for the planar-type and triple-gate fin-type H-diamond MOSFETs, respectively. (c) and (d) The $-\sqrt{|I_{DS}|} - V_{GS}$ and log $|I_{DS}| - V_{GS}$ characteristics for the H-diamond MOSFETs, respectively.

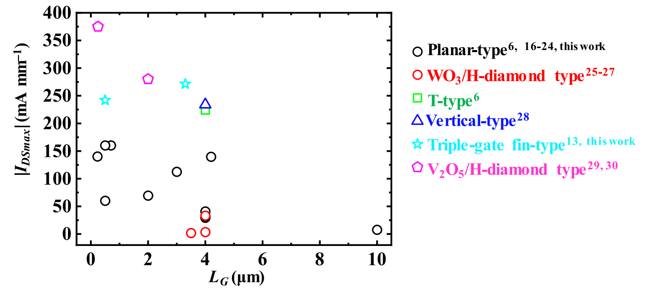

FIGURE 6. Summary of $|I_{DSmax}|$ for the H-diamond MOSFETs on single-crystalline diamond (100) substrates.

and the H-diamond channels. The I_{DS} at $V_{GS} = -15.0$ V for the triple-gate H-diamond MOSFET was −7.0 mA, which is almost double the value of −3.6 mA for the planar-type H-diamond MOSFET. Holes can travel at the both planar and lateral sides in the H-diamond fin channel, leading to a high current output for the triple-gate MOSFET. In order to compare the current outputs for both MOSFETs at the same device area, their I_{DS} maxima (I_{DSmax}) are normalized by the W_G of 25.8 μm (not effective W_G for triple-gate MOSFET). They are −271.3 and −139.5 mA mm^{-1} for the triple-gate fin-type and planar-type H-diamond MOSFETs, respectively. In Fig. 5, panels (c) and (d) show the $-\sqrt{|I_{DS}|}\ -V_{GS}$ and log $|I_{DS}|-V_{GS}$ characteristics for the H-diamond MOSFETs, respectively. The threshold voltages for the planar-type and triple-gate fin-type H-diamond MOSFETs were 0.7 ±0.1 and 15.0 ±0.1 V, respectively. Both MOSFETs operated with normally-on characteristics. The triple-gate MOSFET had a higher threshold voltage than the planar-type one, which implies that it is more difficult to make the H-diamond fin channel "off". This is possibly attributed to the rougher surface for the fin-type H-diamond channel. According to the log $|I_{DS}| - V_{GS}$ characteristics in Fig. 5(d), the on/off ratios for both MOSFETs were as high as 10^{10}. The superior line-shape for the triple-gate MOSFET compared with for the planar-type MOSFET indicates a low interfacial trapped charge density for the Al_2O_3 film on the fin-type H-diamond channel, which is in good agreement with our previous report [13].

Figure 6 summarizes the reported $|I_{DSmax}|$ for the H-diamond MOSFETs on the single-crystalline diamond (100) substrates. Even though the gate lengths for the planar-type H-diamond MOSFETs are sub-micrometre, the $|I_{Dsmax}|$ values are still lower than 160.0 mA mm^{-1} [6], [16]–[24]. Thanks to a high surface charge-transfer doping efficiency, the WO_3 on the H-diamond was able to significantly increase the channel sheet hole density. However, the $|I_{Dsmax}|$ values for the WO_3/H-diamond type MOSFETs were below 33.0 mA mm^{-1} [25]–[27]. Possible explanations for the low $|I_{Dsmax}|$ are an incomplete treatment of the surface for negatively charged adsorbates and damage of the C–H bonds on the H-diamond channel during the fabrication of the WO_3/H-diamond type MOSFETs. Since there are no interspaces between the source/drain and gate electrodes of the T-type H-diamond MOSFET, its on-resistance was much lower than that of the planar-type MOSFET, leading to a high $|I_{DSmax}|$ of 224.1 mA mm^{-1} at an L_G of 4.0 μm [6]. Holes in the vertical-type H-diamond MOSFET can also transfer at both the lateral and planar sides; its $|I_{DSmax}|$ was 234.0 mA mm^{-1} [28]. Our previous triple-gate MOSFET showed an $|I_{DSmax}|$ of 242.0 mA mm^{-1} (normalized by the W_G) at an L_G of 0.5 μm with a ratio of 0.57 between the height of the lateral side and the width of the planar side for each fin [13]. Here, we have improved the fin formation process to increase the ratio to 1.45. The $|I_{DSmax}|$ for the novel triple-gate fin-type MOSFET was 271.3 mA mm^{-1} at an average L_G of 3.3 μm. Recently, there have been new developments for the fabrication of high current output H-diamond MOSFETs [29], [30]. It has been reported that when the entire surface of the H-diamond channel is covered by a V_2O_5 film, the $|I_{DSmax}|$ values for the V_2O_5/H-diamond type MOSFETs are as high as 280.0 and 375.0 mA mm^{-1} at an L_G of 2.0 and 0.25 μm, respectively [29], [30]. Although the $|I_{DSmax}|$ (271.3 mA mm^{-1}) of our novel triple-gate MOSFET is lower than those values, we expect that this value could be further increased by decreasing the L_G of 3.3 μm to sub-micrometres. Moreover, it is also expected that covering the fin-type H-diamond channel with a V_2O_5 film will generate a much higher $|I_{DSmax}|$ for the MOSFETs. It should be noted that the $|I_{DSmax}|$ values for the single-crystalline H-diamond (100)-based MOSFETs were much lower than for NO_2-treated polycrystalline H-diamond-based devices (1350 mA mm^{-1}) [7]; there are two possible explanations for this. (1) The NO_2 treatment may increase the sheet hole density of the H-diamond channel to around 10^{14} cm^{-2} [31]. (2) Conversely, other H-diamond planes such as (111) in the polycrystalline diamond may have higher sheet hole densities than the (100) plane [32].

IV. CONCLUSION

In this study, a novel triple-gate H-diamond MOSFET was fabricated with a ratio for each fin of 1.45 between the height of the lateral side and the width of the planar side. The I_{DSmax} of the triple-gate fin-type MOSFET was significantly higher than for the planar-type H-diamond MOSFET. In a follow-up study, we plan to decrease the L_G to the sub-micrometre scale for this triple-gate H-diamond MOSFET to further increase the current output; this would pave the way for the fabrication of high current out and downscaled H-diamond MOSFETs.

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