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2-Bit/Cell Operation of $Hf_{0.5}Zr_{0.5}O_2$ Based FeFET Memory Devices for NAND Applications

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ABSTRACT The multilevel memory performances of ferroelectric field effect transistor (FeFET) with $Hf_{0.5}Zr_{0.5}O_2$ (HZO) ferroelectric thin film are investigated. First, similar retention characteristics are observed for intermediate and saturated polarization states of HZO ferroelectric thin film, which enables memories for multi-bit data storage. And then, 2-bit/cell operation of HZO-based FeFET is demonstrated utilizing two NAND architecture compatible write schemes of varying program pulse amplitude and width. Low cycle-to-cycle variability, long retention to extrapolation of 10 years at 85°C, and endurance of 500 cycles are achieved for the both schemes. Moreover, the mechanism for multilevel memory operations of the FeFET is illustrated based on the polarization switching dynamics of HZO ferroelectric thin film.

INDEX TERMS FeFET memory, $Hf_{0.5}Zr_{0.5}O_2$, 2-bit/cell, write schemes, retention, endurance.

I. INTRODUCTION

Hafnium oxide (HfO_2) based ferroelectric field effect transistor (FeFET) memory is a promising contender among the emerging non-volatile memories for mass storage applications, with the sign of excellent process compatibility, low power, fast speed and Flash-like structure [1]–[3]. Fascinatingly, it could make use of existing NAND Flash manufacturing environments, such as memory array and integration technologies. Moreover, it was demonstrated that HfO_2 based 3D-FeFET memory could address most issues of 3D NAND Flash for aggressively scaling and allow for a longer scaling path, thereby becoming remarkably attractive for mass storage applications [4]. On the other hand, multilevel memory cell technology is an effective way for low cost, high density memory applications, which has been intensively developed along with the evolution of NAND Flash integration technologies [5]. Thus, it is imperative to explore the multilevel memory performances of HfO_2 based FeFET memory devices for NAND applications.

Recently, the multilevel behaviors in the HfO_2 based FeFETs have been reported by some researchers, and they were harnessed to mimic brain synapses for neuromorphic applications [6]–[10]. For example, a 32-state (5-bit) $Hf_{0.5}Zr_{0.5}O_2$ (HZO) based FeFET synapse with symmetric potentiation and depression characteristics was demonstrated based on the voltage-controlled partial polarization switching dynamics [9]. Moreover, it has been revealed that the multilevel capability of the HfO_2 based FeFET devices is driven by the gradual polarization switching behaviors of HfO_2 based ferroelectric thin film. However, the critical memory characteristics (i.e., write variability, endurance and retention) of the multilevel HfO_2 based FeFETs were seldom investigated. Especially, the systematical studies on the stability of the subloop operations (i.e., intermediate polarization states) for the FeFETs are required.

Among the HfO_2 based ferroelectric thin films, HZO is widely used for device applications [1], [2], [7]–[13], which can be realized more easily in mass production due to homogenously and reproducibly doping [14]. In this work, memory characteristics of the 2-bit/cell (the common multilevel memory cell) HZO based FeFET memory are systematically investigated utilizing two NAND architecture compatible write schemes.

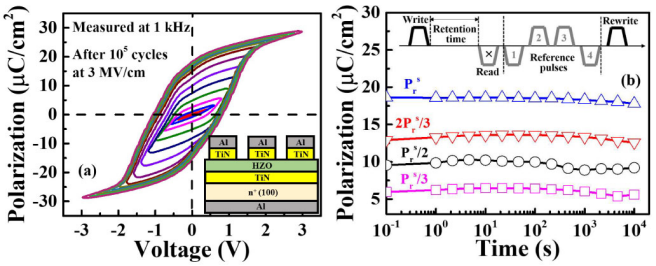

FIGURE 1. **(a) *P-V* hysteresis loops for MFM capacitors. (b) Retention properties of various polarization states of MFM capacitors including saturated polarization (P_r^s) and intermediate polarization states ($P_r^s/3$, $P_r^s/2$, $2P_r^s/3$).**

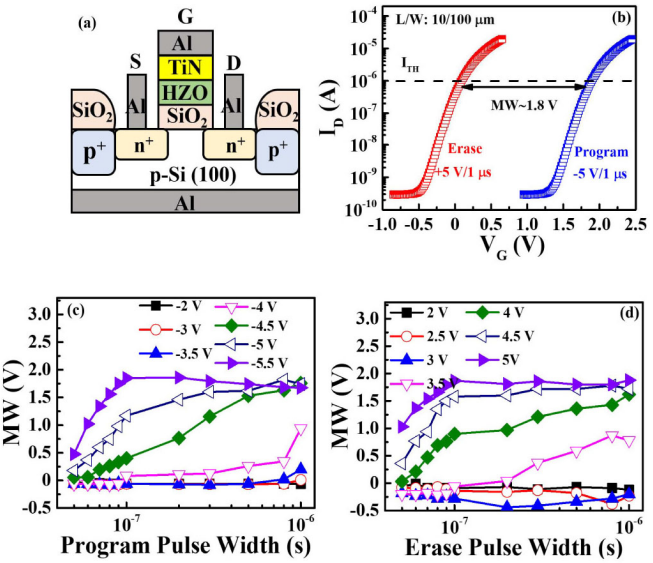

FIGURE 2. **(a) Schematic of the fabricated FeFET. (b) I_D–V_G characteristics of a FeFET after an erase pulse (+5 V/1 μs) and a program pulse (−5 V/1 μs). (c) and (d) are the *MW* of the studied FeFET as a function of program and erase pulse width for varying pulse amplitudes, respectively.**

II. EXPERIMENTS

Metal-ferroelectric-metal (MFM) capacitors were prepared by deposition of a Al/TiN/HZO/TiN film stack on n^+-Si(100) substrates. A 10-nm-thick HZO layer was formed by alternately depositing HfO_2 and ZrO_2 layer through ALD process. For crystallization, annealing was performed at 600°C for 30 sec in N_2 following the formation of TiN top electrodes. The n-channel FeFETs with an Al/TiN/HZO/SiO_2/Si gate stack were fabricated using a gate last process. Following the formation of source (S)/drain (D), a 3-nm-thick SiO_2 buffer layer was grown on the chemically cleaned active area by dry oxidation. Afterward, the TiN/HZO film stack was deposited and annealed utilizing the same process for MFM capacitors. Finally, after opening contact holes at S/D region, the contact was formed by Al metal deposition, patterning, and annealing at 400°C.

III. RESULTS AND DISCUSSION

Polarization hysteresis ($P-V$) loops of an MFM capacitor are shown in Fig. 1(a), where the inset is a schematic of the MFM. Initially, the wake-up process was carried out by cycling the MFM capacitor with alternating switching pulses at ±3 MV/cm (10 kHz) for 1×10^5 cycles. After wake-up cycling, a characteristic transformation from a linear-loop behavior to sub-loop behaviors and a well saturated ferroelectric hysteresis is observed when increasing the applied voltage from 0.2 to 3 V, which indicates the coexistence of multi domains and the possibility of multilevel polarization applications [7]. The remanent polarization (P_r) at saturated state (P_r^s) is 18.6 μC/cm^2 and coercive electric field (E_c) is 0.95 MV/cm. Moreover, the retention properties are characterized. The inset of Fig. 1(b) shows the pulse sequence for retention measurement, where the write pulse is used to establish a defined polarization state and the five pulses (×, 1, 2, 3, and 4) are used to read the absolute value of the polarization after a certain retention time [15]. As shown in Fig. 1(b), the four polarization states (P_r^s, $2P_r^s/3$, $P_r^s/2$ and $P_r^s/3$) are very stable, with 4.3%, 2.3%, 4.2% and 6.6% polarization loss after 10^4 s for P_r^s, $2P_r^s/3$, $P_r^s/2$ and $P_r^s/3$, respectively. The remarkable stability of these intermediate polarization states is similar to that of P(VDF-TrFE) and PZT based MFM capacitors [16], which might originate from the coexistence of effectively independent domains, with different polarizations due to different values of the coercive field. Thus, the stable retention properties of intermediate and saturated polarization states in the HZO thin film demonstrate its ability for multi-bit data storage.

Fig. 2(a) shows a schematic of the fabricated HZO based FeFETs, which has a gate length (L) and width (W) of 10 μm and 100 μm, respectively. Fig. 2(b) shows the transfer characteristics (I_D–V_G curves) responding to a 1-μs −/+5-V program (Prg)/erase (Ers) pulse of a fabricated FeFET. Clearly, the shift of I_D–V_G curves opposite to the polarity of the applied pulses is induced, indicating that the hysteresis is originated from polarization switching of HZO ferroelectric thin film. The hysteresis width of the FeFET known as memory window (MW) is defined as the difference of threshold voltage (V_{TH}) values between programed and erased states, where the V_{TH} can be determined as a gate voltage corresponding to a specified value of drain current (I_{TH}) at 10^{-7} A·W/L [17]. The large MW ~1.8 V of the studied FeFET might be the largest one among the reported HfO_2 based FeFETs [6]–[9], [18]–[20], which would be more practical to achieve more distinctly separate states compared with the previously announced results [6]–[9]. Moreover, detailed program/erase characteristics of the FeFET are elucidated for pulses with varying pulse width (50 ns-1 μs) and amplitude (2-5.5 V), shown in Figs. 2(c) and (d). Prior to each write pulse (Prg or Ers), the FeFET cell is set into an erased or programmed state by applying an initialization pulse of +5 V/1 μs or −5 V/1 μs, respectively. One can see that no polarization reversal (MW~0) is detected up to 1 μs in the voltage range between −3 V and +3 V. When the absolute value of the

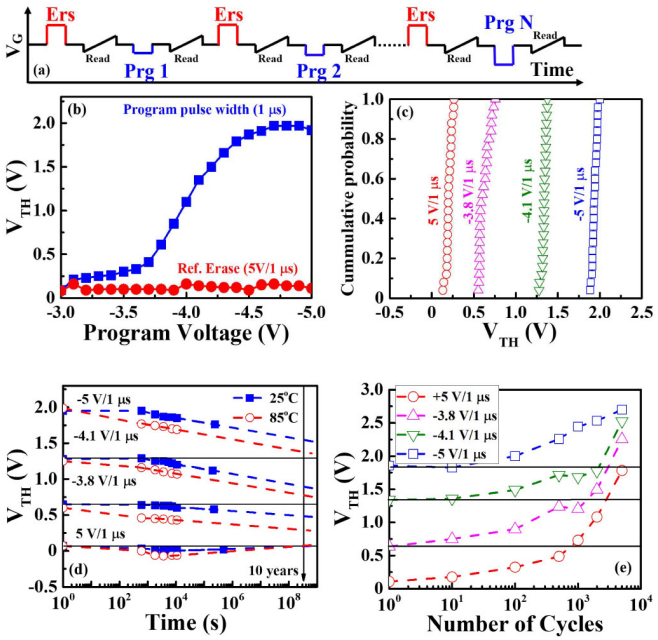

FIGURE 3. (a) V_G waveform scheme for varying program voltage. (b) V_{TH} as a function of program voltage referring to erase operations. (c) Distribution of V_{TH} levels for repeated write operations. (d) Retention properties of the four V_{TH} states. (e) Endurance properties of the four V_{TH} states cycled at ±5 V/1 μs.

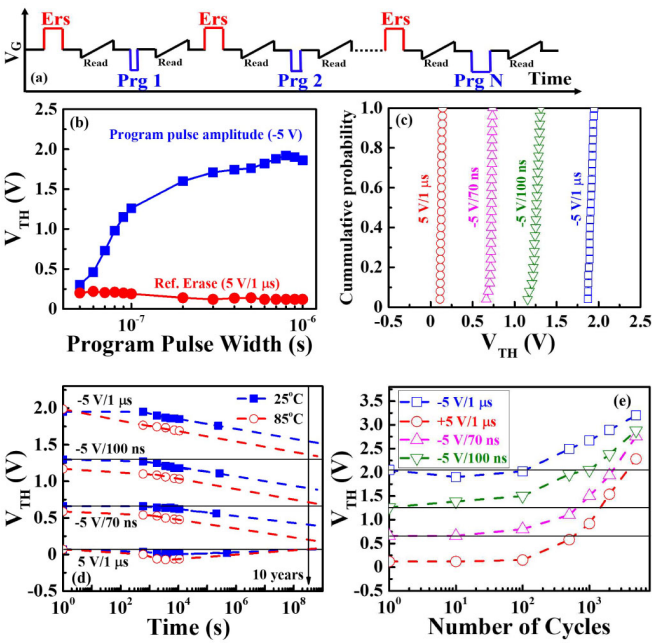

FIGURE 4. (a) V_G waveform scheme for varying program pulse width. (b) V_{TH} as a function of program pulse width referring to erase operations. (c) Distribution of V_{TH} levels for repeated write operations. (d) Retention properties of the four V_{TH} states. (e) Endurance properties of the four V_{TH} states cycled at ±5 V/1 μs.

applied voltage is larger than 3 V, varying Prg/Ers pulse amplitude or width results in various *MW* values, which highly agrees with the general trend of polarization switching in ferroelectrics [21]. This behavior holds for multilevel operation of the FeFET device.

In NAND Flash applications, the conventional and incremental step pulse program (ISPP) schemes are based on varying program pulse width and amplitude, respectively [5]. Thus, the multi-bit memory operations of the studied FeFET are investigated with the two write schemes. First, the ISPP waveforms of V_G shown in Fig. 3(a) is adopted with increasing program pulse amplitude of 0.1 V/step. Fig. 3(b) shows gradual switching events as a function of program pulse amplitude. Four separate V_{TH} states are set by applying V_G pulses with −3.8 V/1 μs, −4.1 V/1 μs, −5 V/1 μs, and +5 V/1 μs, respectively. Fig. 3(c) shows the cumulative distributions of the corresponding four V_{TH} states by repeating write procedures for 25 times for each considered state, indicating a very low cycle-to-cycle variability. The solid and open symbols in Fig. 3(d) show that there is no significant degradation for the four V_{TH} states during retention measurements both at 25°C and 85°C. According to the read margins indicated by the black solid lines and symbol-dash lines, the states can be distinguished up to extrapolation of 10 years at both temperatures. Moreover, the remain read margins for 2-bit/cell operation of the studied FeFET are comparable to those for 1-bit/cell operation of the previously reported HZO based FeFET [18], which are contributed by the large *MW* and stable intermediate polarizations. In addition, Fig. 3(e) shows the evolution of the four V_{TH} states over cycling. The *MW* between Prg (−5 V/1 μs) and Ers (+5 V/1 μs) degrades after 5000 alternating Prg (−5 V/1 μs) and Ers (+5 V/1 μs) cycles, which is mainly caused by oxide charge trapping and interface trap generation [22]–[24]. The four V_{TH} states remain separated up to 5000 cycles and can be sensed after 500 cycles according to the read margins. The strategies of reducing the interfacial field stress and heating techniques for damage recovery can be utilized to improve the endurance limitations [25], [26]. On the other hand, the 2-bit/cell operation is demonstrated by varying program pulse width, which is schematically shown in Fig. 4(a). As shown in Fig. 4(b), consecutive V_{TH} values are obtained by increasing program pulse width from 50 ns to 1 μs at −5 V. Similar to ISPP scheme, low cycle-to-cycle variability, long retention to extrapolation of 10 years at 85°C, and endurance of 500 cycles of four separate V_{TH} states realized by +5 V/1 μs, −5 V/70 ns, −5 V/100 ns and −5 V/1 μs can be seen in Figs. 4(c), (d), and (e), respectively.

Note that the polarization reversal of HZO ferroelectric thin film and other HfO_2 based ferroelectric thin films follows the nucleation limited switching (NLS) model [27]–[29]. Primarily, the polarization reversal was considered as an ensemble of elementary regions that switch independently with a distribution of switching times. This distribution of switching times was attributed to variations in local electric fields when a uniform external field is applied,

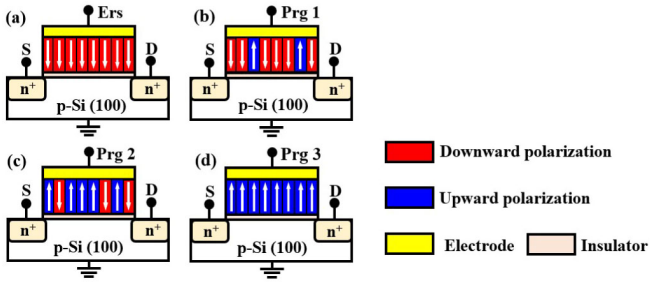

FIGURE 5. (a)-(d) are schematics for four V_{TH} states of FeFET with saturated downward polarization (Ers), intermediate polarizations including a few (Prg 1) and more (Prg 2) upward domains among downward domains, and saturated upward polarization (Prg 3), respectively.

due to impurities or crystal defects. Generally, the characteristic switching time τ (i.e., the unique waiting time for domain nucleation of elementary regions) is expressed as [27]

$$\tau(E_a, E) = \tau_\infty exp\left\{\left(\frac{E_a}{E}\right)^a\right\} \quad (1)$$

where E_a is the activation field, τ_∞ is the time constant obtained for an infinite applied field, and a is an empirical parameter (≥ 1). The value of local electrical field E can be obtained by $E = \eta E_{ext}$, here E_{ext} is the applied external field and η is a random variable with probability density function (PDF) f(η). Accordingly, the mechanism of write operation corresponding to 2-bit/cell in FeFET memory could be schematically depicted as Fig. 5, where the domains only with upward or downward polarization are considered. At the beginning, all the domains are assumed to be downward as shown in Fig. 5 (a), because the positive V_G pulse (+5 V/1 μs) is high enough. As for ISPP scheme, when the amplitude of negative V_G pulse increases from −3 V to −5 V, the relative value of local electrical field E increases, and the characteristic switching time τ decreases based on Eq. (1). Since the downward domains exceeding the local characteristic switching time in the HZO film will switch to upward, the proportion of upward domains increases with increasing the pulse amplitude. Besides, for the scheme of varying the V_G pulse width, the characteristic switching time τ follows the probability density function f(η) due to the constant E_{ext}. The proportion of downward domains induced to reversal also will increase with increasing the pulse width from 50 ns to 1 μs. The behavior for a few downward domains reversal realized by the two schemes (−3.8 V/1 μs, −5 V/70 ns) is schematically shown in Fig. 5 (b), and that for more downward domains reversal induced by the two schemes (−4.1 V/1 μs, −5 V/100 ns) is shown in Fig. 5 (c). Fig. 5 (d) represents the completely reversal of domains from downward to upward realized by the relatively high negative V_G pulse amplitude or width (−5 V/1 μs). In a word, various ratios of upward and downward domain achieved by varying pulse amplitude or width produce different net values of polarization or E_c responsible for V_{TH}, which favors multilevel operation of the FeFET. Moreover, the coexistence of effectively independent domains in the HZO film contributes to the stability of the multi-states in the HZO based FeFET device [16], [30]. On the basis of the above-mentioned mechanism, the uniform coexistence of multi domains in the gate region ($W \times L$) is necessary for multilevel memory applications. Because of the spatial distribution of dielectric and ferroelectric grains as well as the grain size distribution, the variability from cell to cell would be prohibitive for the reliable operation when scaling the gate dimension of FeFET. To implement highly scaled multilevel FeFET memory device, in addition to the film engineering [30], nonplanar configurations might be the candidates due to the large effective W, such as FinFET devices [10] or 3-D memory array architectures [31].

IV. CONCLUSION

The 2-bit/cell operation in HZO based FeFET memory device for NAND architecture applications was demonstrated. Our results show that the stable retention of intermediate polarization states in the HZO ferroelectric thin film enables its memories for multi-bit data storage. Moreover, 2-bit/cell operation of HZO-based FeFET with low cycle-to-cycle variability, long retention to extrapolation of 10 years at 85°C, and endurance of 500 cycles were achieved utilizing two NAND architecture compatible write schemes. The operation principle of 2-bit/cell HZO based FeFET is based on the polarization reversal of HZO ferroelectric thin film following nucleation limited switching model. But further studies are required for practical engineering applications, such as enlarging the memory window, controlling device-to-device variability, improving the endurance, etc.

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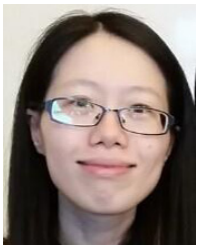

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