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Crystallization Speed in Ge-Rich PCM Cells as a Function of Process and Programming Conditions

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ABSTRACT Quenching-time characterization is the way to measure the speed of chalcogenide material to transform from the amorphous (RESET) state to the crystalline (SET) one after application of a proper programming pulse. It is here proposed to study the impact of process and programming conditions on cell performances, highlighting possible composition variation, and modifications of the physical dimension of the PCM active volume (the dome).

INDEX TERMS Amorphous, chalcogenide, phase change memory (PCM), Ge-Sb-Te (GST) compounds, quenching time, resistance, data retention.

I. INTRODUCTION

Phase Change Memory (PCM) is considered, since many years, one of the most reliable, mature and ready for industrialization concept (among BEOL memories) to replace Floating Gate Non Volatile Memories cells [1]. It has been proven to be compliant with the very demanding Automotive requirements (some years at 150°C) and also able to guarantee Code integrity after assembly on a board (Soldering Reflow thermal profile reaching 260°C as peak temperature for few minutes) on multi Mb-array. To fulfill reliability requirements, specific in particular of embedded Non Volatile Memories for Microcontrollers, an optimized Ge-rich GexSbyTez chalcogenide material has been developed and proposed in [2]. It shows definite improvement in thermal stability with respect to conventional Ge2Sb2Te5 (GST 2-2-5). The increase of Ge concentration is known to reduce GST programming speed: nevertheless the performances in time obtained at array level are definitely better than those today granted by conventional Floating Gate memories for embedded applications, where small code modifications are often needed by applications.

The use of programming parameters like the trailing edge of a reset pulse has been already used to study behavior of phase change memory devices [3], [4]. In this work we use this quick and simple electrical test as monitor of local material properties as a function of different process and programming conditions.

II. EXPERIMENTAL

Electrical characterizations have been performed on Wall-like PCM cells [5] fabricated on 28nm FD-SOI Technology [6]. Cell architecture is characterized by a strip of chalcogenide material laying on top of a thin heater element. This solution is very effective since it allows PCM integration in the Back End Of the Line process with very few dedicated masks (+3 only for storage element definition).

Fig. 1 is a TEM image of PCM array (organized with MOS Select Transistor). GST line width (W_{GST}) is the geometrical dimension of storage element varied at design level and considered among the parameters possibly impacting quenching time figure of merit. W_{GST} is in fact one of the main geometrical parameters driving the cell electrical properties since it defines the target programming current and the portion of GST volume that will become amorphous during RESET operation.

Quenching time characterization consists of a sequence of programming pulses with same max current and an interleaved Read pulse (at low V_{READ}) to monitor the evolution

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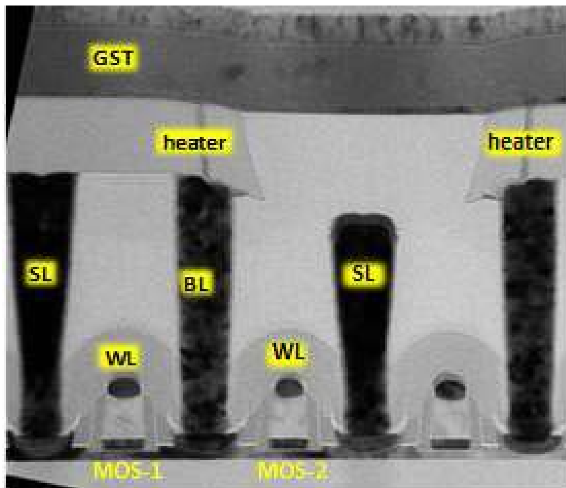


FIGURE 1. TEM image (X-direction). Select Transistor is realized through the parallel of 2 elementary MOS transistors sharing same BL (MOS-1 and MOS-2).

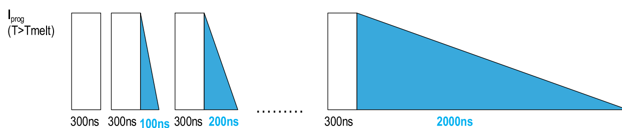


FIGURE 2. Sequence of programming pulses adopted for Quenching-time characterization.

of cell resistance value (Fig. 2). Every programming pulse differs from the previous one only for what concerns the falling time, increased from 0ns to few ms (with step of 100ns). Rising time and pulse width are kept constant (20ns and 300ns respectively). The very first pulse of the sequence is indeed a Reset Pulse (box shaped) that leaves the cell in the amorphous state. The increase of the falling time makes the pulse more and more able to crystallize the GST thanks to less abrupt cooling phase (i.e., increased quenching time). The constant max current (granting a fully melted material) ensures that the cell starts every time from the same physical state and the unique effect measured during the read phase is the PCM-resistance modulation induced by the specific pulse.

III. RESULTS AND DISCUSSION

A. IMPACT OF PROCESS CONDITIONS

GST-alloy in the Ge-rich region of Ge-Sb-Te ternary diagram exhibits much higher crystallization temperature with respect to conventional 2-2-5 (whose crystallization $T_x \sim 150°C$): this has been considered as guideline for material engineering to improve Data Retention properties and match applications targets. Any induced alteration of the alloy composition or stoichiometry, with respect to the as deposited one, will be reflected on cell electrical performances (in particular from Data Retention perspective).

Fig. 3 shows median R_{READ} evolution (wafer map) of experiments carried out on 3 different Process of Reference (POR).

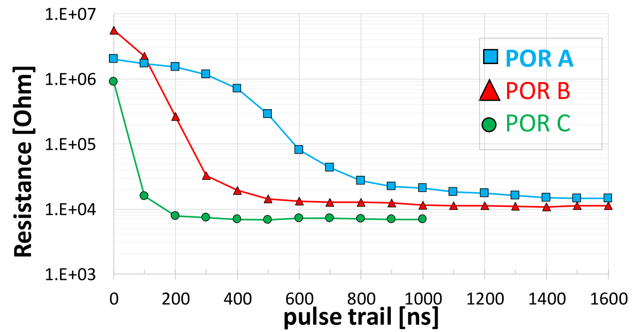


FIGURE 3. R_{READ} median evolution : POR A & POR B (Ge-rich alloy with different process optimizations); POR C (conventional GST-alloy).

POR A = Ge-rich alloy optimized process
POR B = Ge-rich alloy starting process
POR C = Conventional GST 2-2-5

Optimized process includes modification of few key integration steps after GST deposition. The difference between POR A and POR B is not in terms of "as deposited" GST-alloy (that is kept the same) but in terms of locally alteration of the alloy itself induced by process steps that follow the GST deposition brick. In fact, the process steps after the GST deposition can lead to Ge segregation that locally modifies the material composition in the melted region and consequently in the amorphous dome. Starting process POR B clearly shows a different behavior with respect to the optimized POR A, by keeping same cell geometry and experimental set-up. The "not optimized" process (POR B) looks similar to a GST-alloy with less Ge content that needs shorter trailing time to crystalize moving toward the curve of GST 2-2-5 (POR C).

This difference in terms of Ge content between POR A and POR B on quenching time is confirmed also by Reset Retention performances. Fig. 4 shows results of Reset Retention monitor: after programming to reach Reset state (see gray prebake distribution), wafers are baked (1h / 230°C) and read. POR B is significantly worse than POR A in terms of data-loss: more than 70% of cells (data sample = 30 cells) reached a crystalline state. The deposited Ge-rich alloy end of process in this case (POR B) appears to have less Ge content in the amorphous dome (and so a worsened Reset retention capability). Quenching time figure of merit seems a good way to highlight differences of the alloy composition in the active region or possible material degradation not visible with conventional techniques of physical analysis such as EDX or EELS. The accuracy of these techniques ranges $+/-5\%$. Cell behavior is sensitive to local composition change lower than this range.

B. IMPACT OF CELL GEOMETRY

The 3D-rendering of array organization is reported in Fig. 5a. The lateral size of GST line corresponds to W_{GST}. This dimension is the same of the heater element that is in contact

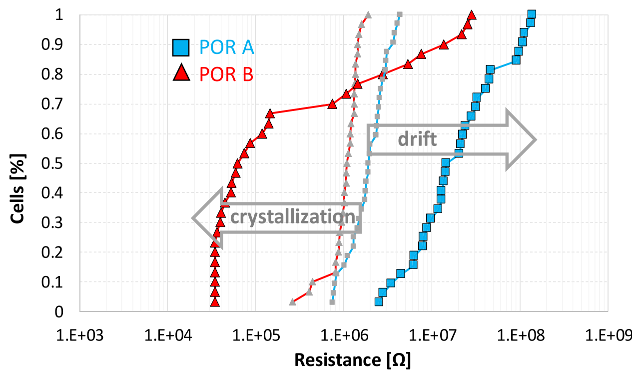


FIGURE 4. **Reset Retention experiment: POR A & POR B. 30 cells tested both for PORA and PORB. In gray color the pre-bake distributions. No evidence of crystallization (i.e., resistance lowering) on POR A (only drift observed).**

with the GST line. The increase of GST line width is a way to modify the dimension of the amorphous dome: if it is used same current density as the one adopted on the reference structure, we expect to obtain a semi-cylindrical region with longer dimension (greater W_{GST}) of amorphous material with the same radius (rough assumption).

Current density J is defined as I_{RESET} divided by Area=W_{GST} x (thickness of heater). The surface (Area) considered to define J is the interface region between GST (Width) directly in contact with the heater element; the other dimension that defines the surface (rectangular shaped) through which the current flows is in fact the thickness of the resistive element (see the sketch reported in Fig. 5b). In our experiments the thickness of heater element is always kept constant so the unique variable that modifies the area is the W_{GST}. To grant on $W_{GST\,2}$ same J as on $W_{GST\,1}$ it is only matter to adjust properly I_{RESET} such that $I_{RESET\,2} = I_{RESET\,1}$ x ($W_{GST\,2}/W_{GST\,1}$).

Our typical current density (reference case) ranges $1\mu A/nm^2$.

Fig. 6 shows two evolutions corresponding to Quenching time characterizations performed on reference target cell ($W_{GST} = W_0$) and on larger cell width ($W'_{GST} = W_0 \times 1.2$). The two geometries belong to the same process (POR A), but cells with narrower dimension exhibit an anticipated crystallization: the response of R_{READ} to the cooling time becomes slower (*faster*) when the volume increases (*reduces*).

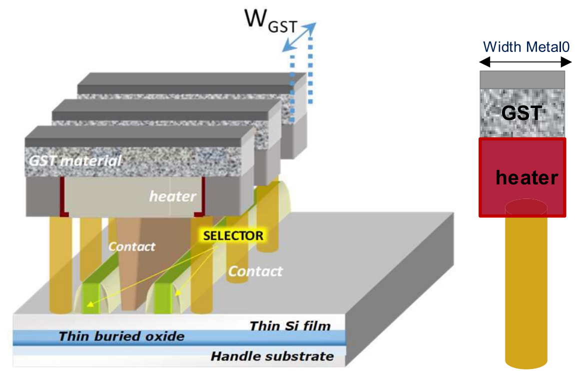
The re-crystallization observed in the Quenching time characterization is driven by the electrical signal applied. Only when the falling phase of the signal (trailing edge) is long enough, with respect to the considered system, it is observed a R_{READ} resistance lower than R_{RESET} (obtained with the very first pulse of the sequence, having a falling time close to zero (i.e., box shaped pulse)).

In our material the crystallization process is mainly due to nucleation and growth and does not occur from the edge of amorphous dome, so that we can imagine that it is required longer time to proper crystallize a larger volume.

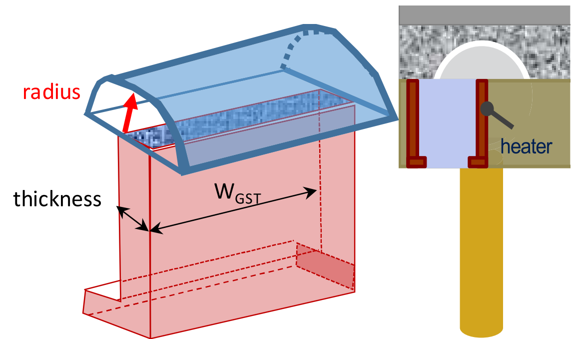
Similar results were also found on silicon with not optimized process (POR B) when W_{GST} dimension is varied: cells with narrower W_{GST} ($W''_{GST} = W_0 \times 0.8$) have an anticipated tendency toward crystalline state.

Note that in this second experiment (W_{GST}, W_{GST} x 0.8) both curves are shifted toward shorter times due to the effect of not optimized process (POR B) as already discussed (Fig. 3 of Section A).

Finally, quenching time figure of merit seems a good way to highlight differences in the volume of melted material.



(a)



(b)

FIGURE 5. **(a) 3D-array organization (left) and section along Width dimension (right). (b) Heater element with semi-cylindrical region of amorphous GST material (left). W_{GST} is the width of GST line (directly in contact with the heater) and of the heater element itself. Current flows through the rectangular Area defined by W_{GST} and thickness. For a given current density J, it is fixed the radius of the amorphous dome.**

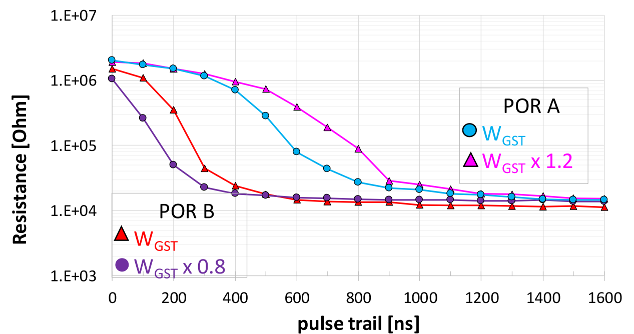


FIGURE 6. **R_{READ} median evolution: POR A & POR B, cells designed with different W_{GST} around typical: 1.2x wider and 0.8x narrower. Same current density J (~$1\mu A/nm^2$) granted by varying I_{RESET} to compensate W_{GST} differences.**

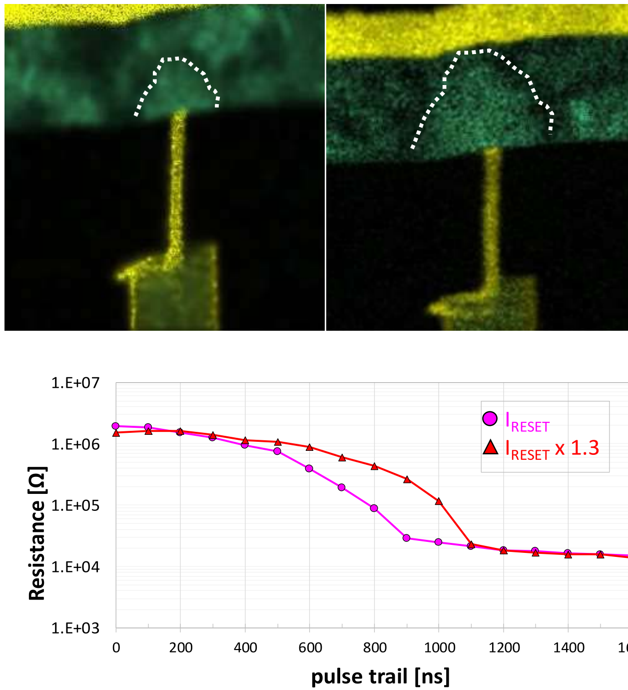


FIGURE 7. Sb-EDX spectra after Reset pulse at I_{RESET1} (top) and I_{RESET2} 1.3x (bottom). Plot shows corresponding R_{READ} median evolution: POR A, fixed geometry, different I_{RESET}.

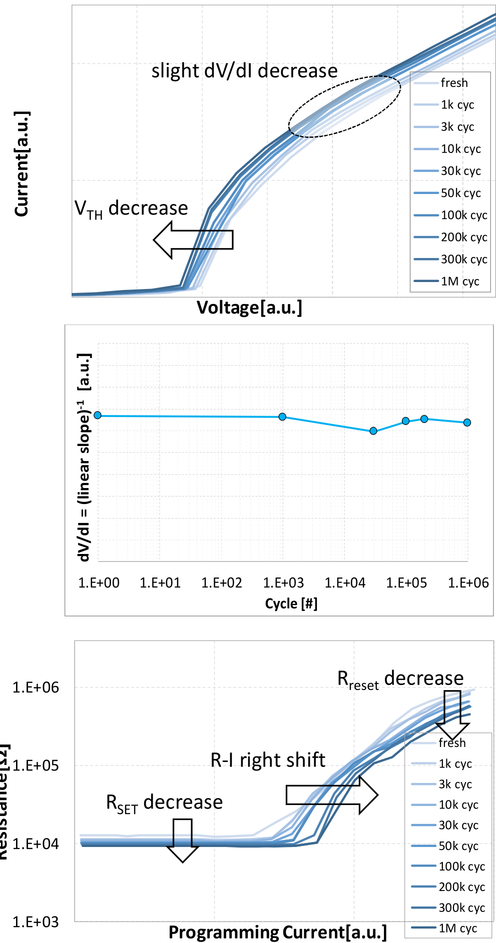


FIGURE 8. "I-V curves" (top) and "R-I programming curves" (bottom) at different cycles. Plot in the middle shows the slight reduction (~100-200ohm) of dV/dI slope.

C. IMPACT OF PROGRAMMING CURRENT

An alternative way to modulate the volume of melted material is to vary the programming current (I_{RESET}): the higher the I_{RESET} value, the more extended is the portion of melted material (i.e., the dome in the amorphous state). To support this statement, Fig. 7 shows two EDX pictures (Sb-spectra) of cells put in the Reset state with I_{RESET1} (left) and $I_{RESET2} = I_{RESET1} \times 1.3$ (right). The increased volume of activated material is pretty evident. Corresponding Quenching time characterization confirms that when the volume of melted material is greater (i.e., higher I_{RESET}) there is an increase of the quenching time needed to reach a well-defined crystalline state (close to 10kohm).

Values of Reset resistance greater than few Mohm are not so accurate in our Quenching-time characterization due to hardware constraints. Reliable Current reading covers 0.4μA – 0.4mA that in Resistance means 1Mohm – 1kohm). This can justify the light inconsistency in Fig. 7 in terms of electric read resistance at the beginning of the characterization (pulse trail = 0÷200 ns) with resistances values higher with I_{RESET2} than I_{RESET1}.

The role of "electrical activation" has been already discussed in [7]: "forming" operation, related to the maximum current flowed into the cell at very first programming operation, is able to create a Sb-rich region: the higher the forming current the wider the Sb-rich region corresponding to the activated region. In our experiments $I_{FORMING} = I_{RESET}$ and so higher I_{RESET} (1.3x) means also higher $I_{FORMING}$ and correspondingly wider activated region (see Fig. 7- EDX picture).

Plot reported in Fig. 7 shows a delay when current is increased (1.3x): Sb-enrichment is present but also a volume increase; we propose that delay is driven by volume increase similarly to what observed modifying only the geometrical dimension (see Section B, Fig. 6).

D. IMPACT OF ENDURANCE

The effects of cycling on Phase Change Memory Cells have been widely studied with the objective to understand the impact of repeated Set and Reset operations on cell performances.

Electrical parameters, on which the final application relies, are the result of physical, thermal, chemical and microscopic characteristics of PCM cell, all of them modulated by extended Set and Reset operations [8], [9], [10].

Usual measurements performed to assess cell behavior across cycling consist of full data collection after predefined numbers of Set/Reset operations. In our case every cycle is performed by applying fixed Set and Reset pulses, both in terms of max current and timing. Fig. 8 collect typical figures of merit up to 1Mcycles. Results here obtained show

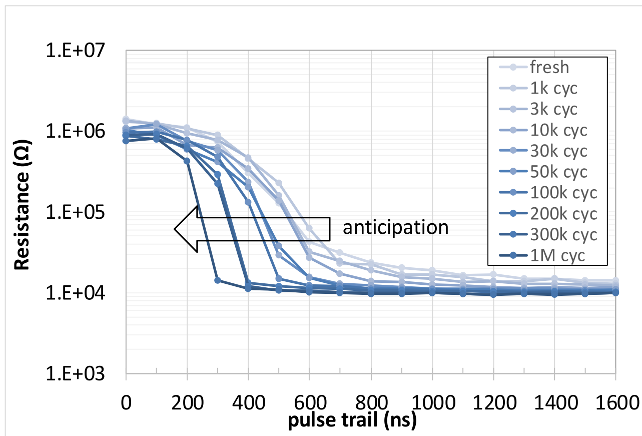


FIGURE 9. R_{READ} median evolution for cells of POR A ("optimized") after different number of Set/Reset cycles.

the expected behaviors with the number of cycles, as already reported by others [11]:

- slight reduction (~100-200ohm) of dV/dI slope at enough high voltage (linked to R_{HEATER} decrease = ageing)
- decrease of lowest resistance in the R-I plot (R_{SET} at fixed Set pulse)
- Set-to-Reset edge of R-I curves shift to higher currents
- decrease of highest resistance in the R-I plot (R_{RESET} at fixed Reset pulse)
- decrease of V_{TH} (threshold switch)

Changes in GST material (moving to more Sb-rich composition in the active region) have been already considered at the origin of these parameters evolution, in particular for what concerns large part of R_{SET} decrease [12], [13].

In addition we propose to correlate the decrease of R_{RESET} to a slight dimensional reduction of the amorphous dome: aged cell, when treated with fixed programming pulse, it is less efficient to melt and amorphize the same volume of material of a not-cycled device.

TEM and EDX pictures have been collected on PCM cells preconditioned at different number of cycles; they show a reduction of the amorphous dome (obtained with fixed reset pulse) when the number of cycles increases. For this reason we propose to correlate the decrease of R_{RESET} not only to slight GST-alloy changes, as already mentioned in [12] and [13], but also to a dimensional reduction of amorphous dome.

In a real product, anyway, these ageing effects can be addressed by proper programming algorithms. Algorithm embedded in the product applies a conventional Program and Verify sequence (up to a predefined max number of pulses) to recover the portion of population not properly programmed at previous steps.

Effects of endurance test have been also studied in terms of quenching time characterization by launching this kind of assessment at every readout point. Results are reported in Fig. 9 and clearly evidence an anticipated crystallization: the higher the number of cycles considered and the shorter is the falling time of the pulse required to reach a significant crystallization.

This result is well consistent with the consideration about dimensional reduction of amorphous dome with the increase of cycles.

IV. CONCLUSION

Quenching time characterization is proposed as a method to get insight on the local chemical-physical properties of chalcogenide in a Phase Change Memory cell.

Quenching time figure of merit clearly responds to alloy modifications (as consequence for example of not optimized integration) and/or dimensional variations of active material.

It can be adopted not only as a simple way to electrically compare GST-alloy properties as a function of material composition but also to understand in a more solid way results coming from complementary tests like Data Retention and Endurance.

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Authors' photographs and biographies not available at the time of publication.