Received 22 February 2019; revised 8 April 2019; accepted 14 April 2019. Date of publication 22 April 2019; date of current version 3 May 2019. The review of this paper was arranged by Editor C.-M. Zetterling.

Digital Object Identifier 10.1109/JEDS.2019.2912186

# Effect of Al<sub>2</sub>O<sub>3</sub> Passivation on Electrical Properties of $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Field-Effect Transistor

# JIYEON MA<sup>®</sup><sup>1</sup>, OUKJAE LEE<sup>2</sup>, AND GEONWOOK YOO<sup>®</sup><sup>1</sup>

1 School of Electronic Engineering, Soongsil University, Seoul 06938, South Korea 2 Center for Spintronics, Korea Institute of Science and Technology, Seoul 02792, South Korea

CORRESPONDING AUTHOR: G. YOO (e-mail: gwyoo@ssu.ac.kr)

This work was supported by the Korea Institute for Advancement of Technology under the Competency Development Program for Industry Specialists of the Korean Ministry of Trade, Industry and Energy (HRD Program for Software-SoC Convergence) under Grant N0001883.

**ABSTRACT** We report on the effect of Al<sub>2</sub>O<sub>3</sub> surface passivation on electrical properties of beta-gallium oxide ( $\beta$ -Ga<sub>2</sub>O<sub>3</sub>) nanomembrane field-effect transistor (FET). The fabricated bottom-gate  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>(100) FET exhibits enhanced channel conductance and reduced hysteresis after the conformal atomic layer deposited Al<sub>2</sub>O<sub>3</sub> passivation investigated by high-resolution transmission electron microscope (HR-TEM) analysis. Moreover, abnormal positive threshold voltage ( $V_{TH}$ ) shifts under negative bias stress are turned into negative  $V_{TH}$  shifts, and off-state breakdown characteristics is improved as well. A modeling work using physics-based TCAD shows reduced surface depletion effect after the surface passivation. The results demonstrate that high-quality ALD-Al<sub>2</sub>O<sub>3</sub> surface passivation is an effective method to improve electrical properties of the bottom-gate  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET and its device applications.

**INDEX TERMS**  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, passivation, surface depletion.

### I. INTRODUCTION

Beta-gallium oxide ( $\beta$ -Ga<sub>2</sub>O<sub>3</sub>) has attracted great attention very recently as a promising candidate for next generation high power device application due to its superior electrical properties. Its wide bandgap is about 4.6  $\sim$  4.9 eV, allowing high-temperature and high-voltage operation estimated to be a breakdown field ( $E_{br}$ ) of up to 8 MV/cm [1]–[3]. Consequently, even with nominal electron mobility of 100 cm<sup>2</sup>/Vs at room temperature,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is estimated to possess several times higher Baliga's figure-of-merit (FOM) than that of current viable solutions such as silicon carbide (SiC) and gallium nitride (GaN) [3], [4]. The highest measured mobility is so far reported to be  $\sim 180 \text{ cm}^2/\text{Vs}$  [5], and its theoretical limit in a bulk crystal is estimated below 200 cm<sup>2</sup>/Vs at 300 K [6]. Furthermore, a high-quality native Ga<sub>2</sub>O<sub>3</sub> substrate from bulk single crystal obtained from melt-growth methods, such as Czochralski and edge-defined film-fed growth (EFG), provide a competitive cost over other competing wide bandgap materials [7]–[10].

In order to take advantage of the superior FOMs and fabricate high performance devices for various applications, a high-quality interface with  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is of primary concern since it generally affects field-effect mobility, stress instability, breakdown characteristics, etc. Thus, several improvement methods have been reported using high-k oxides as a gate-dielectric layer and even heterostructures [5], [11]–[13]. Furthermore, surface depletion effect on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is reported to affect threshold voltage as well as bias-stress stability in a bottom-gate configuration, and so dielectric passivation is suggested [14]–[17]. From a practical point of view, the stress induced instability issue associated with high surface states requires a proper passivation scheme to be incorporated.

In this work, we investigate the effect of atomic layer deposited (ALD) aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) surface passivation on electrical properties of bottom-gate  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>(100) FET. The  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanomembrane is obtained from an unintentionally n-doped (UID) bulk crystal using a mechanical exfoliation method. Electrical properties of the fabricated bottom-gate  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>(100) FET are extracted and compared before and after the Al<sub>2</sub>O<sub>3</sub> surface passivation. Highresolution transmission electron microscope (HR-TEM) analysis is carried out to investigate the Al<sub>2</sub>O<sub>3</sub>/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> interface. Moreover, negative bias stress instability as well as off-state breakdown characteristics are also studied and compared. Finally, detailed analysis using energy band model



**FIGURE 1.** (a) A representative SEM image of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET (*W/L* = 4.5  $\mu$ m/5.6  $\mu$ m) with bottom gate configuration using a mechanical exfoliation method (Inset) Its cross-sectional schematic illustration. (b) Cross-sectional HR-TEM image of the exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channel (Inset) Its corresponding electron diffraction pattern with the unit of 5 1/nm indicating 5 reserved nanometers, confirming the (100) surface orientation of the exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanomembrane.

and TCAD simulations has been conducted to discuss the effect of  $ALD-Al_2O_3$  surface passivation.

## **II. EXPERIMENTS**

Based on a conventional scotch-tape method,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flakes were mechanically exfoliated from a (-201) surface  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> bulk substrate (15 mm x 10 mm) with unintentional n-type doping (UID) concentration of 4.8 x  $10^{17}$  cm<sup>-3</sup>, and then transferred onto  $SiO_2/p^{++}Si$  (300nm/500µm) substrate. The heavily doped  $p^{++}$  Si substrate is used as a bottom gate. The sample was immediately cleaned in Acetone and IPA. Then source and drain (S/D) electrodes of Ti/Au (20/120 nm) were deposited by thermal evaporation and patterned using a conventional photolithography and lift-off process. Post-deposition anneal process was not performed. After that, the other side (top surface) of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flakes was passivated with about 20 nm thick Al<sub>2</sub>O<sub>3</sub> layer deposited by ALD at 200 °C. Trimethyl Aluminum (TMA) and water as Al precursor and oxygen source, respectively. Finally, source/drain (S/D) contacts were open via reactive-ion etching (RIE) using CF<sub>4</sub>/O<sub>2</sub> gases (150 W). Focused ionbeam (FIB)-scanning electron microscopy (SEM, Nova 600) and high resolution transmission electron microscopy (HR-TEM, Talos F200X) equipped with an energy-dispersive X-ray spectrometer (EDX) was used. Electrical characterization was carried out using Keithley 4200A semiconductor parameter analyzer in ambient conditions. The commercial Silvaco Atlas is employed for TCAD simulation.

#### **III. RESULTS AND DISCUSSION**

Fig. 1(a) shows a representative scanning electron microscopy (SEM) image of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanomembrane FET with its cross-sectional schematic illustration in the inset. The monoclinic structure of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, having a relatively large lattice constant along the [100] direction, allows a simple cleavage into flakes or nanomembranes similar to two-dimensional layered materials [14]–[19]. Fig. 1(b) shows a cross-sectional HR-TEM



**FIGURE 2.** (a) Transfer curves  $(I_{DS}-V_{GS})$  by double-sweep for  $V_{DS} = 1$  V before and after ALD-Al<sub>2</sub>O<sub>3</sub> passivation. Transconductance  $(g_m)$  vs.  $V_{GS}$  for the same  $V_{DS}$  is shown. (b) Output characteristics  $(I_{DS}-V_{DS})$  for  $V_{GS} = -30, -20, -10$ , and 0 V before and after the passivation (Inset)  $I_{DS}-V_{DS}$  of the device for low  $V_{DS}$  regime of  $0 \sim 1.0$  V before and after passivation.

image of the exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> preserving high crystal quality of bulk  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystal with no damage or strain, and its selected-area electron diffraction (SAED) pattern shown in the inset of Fig. 1(b) confirms the lattice parameters and directions of the exfoliated flake. A clean and facile cleavage along the [100] direction is achieved, and so the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> with (100) surface orientation forms the channel. Although the approach is not scalable, it allows a simple device fabrication to investigate electrical material properties of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> with the specific surface orientation.

Fig. 2(a) shows measured transfer curves of  $I_{DS}$ - $V_{GS}$ for  $V_{\rm DS} = 1$  V before and after the Al<sub>2</sub>O<sub>3</sub> passivation by double-sweep method applying  $V_{\rm GS}$  from -100 V to 0 V (forward sweep) and then back to -100 V (backward sweep). The characterized device has a channel width (W)/length (L) of 2  $\mu$ m/16  $\mu$ m with channel thickness of about 260 nm. The peak transconductance  $(g_m)$ , which is calculated from  $g_{\rm m} = dI_{\rm DS}/dV_{\rm GS}$ , increases from 0.10 to 0.13 mS/mm, and the subthreshold slope (SS) calculated from  $SS = [d(\log_{10} I_{\rm DS})/dV_{\rm GS}]^{-1}$  improves from 0.30 to 0.25 V/dec. The relatively low  $g_m$  compared with the values from other groups can be associated with a low doping concentration of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and un-optimized S/D metal contact process. Through successful elimination of water and oxygen molecules at the channel surface, a negligible hysteresis  $(\Delta V)$  is observed after the passivation in comparison with an initial hysteresis of 2.6 V. A negative  $V_{\text{TH}}$  shift of -8.3 V (from -28.2 V to -36.5 V) is due to positively fixed charges inside the Al<sub>2</sub>O<sub>3</sub> layer inducing further electrons into the channel (i.e., n-doping effect) and/or suppressed surface depletion effects around the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flake. Fig. 2(b) compares measured output curves of IDS-VDS for VGS = (term missing) (set as ms) -30, -20, -10, and 0 V, and the inset shows ohmic-like contact behaviors of both before and after the passivation in low  $V_{\text{DS}}$  regions.

The interface of ALD-Al<sub>2</sub>O<sub>3</sub>/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub>(100) is investigated by HR-TEM analysis. Fig. 3(a) shows the STEM image, and Fig. 3(b) and (c) show EDX mapping of different layers, confirming the elements of layers. Platinum(Pt) particles on top of the Al<sub>2</sub>O<sub>3</sub> layer are due to the Pt coating process during sample preparation for TEM. Fig. 3(d) shows a cross-sectional HR-TEM image of the interface with red dashed box, confirming a uniform amorphous Al<sub>2</sub>O<sub>3</sub> layer with a few nm thick conformal Al<sub>2</sub>O<sub>3</sub> interlayer in a different phase on the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> surface. After being crystallized at the initial stage of ALD deposition attributed to atomic arrangement similarities between the Al<sub>2</sub>O<sub>3</sub> and  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> [20], the conformal Al<sub>2</sub>O<sub>3</sub> layer successfully passivates dangling bonds and surface states on the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> surface, consequently improving the overall device performance.



**FIGURE 3.** (a) HAADF-STEM image of the Al<sub>2</sub>O<sub>3</sub>/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> structure (yellow dashed lines for eye guidance) and (b) its EDX compositional mapping of the different layers; element (c) Al. (d) A cross sectional HR-TEM image with an indication (red dashed box) of conformal Al<sub>2</sub>O<sub>3</sub> layer at the interface Al<sub>2</sub>O<sub>3</sub>/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub>(100).

Furthermore, the Al<sub>2</sub>O<sub>3</sub> surface passivation improves biasstress stability. In order to investigate electrical instability of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET, we performed transfer characteristics measurements under negative bias stress (NBS,  $V_{\text{GS}} - V_{\text{TH}} < 0$ ) during the given stress time (10,000 sec). We only interrupted the applied stress for the measurement at predetermined steps by sweeping  $V_{\text{GS}}$  from -100 V to 0 V at  $V_{\text{DS}} = 1$  V, and extracted  $\Delta V_{\text{TH}}$  from  $\Delta V_{\text{TH}} = V_{\text{TH}}$ (t = t<sub>STR</sub>) -  $V_{\text{TH}}$  (t=0). Fig. 4(a) shows the change of

514

extracted  $\Delta V_{\text{TH}}$  as a function of stress time for the asfabricated (i.e., unpassivated) and Al<sub>2</sub>O<sub>3</sub>-passivated device (i.e., ALD-Al<sub>2</sub>O<sub>3</sub>). Abnormal positive  $\Delta V_{\text{TH}}$  of ~37 V observed in the unpassivated device is turned into negative  $\Delta V_{\text{TH}}$  of about -12 V in the Al<sub>2</sub>O<sub>3</sub>-passivated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET, which is a typical shift behavior under NBS.



**FIGURE 4.** (a) Threshold voltage shifts ( $\Delta V_{TH}$ ) of the unpassivated (i.e., as-fabricated) and Al<sub>2</sub>O<sub>3</sub>-passivated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>(100) FET as a function of stress time (t<sub>STR</sub>, 10,000 sec) under negative bias stress ( $V_{GS} - V_{TH} < 0$  V) measured at  $V_{DS} = 1$  V. (Inset)  $\Delta V_{TH}$  in logarithmic scale of stress time. (b) Three terminal off-state breakdown measurement of the unpassivated and Al<sub>2</sub>O<sub>3</sub>-passivated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET.

In addition, we performed three-terminal off-state breakdown measurement in order to evaluate the passivation effect on breakdown characteristics. Same effective gatebias ( $V_{\rm GS} - V_{\rm TH}$ ) was applied to maintain off-state, and  $V_{\rm DS}$ was swept until destructive breakdown happened by reaching a preset compliance current value. Although the abrupt increase in  $I_{\rm OFF}$  at  $V_{\rm DS} = 25$  V is unclear, a breakdown voltage (BV) of 123 V is observed for the unpassivated device as shown in Fig. 4(b). However, no destructive BV is measured in the sweep range after the passivation because the Al<sub>2</sub>O<sub>3</sub> layer has not only reduced dangling bonds and defects on the surface leading to a reduced current collapse effect and but also provided smoother field distribution in the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channel [26]. The drain current fluctuation for  $V_{\rm DS} > 160$  V can be attributed to traps-to-band tunneling current and charging/discharging of the traps. Further optimization of the ALD surface passivation on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>(100) is suggested

In order to validate the experimental results, TCAD simulations are carried out [21]. Firstly, TCAD parameters are calibrated to the measured I-V characteristics before and after the passivation. We further incorporate Shockley-Read-Hall, Fermi-Dirac statistics, and Auger recombination models, and added a parameter (INTTRAP) in order to set shallow and deep trap levels taken from other groups' DLTS and DLOS analysis, respectively [22], [23]. Fig. 5(a) shows electric-field (E Field) distributions of fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET in the on-state before and after the Al<sub>2</sub>O<sub>3</sub> passivation, indicating reduced peak electric field at the drain edge and an even field distribution along the channel. Electron current (e-current) densities of the device are also present in Fig. 5(b). It is clearly shown that the depleted width at the channel surface is reduced after the passivation and the passivated device has more conducting carriers under the same gate bias. The reduced surface depletion effect is discussed in detail using energy band diagrams hereinafter.





Fig. 6 illustrates the surface depletion effect by surface defect states (accept-like) which is larger than the amount of released-charges (i.e., electrons) from the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> interface states (donor-like) under NBS condition [15], [16], [24], [25]. Depleted charges from the channel surface exceed released charges into the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channel because of conceivable surface oxygen vacancies, defect states, and adsorbates. After the Al<sub>2</sub>O<sub>3</sub> passivation, however, the negative  $\Delta V_{\text{TH}}$  of about -12 V, which is a typical shift behavior under NBS, was achieved. As validated by the simulation, the surface depletion width was decreased and so surface depletion effect was suppressed by the Al<sub>2</sub>O<sub>3</sub> passivation.



**FIGURE 6.** Schematic illustration of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>(100) surface states before and after ALD-Al<sub>2</sub>O<sub>3</sub> passivation.

#### **IV. CONCLUSION**

In conclusion, we have investigated the effect of ALD-Al<sub>2</sub>O<sub>3</sub> surface passivation on electrical properties and device instability of the bottom gate  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>(100) FET;  $g_{\rm m}$  increases from 0.1 to 0.13 mS/mm, SS is reduced from 0.30 to 0.25 V/dec, and a negligible hysteresis ( $\Delta V$ ) is achieved in comparison with the initial hysteresis of 2.6 V. HR-TEM and EDX analysis confirm that a conformal Al<sub>2</sub>O<sub>3</sub> layer has been deposited on the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>(100) surface, resulting in successful reduction of surface states and adsorbates at the channel surface. Consequently, abnormal positive  $\Delta V_{\rm TH}$ under NBS due to the predominant surface depletion effect is altered into conventional negative  $\Delta V_{\rm TH}$ , and an increased BV is obtained in three-terminal off-state breakdown measurement. Further improvements in both device performance and stability are expected with ALD process optimization, and therefore the high-quality ALD-Al<sub>2</sub>O<sub>3</sub> passivation is proposed to achieve high performance  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET.

#### REFERENCES

- M. Higashiwaki *et al.*, "Recent progress in Ga<sub>2</sub>O<sub>3</sub> power devices," *Semicond. Sci. Technol.*, vol. 31, no. 3, pp. 1–11, Jan. 2016. doi: 10.1088/0268-1242/31/3/034001.
- [2] S. J. Pearton *et al.*, "A review of Ga<sub>2</sub>O<sub>3</sub> materials, processing, and devices," *Appl. Phys. Rev.*, vol. 5, no. 1, pp. 1–55, Jan. 2018. doi: 10.1063/1.5006941.
- [3] M. Higashiwaki and G. H. Jessen, "Guest Editorial: The dawn of gallium oxide microelectronics," *Appl. Phys. Lett.*, vol. 112, no. 6, pp. 1–5, Feb. 2018. doi: 10.1063/1.5017845.
- [4] B. J. Baliga, "Semiconductors for high-voltage, vertical channel fieldeffect transistors," J. Appl. Phys., vol. 53, no. 3, pp. 1759–1764, Mar. 1982. doi: 10.1063/1.331646.
- [5] Y. Zhang *et al.*, "Demonstration of high mobility and quantum transport in modulation-doped β-(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub>/Ga<sub>2</sub>O<sub>3</sub> heterostructures," *Appl. Phys. Lett.*, vol. 112, no. 17, pp. 1–5, Apr. 2018. doi: 10.1063/1.5025704.
- [6] N. Ma *et al.*, "Intrinsic electron mobility limits in β-Ga<sub>2</sub>O<sub>3</sub>," *Appl. Phys. Lett.*, vol. 109, no. 21, pp. 1–5, Nov. 2016. doi: 10.1063/1.4968550.
- [7] Y. Tomm, P. Reiche, D. Klimm, and T. Fukuda, "Czochralski grown Ga<sub>2</sub>O<sub>3</sub> crystals," *J. Cryst. Growth*, vol. 220, no. 4, pp. 510–514, Dec. 2000. doi: 10.1016/S0022-0248(00)00851-4.

- [8] Z. Galazka *et al.*, "Scaling-up of bulk β-Ga<sub>2</sub>O<sub>3</sub> single crystals by the Czochralski method," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 2, pp. Q3007–Q3011, Jan. 2017. doi: 10.1149/2.0021702jss.
- [9] A. Kuramata *et al.*, "High-quality β-Ga<sub>2</sub>O<sub>3</sub> single crystals grown by edge-defined film-fed growth," *Jpn. J. Appl. Phys.*, vol. 55, no. 12, pp. 1–6, Nov. 2016. doi: 10.7567/JJAP.55.1202A2.
- [10] H. Aida *et al.*, "Growth of β-Ga<sub>2</sub>O<sub>3</sub> single crystals by the edgedefined, film fed growth method," *Jpn. J. Appl. Phys.*, vol. 47, no. 11R, pp. 8506–8509, Nov. 2008. doi: 10.1143/JJAP.47.8506.
- [11] H. Zhou, S. Alghmadi, M. Si, G. Qiu, and P. D. Ye, "Al<sub>2</sub>O<sub>3</sub>/β-Ga<sub>2</sub>O<sub>3</sub> (-201) interface improvement through piranha pretreatment and postdeposition annealing," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1411–1414, Nov. 2016. doi: 10.1109/LED.2016.2609202.
- [12] M. A. Bhuiyan *et al.*, "Charge trapping in Al<sub>2</sub>O<sub>3</sub>/β-Ga<sub>2</sub>O<sub>3</sub>-based MOS capacitors," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1022–1025, Jul. 2018. doi: 10.1109/LED.2018.2841899.
- [13] A. Jayawardena, R. P. Ramamurthy, A. C. Ahyi, D. Morisette, and S. Dhar, "Interface trapping in (-201) β-Ga<sub>2</sub>O<sub>3</sub>MOS capacitors with deposited dielectrics," *Appl. Phys. Lett.*, vol. 112, no. 19, pp. 1–5, May 2018. doi: 10.1063/1.5019270.
- [14] H. Zhou *et al.*, "High-performance depletion/enhancement-ode β-Ga<sub>2</sub>O<sub>3</sub> on insulator (GOOI) field-effect transistors with record drain currents of 600/450 mA/mm," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 103–106, Jan. 2017. doi: 10.1109/LED.2016.2635579.
- [15] H. Zhou, K. Maize, G. Qiu, A. Shakouri, and P. D. Ye, "β-Ga<sub>2</sub>O<sub>3</sub> on insulator field-effect transistors with drain currents exceeding 1.5 A/mm and their self-heating effect," *Appl. Phys. Lett.*, vol. 111, no. 9, pp. 1–4, Aug. 2017. doi: 10.1063/1.5000735.
- [16] J. Ma, O. Lee, and G. Yoo, "Abnormal bias-temperature stress and thermal instability of β-Ga<sub>2</sub>O<sub>3</sub> nanomembrane field-effect transistor," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1124–1128, Sep. 2018. doi: 10.1109/JEDS.2018.2868905.
- [17] A. Y. Polyakov *et al.*, "Defect states determining dynamic trappingdetrapping in β-Ga<sub>2</sub>O<sub>3</sub> field-effect transistors," *ECS J. Solid State Sci. Technol.*, vol. 8 no. 7, pp. Q3013–Q3018, Jan. 2019. doi: 10.1149/2.0031907jss.
- [18] W. S. Hwang *et al.*, "High-voltage field effect transistors with widebandgap β-Ga<sub>2</sub>O<sub>3</sub> nanomembranes," *Appl. Phys. Lett.*, vol. 104, no. 20, pp. 1–5, May 2014. doi: 10.1063/1.4879800.
- [19] J. Kim, S. Oh, M. A. Mastro, and J. Kim, "Exfoliated β-Ga<sub>2</sub>O<sub>3</sub> nano-belt field-effect transistors for air-stable high power and high temperature electronics," *Phys. Chem. Chem. Phys.*, vol. 18, no. 23, pp. 15760–15764, Jun. 2016. doi: 10.1039/C6CP01987K.
- [20] T. Kamimura, D. Krishnamurthy, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Epitaxially grown crystalline Al<sub>2</sub>O<sub>3</sub> interlayer on β-Ga<sub>2</sub>O<sub>3</sub> (010) and its suppressed interface state density," *Jpn. J. Appl. Phys.*, vol. 55, no. 12, pp. 1–7, Oct. 2016. doi: 10.7567/JJAP.55.1202B5.
- [21] ATLAS SILVACO, Simulation Standard 23, Jul. 2013.
- [22] K. Irmscher, Z. Galazka, M. Pietsch, R. Uecker, and R. Fornari, "Electrical properties of β-Ga<sub>2</sub>O<sub>3</sub> single crystals grown by the Czochralski method," J. Appl. Phys., vol. 110, no. 6, pp. 1–7, Aug. 2011. doi: 10.1063/1.3642962.
- [23] Z. Zhang, E. Farzana, A. R. Arehart, and S. A. Ringel, "Deep level defects throughout the bandgap of (010) β-Ga<sub>2</sub>O<sub>3</sub> detected by optically and thermally stimulated defect spectroscopy," *Appl. Phys. Lett.*, vol. 108, no. 5, pp. 1–5, Feb. 2016. doi: 10.1063/1.4941429.
- [24] K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, "Origins of threshold voltage shifts in room-temperature deposited and annealed a-In–Ga–Zn–O thin-film transistors," *Appl. Phys. Lett.*, vol. 95, no. 1, pp. 1–3, Jul. 2009. doi: 10.1063/1.3159831.

- [25] E. N. Cho, J. H. Kang, C. E. Kim, P. Moon, and I. Yun, "Analysis of bias stress instability in amorphous InGaZnO thin-film transistors," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 1, pp. 112–117, Mar. 2011. doi: 10.1109/TDMR.2010.2096508.
- [26] Y. Ohno, T. Nakao, S. Kishimoto, K. Maezawa, and T. Mizutani, "Effects of surface passivation on breakdown of AlGaN/GaN highelectron-mobility transistors," *Appl. Phys. Lett.*, vol. 84, no. 12, pp. 2184–2186, Mar. 2004. doi: 10.1063/1.1687983.



**JIYEON MA** received the B.S. degree in electronic engineering from Soongsil University, Seoul, South Korea, in 2018, where he is currently pursuing the M.S. degree. His current research focuses on gallium oxide-based devices and fabrication.



**OUKJAE LEE** received the B.S. degree in physics and mathematics from Seoul National University in 2004 and the Ph.D. degree in applied physics from Cornell University in 2012. He is a Senior Research Scientist with the Korea Institute of Science and Technology, Seoul, South Korea. He was a Post-Doctoral Scholar of electrical engineering with the University of California, Berkeley from 2013 to 2015. His research interest is nonvolatile magnetic memory (MRAM) and experimental spintronics, where he has studied magnetic

excitations of nanoscale magnets via current induced spin-transfer-torque or spin-orbit-torque.



**GEONWOOK YOO** received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2005, the M.Eng. degree in biomedical engineering from Cornell University and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 2011. He was a Senior Engineer with Samsung Electronics from 2010 to 2014 and a Senior Researcher with Korea Electronics Technology Institute from 2014 to 2016. In 2016, he then joined Soongsil University, Seoul, as an Assistant

Professor with the School of Electronic Engineering. His research interests include low-dimensional and wide bandgap semiconductor materials and devices.