Received 24 January 2019; revised 11 February 2019; accepted 27 March 2019. Date of publication 3 April 2019; date of current version 19 April 2019.
The review of this paper was arranged by Editor T.-L. Ren.

Digital Object Identifier 10.1109/JEDS.2019.2908255

Impacts of HfO_2/ZnO Stack-Structured Charge-Trap Layers Controlled by Atomic Layer Deposition on Nonvolatile Memory Characteristics of In-Ga-Zn-O Channel Charge-Trap Memory Thin-Film Transistors

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This work was supported in part by the National Research Foundation of Korea grant funded by the Korean Government (MEST, Nonvolatile Memory Transistors Using Binary Ferroelectric Metal Oxides Thin Films) under Grant NRF-2017R1A2B4007492, in part by the Electronics and Telecommunications Research Institute grant funded by the Korean Government (Development of Neuromorphic Hardware by Using High Performance Memristor Device Based on Ultra-Thin Film Structure) under Grant 18ZB1800, and in part by the Kyung Hee University–Samsung Electronics Research and Development Program entitled "Flexible Flash Memory Device Technologies for Next-Gen Consumer Electronics."

ABSTRACT We fabricated the charge-trap memory thin film transistors (CTM-TFTs) using InGaZnO (IGZO) active channel and HfO_2/ZnO stack-structured charge-trap layer (CTL). To investigate the effects of the number and thickness of HfO_2 layers inserted between the ZnO within the stack structured CTLs on the device characteristics, 2-nm-thick HfO_2 thin films were inlaid once, twice, and four times, and 4-nm-thick HfO_2 layers were introduced twice between the ZnO layers. The CTM-TFTs using the stack structured CTLs with 4-nm-thick HfO_2 layers showed good memory characteristics, including large memory window (MW) of 25 V and rapid program/erase (P/E) speed of 500 μs because of high total trap density of HfO_2 with a sufficient thickness to provide charge-trap centers. On the contrary, relatively narrow MW of 16 V and slower P/E speed of 100 ms were obtained for memory device using the stacked CTL with four HfO_2 layers of 2 nm. The HfO_2 layer with a thickness as thin as 2 nm was supposed to act as just dielectric films deactivating the trapping or migration of electron charges due to too thin film thickness. The gate-stack structures confirmed from STEM images suggested that the modulations in memory device characteristics with different CTL structures resulted from the variations in designs of stack structured CTLs when the interface qualities within the gate-stacks were well prepared. Moreover, the detailed fabrication conditions were found to be important control parameters to reproducibly obtain reliable memory device characteristics.

INDEX TERMS High-k material, HfO_2, ZnO, ALD, IGZO charge-trap memory.

I. INTRODUCTION

Charge-trap memory thin-film transistors (CTM-TFTs) utilizing oxide semiconductor channels like an amorphous In-Ga-Zn-O (a-IGZO) have attracted much attentions for novel electronic devices. Thanks to lots of advantages such as low-temperature process compatibility and optical transparency, they can be utilized for various applications such as flexible and transparent electronic systems. [1]–[4] However, to realize more advanced nonvolatile memory devices for next-generation consumer electronic applications, the wide memory window (MW), fast program/erase (P/E) speed, and long retention time should be simultaneously guaranteed with a lower-power consumption. On the contrary, it is difficult to obtain a fast P/E speed, low voltage operation, and a long retention time at the same time because of their trade-off relationship. The tunneling oxide thickness can be reduced for achieving fast P/E speed and low voltage operation, which can enhance the program efficiency due to a higher electric

field applied across the gate-stack. However, the leakage current increases and hence the retention property is degraded. Alternatively, when the tunneling layer thickness increases, the retention time will be elongated due to reduced leakage component but the longer and higher voltage signals are required for the P/E operations.

The charge-trap layer (CTL) plays important roles in the oxide semiconductor CTM-TFTs. The CTL determines overall memory performances related to the efficiency of charge trap/detrap events. Various CTL materials have been investigated to improve the memory characteristics, such as metal nanoparticle, rare-earth oxide film, and oxide semiconductor [5]–[8]. Among them, the oxide semiconductor can be utilized for the CTL due to thier unique band structure. The IGZO, which is widely used as a channel material for the oxide semiconductor TFTs, was also used as a CTL by controlling the deposition conditions and the program capability with the V_{TH} shift wider than 3.8 V was obtained with a 10-ms program pulse. However, the device properties including long program time and long-term reliabilities needed to be improved [9]. The ZnO was also chosen as one of the oxide semiconductor CTLs considering its intrinsic defects of shallow and deep level states. According to prior researches on the ZnO CTLs, [10] the memory device showed the V_{TH} shift of 2.35 V when the gate voltage was swept from −25 to 25 V for P/E operations. Previously, the CTM-TFTs were successfully demonstrated to exhibit sound memory characteristics on plastic PEN substrates as well as rigid glass substrates [11]–[12]. Therefore, the oxide semiconductor, especially ZnO, is a potential CTL candidate for the oxide CTM TFTs. However, it has been a hard task to obtain faster P/E speed, low voltage operation and longer retention time at the same time when the ZnO CTL has been employed.

From these technical backgrounds, it will be useful to consult from the typical examples developed in Si-based charge-trap flash (CTF) memories, in which specified materials composing the gate-stack structure including charge-trap, tunneling, and blocking oxide layers have been replaced. Especially, the Si_3N_4, that has been commonly used as a CTL for the CTFs, can be substituted with high-k dielectrics. Furthermore, the multi-stack-structured CTLs using high-k materials have been recently introduced. High-k dielectrics can also be promising candidates for CTLs for oxide CTM-TFTs because of their several advantages such as high dielectric constant as well as high trap density and high charge-trap efficiency due to their intrinsic defects. Furthermore, the improvements in P/E speed and retention time have been reported by introducing the high-k CTLs. There have been numerous works introducing the high-k CTLs such as Al_2O_3, Ta_2O_5, ZrO_2, and HfO_2 and their multi-stack structures in Si-based CTFs [13]–[18]. Among them, a HfO_2 has been widely employed as a CTL because of its wide band gap (∼5.7 eV), high dielectric constant (∼25), and charge-storage capability even at a low voltage [19]–[20]. The memory devices employing the HfO_2 CTL showed a low leakage current density and superior device performance compared with those using the Si_3N_4 CTL [21]. Thus, the introduction of high-k HfO_2 layers between the ZnO to build the designed multi-layer stacked CTLs can be a promising strategy to enhance the overall memory characteristics of our proposed CTM-TFTs.

Meanwhile, the deposition method of CTL is also one of the important strategies to be considered. To obtain well-designed stack-structured HfO_2/ZnO CTL, the film thickness and uniformity should be controlled in a nanometer scale. Moreover, each layer should remain smooth surface for forming good interfaces with other layers. Therefore, the atomic-layer deposition (ALD) can be a promising method to uniformly form the functional oxide thin films in their thicknesses and compositions. One of the specified benefits of ALD is to form the laminated film structures by designing the ALD cycle configuration. By adding or subtracting several cycles of precursors, we can design the multi-layer structures composed of each oxide film with planned composition and thickness.

Thus, in this work, we uniquely introduced a stack-structured CTL with HfO_2/ZnO multi-layers using ALD process and investigated the effects of ALD cycle configuration of stack-structured CTLs on the memory characteristics of the fabricated CTM-TFTs. It is the first time to suggest the stacked CTLs using combinations of oxide semiconductor and high-k dielectric. A few layers of high-k HfO_2 thin films were inserted between the ZnO semiconducting layers, which were confirmed to show sound CTL behaviors. The ALD cycle configuration was designed so as to confirm two effects of the inserted HfO_2, which were the number of inserted HfO_2 layers and the thickness of HfO_2 introduced at once. The CTM-TFTs using the HfO_2/ZnO stacked CTL with good interface qualities showed sound memory operations including rapid P/E speed as well as large memory window by adding a few layers of HfO_2 with a sufficient thickness to work as CTL. The physical origins of the variations in memory device characteristics with various stacked CTL structures were extensively discussed and the impacts of the device fabrication process was also suggested as one of the important controlling parameters influencing the device performance.

II. EXPERIMENT

We firstly prepared metal-Al_2O_3-HfO_2-Al_2O_3-Si (MAHAS) capacitors in order to check the charge-trap feasibility of HfO_2 itself. A 3-nm-thick Al_2O_3 tunneling layer was deposited by ALD at 180 °C on the cleaned p-type Si substrates. Then, an 8-nm-thick HfO_2 CTL was formed at different ALD temperatures. When the ALD temperatures were varied to 100, 150, and 250 °C, the cycle numbers for depositing HfO_2 were controlled as 80, 80, and 100, respectively, considering a different deposition rates at each temperature condition. A 50-nm-thick Al_2O_3 blocking oxide was deposited using ALD at 150 °C. A 100-nm-thick Al was

formed as top electrode using thermal evaporation and patterned with the size of 200×200 μm^2 by photolithography and lift-off process. The backside contact was formed by using silver paste.

We fabricated the top-gate CTM-TFTs using HfO_2/ZnO stacked-CTLs on the indium-tin oxide (ITO)-coated glass substrates. The ITO was patterned into source/drain (S/D) electrodes using photolithography and wet-etching process. A 25-nm-thick amorphous In-Ga-Zn-O (IGZO) was formed as an active layer using RF magnetron sputtering at room temperature (RT) with an IGZO (In:Ga:Zn=2:1:2 atomic ratio) single target. An Al_2O_3 tunneling oxide was deposited in two steps in order to protect the IGZO active layer from chemical damages during the CTL patterning process. The first 5-nm-thick Al_2O_3 tunneling layer was formed via ALD at 180 °C. Then, the stacked structure of IGZO and the first tunneling layer were patterned by a diluted hydrofluoric acid-based (DHF) wet etchant. Next, 5-nm Al_2O_3, 22-nm HfO_2/ZnO, and 3-nm Al_2O_3 layers were deposited consecutively by ALD without breaking a vacuum at 180, 100, and 150 °C, as the second tunneling, charge-trap, and top protection layers, respectively. Trimethylaluminium (TMA), diethylzinc (DEZ), tetrakis(ethylmethylamino)hafnium (TEMAHf) and water vapor (H_2O) were employed as aluminum, zinc, hafnium precursors and oxidant, respectively. After one-step etching for the second tunneling and charge-trap layers, a 50-nm-thick Al_2O_3 blocking layer was deposited by ALD at 150 °C and patterned using phosphoric acid for metal contact. Finally, the ITO film with a thickness of 150 nm was prepared via DC sputtering and patterned as gate electrodes and S/D pads by lift-off process. Figures 1(a) and 1(b) show cross-sectional views of the fabricated MAHAS capacitor and CTM-TFT, respectively.

The HfO_2/ZnO stack-structured CTL is the most important part to determine the device properties in this work. The main idea is adding high-k HfO_2 thin films into the ZnO layers. The ALD cycle configurations were designed to figure out the effects of the number of HfO_2 layers inserted between the ZnO and the thickness of one inserted layer of HfO_2. Detailed ALD cycle configurations for the stacked CTLs were designed as follows: HfO_2 thin films were inlaid once, twice, and four times between the ZnO layers, in which the ALD cycles of inserted HfO_2 layer was set as 10 and the supercycle was adjusted to obtain total CTL thickness of 22 nm. The thickness of one inserted layer of HfO_2 corresponds to 2 nm. For conveniences, we termed these devices as S1, S2, and S3, respectively. The S4 was also prepared to examine the thickness effect of inserted HfO_2 layer, in which a 20-cycled HfO_2 layers with a thickness of 4 nm were inlaid twice between the ZnO. All the inserted HfO_2 layers were positioned to keep them with an equal distance. The designed ALD cycles were illustrated in Fig. 1(c).

Chemical bonding characteristics were analyzed by X-ray photoelectron spectroscopy (XPS) using Al Kα radiation at

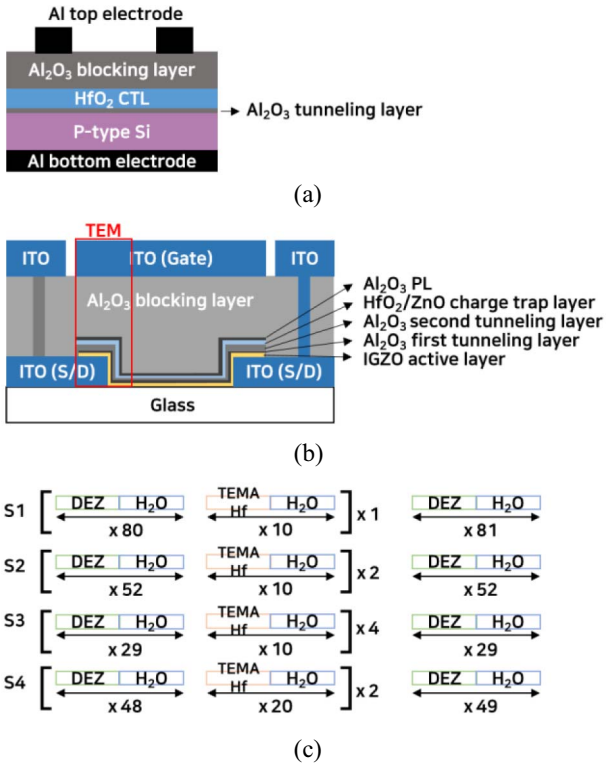


FIGURE 1. Schematic cross-sectional view of the fabricated MAHAS capacitors and (b) IGZO CTM-TFTs using HfO_2/ZnO stack-structured CTLs. (c) ALD cycle configurations for the HfO_2/ZnO stack CTLs for the S1, S2, S3, and S4.

a scan step of 0.05 eV. The cross-sectional microstructures of the fabricated CTM devices were visually observed by scanning transmission electron microscopy (STEM, JEM-ARM200F) at an accelerating voltage of 200 kV. The TEM samples were prepared using a dual-beam focused ion beam (FIB, FEI, Nova200) in TEM sample preparation mode. The observation areas were determined at edge and center regions of the CTL, as indicated in Fig. 1(b).

The device characteristics of the fabricated MAHAS capacitors and IGZO CTM-TFTs were evaluated by using a semiconductor parameter analyzer (Keithley 4200SCS) and a pulse generator (HP 8110A) in a dark box at RT. The gate width (W) and length (L) of the evaluated TFTs were 40 and 40 μm, respectively. The overlap margin between the IGZO active layer and CTL was 5 μm on both sides of the electrodes.

III. RESULTS AND DISCUSSION

A. INVESTIGATIONS ON THE FEASIBILITY OF HFO_2 AS CHARGE TRAP LAYER

Figure 2(a) shows the high-frequency (1 MHz) capacitance-voltage (C-V) characteristics for the MAHAS capacitors using HfO_2 CTLs deposited at various ALD temperatures of 100, 150, and 250 °C. All devices showed counterclockwise hysteresis in C-V curves, which means that the charge-trapping events occurred in HfO_2 thin films, when the gate

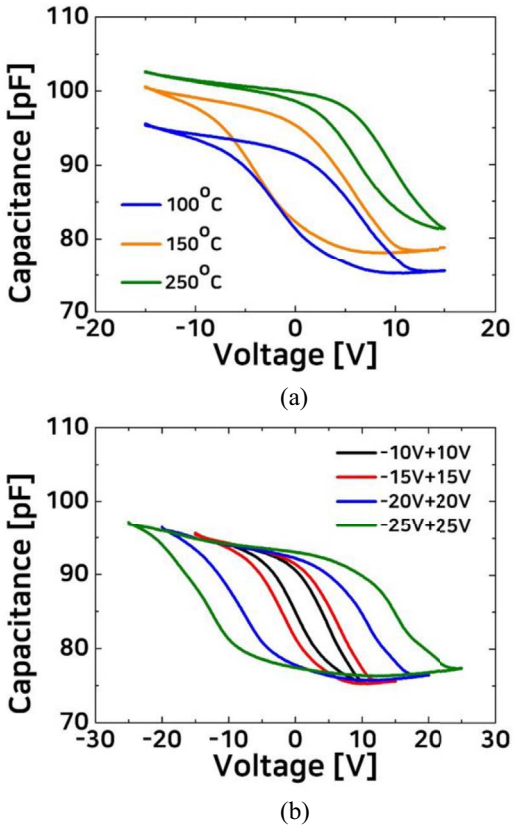
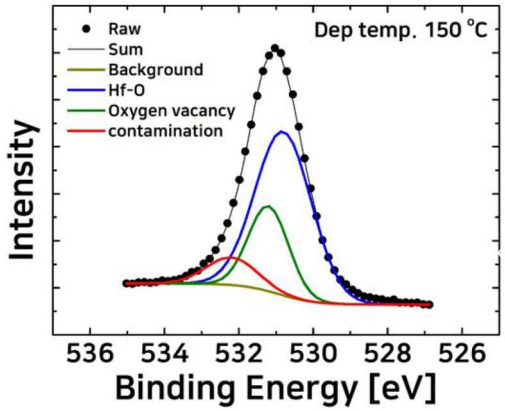


FIGURE 2. (a) Comparison of C-V curves among the MAHAS capacitors with HfO_2 CTLs prepared at deposition temperatures of 100, 150, and 250 °C at 1 MHz. (b) C-V curves of the MAHAS capacitors using HfO_2 deposited at 100 °C with different gate voltage sweep ranges from ±10 to ±25 V.

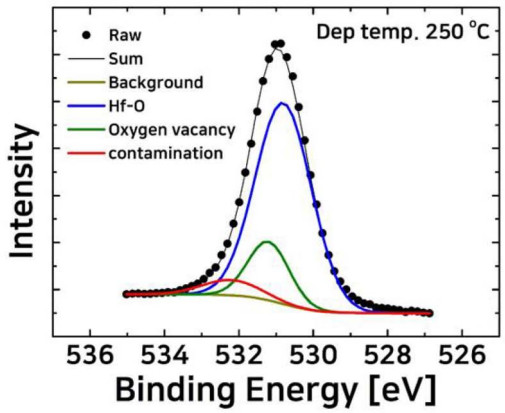
voltage (V_{GS}) was swept from −15 to +15 V and then reversed to −15 V. However, the width of MW, which is defined as the difference of the flat-band voltage between the program and erase states generated by charge-trap/detrap events, were remarkably dependent on the deposition temperature. While there was no marked difference in the MW when the ALD temperature was varied from 100 to 150 °C, the MW width significantly decreased with increasing the ALD temperature from 150 to 250 °C. These results suggest that the HfO_2 thin films deposited at a temperature lower than 150 °C can exhibit higher charge-trap capability. These temperature-dependent nonvolatile memory properties can be explained by the predominant physisorption and weak thermal decomposition at low deposition temperature. Thus, imperfect chemical reactions can induce more trap sites such as functional adsorption sites and oxygen vacancies. The devices showed slight dispersion of capacitance values due to the differences in dielectric constants depending on the ALD temperatures. The capacitance at an accumulation region increased as increases in ALD temperature owing to the increment of dielectric constant of the HfO_2 film [22]. Thickness variations might also influence on the capacitance dispersions, even though we calibrated the film thickness considering the deposition rate depending on the ALD temperature. The MW of the MAHAS capacitors using the HfO_2 deposited at 100 °C increased from 7.6 to 27.6 V when the V_{GS} sweep ranges were varied from ±10 to ±25 V, respectively, as shown in Fig. 2(b). It is noteworthy that the MW width could be controlled by the P/E voltage ranges. The difference in memory device characteristics depending on the deposition temperature can also be examined from the XPS results. Figures 3(a) and (b) show the O 1s spectra and their deconvolution fitting curves of the HfO_2 thin films prepared at deposition temperature of 150 and 250 °C, respectively. The Shirley type background was utilized and the background binding energy was set from 527 to 535 eV. The peaks of oxygens in oxygen lattices, oxygen vacancies, and contaminations in O 1s spectra were decomposed to be about 530.8, 531.2, and 532.2 eV, respectively. The relative areal ratios of each bonding to the total area in the O 1s spectrum were shown in Fig. 3(c). The relative areal percentage of oxygen vacancies were 24.4 and 16.6 % for the HfO_2 grown at 150 and 250 °C, respectively. When the deposition temperature increased, relative areal percentage of oxygen vacancies and contamination decreased. It was confirmed from these results that the HfO_2 thin films deposited at an ALD temperature lower than 150 °C can be utilized as promising CTLs for the proposed CTM-TFTs thanks to high-density trap sites such as oxygen vacancies induced by incomplete chemical reactions due to lack of thermal energy during the ALD process.

B. DEVICE CHARACTERISTICS OF THE CTM-TFTS USING THE HFO_2/ZNO STACKED CHARGE TRAP LAYERS

Figure 4(a) shows the drain current – gate voltage (I_{DS}-V_{GS}) characteristics of S1, S2, S3, and S4 devices using the HfO_2/ZnO stacked CTLs, in which CTLs were deposited at 100 °C on the basis of the previous results obtained at MAHAS capacitors. All devices showed the MW of at least 16 V when the V_{GS} was swept in the range from −25 to 25 V in forward and reverse directions. The MW values of S1, S2, S3, and S4 devices were measured to be 21.2, 21.4, 16.6, and 25 V, respectively. While the S4 showed the largest MW, the S3 showed the narrowest MW. The significant variations in the MW among the devices can be explained by the effect of HfO_2 layers inserted between the ZnO layers. The thickness of inserted HfO_2 was expected to be about 2 nm for the S1, S2, and S3 devices according to the designed ALD configuration [Fig. 1(c)]. However, it can be supposed that 2-nm-thick HfO_2 layer is too thin to trap the charges but may act as a just insulator. Thus, the MW of the S3 was relatively narrow due to the counteraction against the charge-traps within a thin HfO_2 layer. On the other hand, considering that the MW of the S4 was markedly larger than other devices, the thickness of the inserted HfO_2 layer should be prepared to be as thick as 4 nm in order to work as CTL due to higher total trap densities. Nevertheless, the S1 and S2 exhibited similar MW values. It can be suggested that 2-nm-thick HfO_2 thin films inserted between the ZnO layers



(a)



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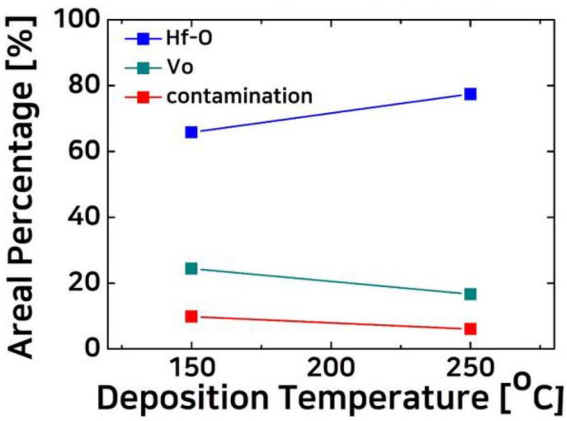
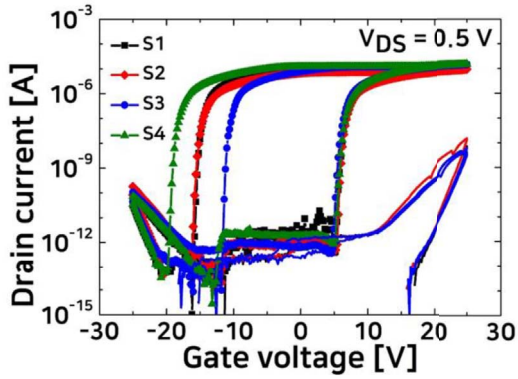
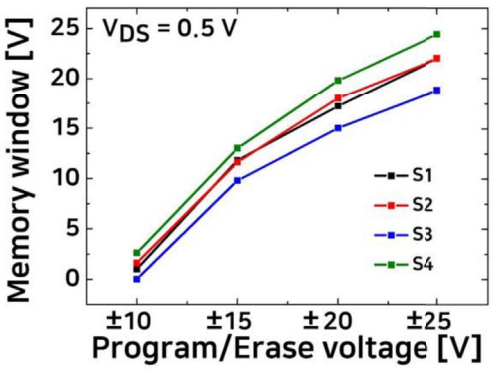


(c)

FIGURE 3. **Variations of the O 1s spectra in HfO_2 thin films deposited at (a) 150 and (b) 250 °C, respectively. (c) Summary of the relative areal ratio for each peak to total peak area.**



(a)



(b)

FIGURE 4. **(a) Comparison of I_{DG}-V_{GS} characteristics for the S1, S2, S3, and S4 using the HfO_2/ZnO stack CTLs. The V_{GS} was swept in the ranges from −25 to 25 V at V_{DS} of 0.1 V. (b) Variations in the MW depending on gate voltage sweep ranges for the S1, S2, S3, and S4.**

do not significantly influence on the memory properties when the HfO_2 layer was introduced once or twice because they occupy only a small proportion within the total CTL structures. However, when more than four layers of 2-nm-thick HfO_2 were inserted between the ZnO, the total thickness of CTL that can actually trap the charges markedly decreased and the charge-trap events were suppressed to the contrary. The MWs for all the devices almost linearly increased with increasing the V_{GS} sweep range from ±10 to ±25 V due to the increases in total number of trapped charges, as shown in Fig. 4(b). All the devices except for the S3 showed clear MW even at a V_{GS} sweep range of ±10 V. Thus, the MW was found to be readily modulated by just controlling the V_{GS} sweep range due to the efficient charge-trapping effects.

Next, the P/E speeds of the fabricated devices, which is one of the essential memory performances, were investigated. Figure 5 represents the variations in the programmed I_{DS} values for each device when the read-out voltage (V_R) was fixed at 0 V. The pulse width was varied to 1 μs, 10 μs, 100 μs, 500 μs, 1 ms, 10 ms, 100 ms, 200 ms, 500 ms, and 1 s when the pulse amplitudes were set as −20 and +20 V for P/E operations, respectively. The S3 showed the memory on/off ratio as high as 10^7 only when the pulse width was controlled to be longer than 100 ms. On the contrary, for the S1 and S2, the on/off ratio higher than 10^7 could be obtained even with 100-μs-wide P/E pulses. For the S4, the P/E pulses as long as 500 μs was required to secure the on/off ratio of 10^7. These results were attributed to the differences in number and thickness of inserted HfO_2 layers. First, in terms of number of inserted HfO_2 layer,

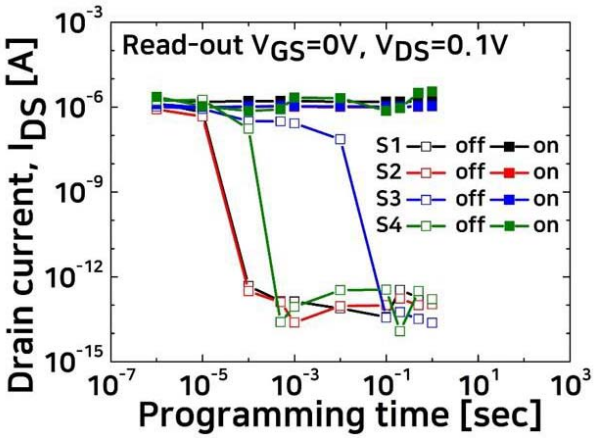


FIGURE 5. Variations in the programmed I_{DS} of on- and off- states for the CTMs as a function of program pulse width from 1 s to 1 μs. The pulse amplitudes for the on- and off-states were fixed at −20 and 20 V, respectively. The read-out voltage was set as 0 V and a V_{DS} of 0.1 V.

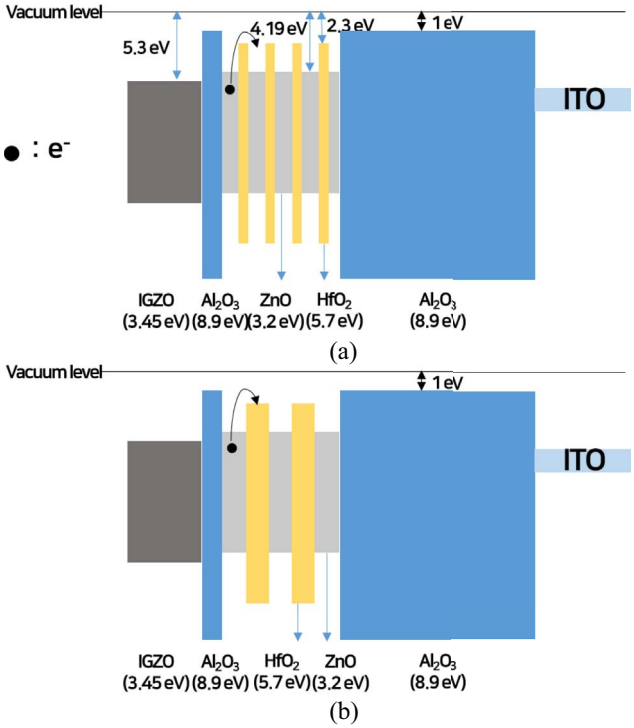


FIGURE 6. Schematic illustration of band diagram of the stack structured CTLs for the (a) S3 and (b) S4 devices, respectively, without application of external electric field. The movements of electron charges within the different CTL structures for both devices were indicated by arrows.

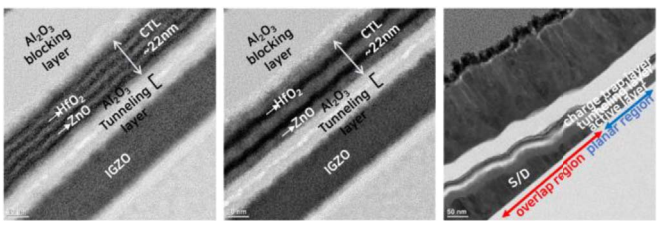


FIGURE 7. Cross-sectional STEM-HAADF images at active channel planar regions for the (a) S3 and (b) S4, respectively. Cross-sectional STEM-HAADF images at overlap region at source (drain)/channel/tunnel/charge trap layer for the (c) S4.

the charge-trap operations as well as the drifts of charges injected from the channel were suggested to be markedly interrupted with increasing the number of the inserted thin HfO_2 layers when the inserted HfO_2 thickness was 2 nm. As a result, the S3 with the largest portion of 2-nm-thick HfO_2 layers within total CTL stack showed the narrowest MW and the slowest P/E speed. Whereas, the S4 representing the widest MW showed degraded P/E speed compared with the S1 and S2. Thus, secondly, in terms of thickness of the inserted HfO_2 layers, the total P/E speed for the stack CTL was dominantly determined by the thickness of HfO_2 inserted at once. That is, the migration velocity of trapped charges within the 4-nm-thick HfO_2 layer was supposed to be slower than that within the ZnO layer and hence the P/E operations may be retarded, although the HfO_2 can be acted as a promising CTL.

Figures 6(a) and 6(b) show the schematic illustrations of the band diagrams for the S3 and S4, respectively, when no external field was applied to gate terminal. For the S3 shown in Fig. 6(a), the electrons injected from the active channel just pass through the HfO_2 layer and are trapped in only ZnO layers because the HfO_2 thickness is too thin to effectively trap the electrons compared to the ZnO layers. Therefore, it takes more time to sufficiently trap the charges within total CTL structure due to the inserted dielectric HfO_2 layer, and hence, the P/E speed of the S3 may be lag behind. On the contrary, for the S4 [Fig. 6(b)], since 4-nm-thick HfO_2 layers can be acted as effective CTLs, parts of electrons can be easily trapped in the 4-nm-thick HfO_2 layers and others can migrate through the total CTL structures during the charge-trap events, even though their velocity is not so fast. Thus, the P/E speed of the S4 was examined to be faster than that of the S3, as shown in Fig. 5. Alternatively, it is interesting to note that the S1 and S2 did not exhibit any marked differences in their memory characteristics including the MW and P/E speed, as discussed above. We expect that the memory retention properties will be different between the S1 and S2 because the 2-nm-thick HfO_2 layers might impede the charge trapping into the CTL and retaining the trapped charges. However, because the device fabrication process should be additionally improved to fairly evaluate the memory retention characteristics, which will be discussed in the next section, the data retention properties of our proposed CTM-TFTs and their comparisons among the controlled devices will be carefully investigated as future works.

C. IMPACTS OF THE INTERFACE QUALITIES IN THE STACKED CTLS ON DEVICE CHARACTERISTICS

Figures 7(a) and 7(b) show the STEM images of the S3 and S4 devices in planar regions, representatively. All the layers

have uniform surfaces and well-distinguished clear interfaces between the layers with a benefit of ALD process. Both devices have the same thicknesses of IGZO active, Al_2O_3 first and second tunneling, and Al_2O_3 blocking layers, which were estimated to be 25, 5, 5, and 50 nm, respectively. These values were well accordance with our designs. As a main concept of device structure, the stacked CTLs of the S3 and S4 display obvious distinctions at the planar region on the active channel. The total thicknesses of the CTLs for both devices were 22 nm. For the S3, the stacked CTL included four layers of HfO_2 with a thickness of approximately 2 nm between the ZnO layers. On the other hand, thicker HfO_2 layers of 4 nm were inlaid twice between the ZnO for the S4. Although the well-designed CTL structures were achieved in the planar channel region, it would be more important to carefully control the conformal interfaces within the gate stack structures at the overlapped regions among the Al_2O_3 tunneling, IGZO active, and ITO S/D layers in order to obtain the memory characteristics as designed and expected. It was previously reported for our fabricated CTM-TFTs that the charge trap/detrap events were mainly determined at these overlapped regions due to the electric field concentration caused by rough surfaces locally damaged during the wet etching process [23]. Therefore, it is also important to carefully check the interface qualities within the gate-stacks at the overlapped regions. Figure 7(c) represents the STEM images of the overlapped region for the S4. Even though the overlapped regions appeared to be rather rough and rippling due to the tapered slope and rugged surfaces of ITO layers caused by wet etching process, the interfaces were so clearly defined between the layers, and each layer composing the stacked CTL structure was formed with uniform thickness along the surface of a lower layer without any disconnection and/or aggregation. In other words, each layer was conformally formed to have designed film thickness, and this device showed good memory characteristics, as discussed above. Thus, when the designed stacked CTLs could be well prepared within the gate-stack structures at planar channel region as well as at overlapped regions, the memory operations of the fabricated CTM-TFTs could be effectively modulated with the differently designed CTL structures.

Here, we suggest the additional impacts of fabrication process as important and interesting control parameters influencing on the memory device characteristics. Alternatively, the reliability and reproducibility of the proposed CTM-TFTs employing the designed stacked CTLs should be carefully checked, even though the best devices exhibited the sound memory characteristics as expected. Especially, as mentioned above, the gate-stack structures including the stacked CTLs should be identically prepared at the overlapped regions to satisfy the device reproducibility. In order to experimentally verify this important issue, several number of devices with the same structure of stacked CTL were repeatedly fabricated and the microstructures at the overlapped regions of the fabricated devices were analyzed with TEM images.

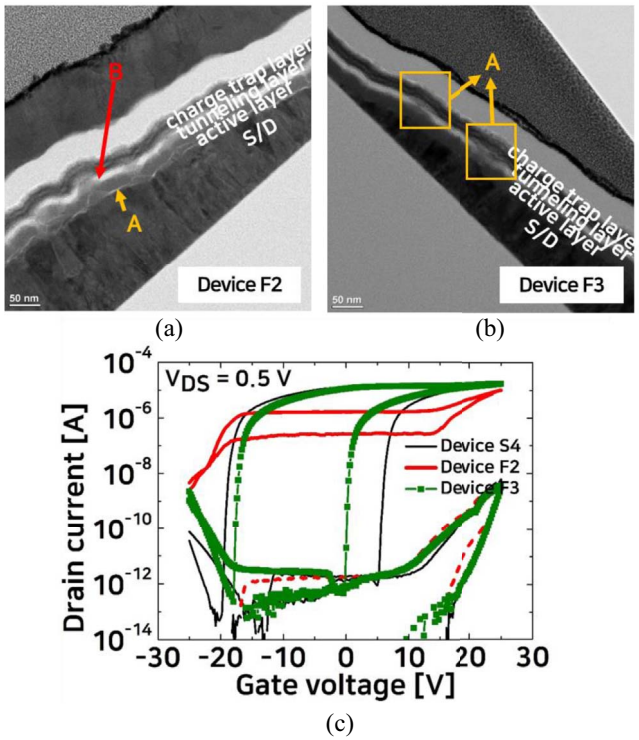


FIGURE 8. Cross-sectional STEM-HAADF images at overlap regions for the (a) F2 and (b) F3, respectively. (c) Comparisons of I_{DG}-V_{GS} characteristics for the S4, F2, and F3 fabricated with the same gate stack structures.

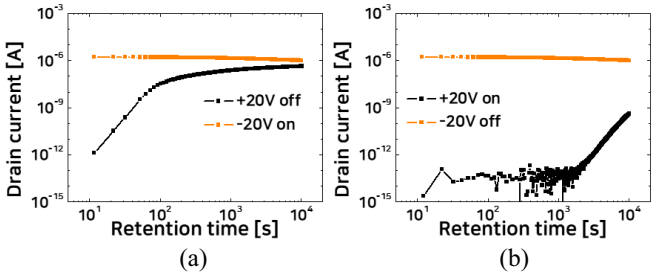


FIGURE 9. Typical characterizations on the memory retention properties of the on- and off-programmed currents for the device S2 fabricated (a) before and (b) after the subsequent improvements in process conditions.

Figures 8(a) and (b) represent the STEM images of additionally fabricated two devices using 4-nm-thick HfO_2 layers inserted twice, respectively. Figure 8(c) shows the comparisons of the memory characteristics among the additionally fabricated devices and the S4 discussed in Section II. For convenience, the additionally fabricated two devices were termed F2 and F3, respectively. The device S4 were confirmed to show good memory characteristics thanks to well-prepared interfacial qualities within the gate-stacks, as shown in Fig. 7(c). On the contrary, for the device F2 shown in Fig. 8(a), the contact regions between the ITO S/D and IGZO active layers were incompletely formed with distinct interface boundaries, as indicated by arrow A in

Fig. 8(a). In addition, tunneling layer failed to have smooth surface and uniform thickness, as indicated by arrow B in Fig. 8(a), owing to uneven film surface of the IGZO active layer compared with well-fabricated devices. Poor qualities of contact reasons between the S/D and active layers may limit the on-current owing to considerable amount of contact resistance [24]. As results, the F2 showed the marked degradations in device characteristics including high off-current and low on-current, as confirmed in Fig. 8(c). Alternatively, for the device F3 shown in Fig. 8(b), the interfaces within the gate-stacks composed of active, tunneling, and charge trap layers were not clearly discriminated, showing undesirable inter-diffusion, as described in box area A in Fig. 8(b). Especially, the tunneling layer thickness could not be accurately defined due to the formation of interfacial transition layer. As results, the F3 exhibited narrower MW compared with the S4 because of poor interfacial qualities of the gate-stack. Furthermore, the long-term memory retention, which is one of the important performances to be carefully checked for memory devices, was found to be sensitively influenced by slight differences in final device structures resulted from the minute changes in processes at each fabrication than the device characteristics including the charge-trap assisted MW and P/E program operations. In other words, the fabrication process details and resulting final device structure should be very carefully controlled for accurately comparing the memory retention performance among the devices with differently designed CTL structures proposed in this work. However, unfortunately, it was very difficult to reproducibly prepare the gate-stack structures, because the gate-stacks composed of several-nm-thick thin films can be easily deteriorated during the device fabrication processes such as wet etching. Figure 9(a) shows the memory retention properties of the firstly fabricated S2. While there was no marked variation in programmed current of the on-state with time evolution, the off-programmed current drastically increased with a lapse of retention time. From these results, it can be suggested that the charges could not be stably trapped in the CTL for a long time, which was supposed to be due to rough interfaces within the gate stack structure irrespective of conformal formation of each layer, as can be seen in Fig. 7. Whereas, better retention properties of the S2 could be obtained by carefully optimizing the etching process, as shown in Fig. 9(b), even though both devices have the same gate stack structures. As an example, 1-wt% amounts of ammonium fluoride was specifically mixed with the diluted hydrofluoric acid as a wet chemical etchant to reduce the etch time for the HfO_2 layers, since an etch time as long as 3 min might deteriorate interfacial qualities within gate stack structure. In conclusion, the careful optimization of the device fabrication process as well as accurate designs for the stacked CTL structures are quite demanding to ensure improved device characteristics for our proposed memory TFTs. Namely, the nonvolatile memory characteristics can be expected to be far enhanced by accurately controlling the gate-stack structures including the stacked CTLs as designed. Thus, additional optimization of fabrication process will be performed to improve the reproducibility in preparing the interfacial qualities in the gate-stacks of the CTM-TFTs as future works.

IV. CONCLUSION

We proposed IGZO-channel CTM-TFTs using newly designed stacked CTLs composed of high-k dielectric HfO_2 and oxide semiconductor ZnO. The nonvolatile memory operations of the fabricated CTM-TFTs employing various structures of stacked CTL were characterized and compared when the number and the thickness of HfO_2 layers inserted into the ZnO layer were strategically controlled. All the fabricated CTM-TFTs using HfO_2/ZnO stacked CTLs exhibited good memory characteristics including large MW and fast P/E speed. When introducing the 4-nm-thick HfO_2 layers twice, the CTM-TFT showed the best device characteristics such as a large MW of 25 V and a fast P/E speed of 500 μs. Furthermore, the memory operations could be successfully confirmed even with P/E program voltage of $\pm$10 V. On the contrary, the inserted HfO_2 layer with a thickness of 2 nm were found to be inappropriate for the CTL applications due to its dielectric properties with smaller number of trap sites. It is also noteworthy that the obtained device characteristics were closely related to the interface qualities within the gate-stack structures including the stacked CTLs especially at overlap regions among the charge-trap, tunneling, active, and S/D layers. In other words, when the stacked CTLs were well prepared with good interfaces by ALD process, the memory performance of the CTM-TFTs using various CTL structures could be guaranteed as designed. However, to realize highly reproducible memory characteristics of our proposed CTM-TFTs, the fabrication process window was suggested to be additionally enhanced owing to the unavoidable variabilities in process-dependent device structures. Consequently, the introduction of HfO_2/ZnO stacked CTLs prepared by ALD process can be a useful methodology to provide highly-functional memory devices for future flexible and transparent electronics applications.

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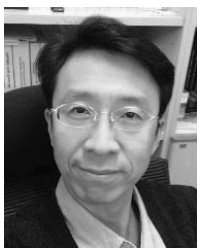

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