Received 13 February 2019; accepted 17 March 2019. Date of publication 3 April 2019; date of current version 19 April 2019.
The review of this paper was arranged by Editor C. Bulucea.

Digital Object Identifier 10.1109/JEDS.2019.2907314

Improving the Scalability of SOI-Based Tunnel FETs Using Ground Plane in Buried Oxide

SHELLY GARG AND SNEH SAURABH (Senior Member, IEEE)

Department of Electronics and Communication Engineering, Indraprastha Institute of Information Technology Delhi, New Delhi 110020, India

CORRESPONDING AUTHOR: S. GARG (e-mail: shellyg@iiitd.ac.in)

This work was supported in part by the Science and Engineering Research Board (SERB), Department of Science and Technology (DST), India, under Grant ECR/2016/001268, and in part by University Grants Commission (UGC) under Senior Research Fellow Scheme (SRF).

ABSTRACT Tunnel field-effect transistors (TFETs) are known to exhibit degraded electrical characteristics at smaller channel lengths, primarily due to direct source-to-drain band-to-band tunneling (BTBT). In this paper, we propose a technique to suppress direct source-to-drain BTBT by increasing the effective distance between the source and the drain. We propose to add a ground plane (GP) in the buried oxide of a silicon-on-insulator (SOI) TFET which depletes the drain and increases the effective source-to-drain distance. Using 2-D device simulations it is shown that the introduction of the ground plane is effective in reducing OFF-state current and ambipolar current, as well as, in improving the average subthreshold swing for the small channel length SOI-TFETs. Additionally, the addition of GP is helpful in ameliorating the short-channel effects, such as drain-induced barrier lowering and threshold voltage roll-off.

INDEX TERMS TFETs, SOI, ground plane, scalability, short-channel effects, ambipolar current.

I. INTRODUCTION

Tunnel field-effect transistor (TFET) is a promising device because of its ability to deliver subthreshold swing smaller than 60 $mV/decade$ at room temperature [1]–[5]. However, in TFETs with small channel length, there is a direct band-to-band-tunneling (BTBT) between the source and the drain leading to unacceptably high OFF-state current (I_{OFF}), affecting the scalability of the TFETs [6], [7]. Moreover, TFETs suffer from the problem of ambipolar conduction which restrict the use of TFETs in wide-scale applications [4], [7]–[9].

Ambipolar conduction in TFETs can be suppressed using various techniques proposed in literature such as asymmetric doping in source and drain regions, gate overlap and underlap, spacer engineering, hetero-dielectric buried oxide (HDB), gate material engineering, DP-DGTFET etc [6], [7], [10]–[16]. However, most of these techniques are not effective at smaller L_G and, hence, are not directly useful in future advanced technologies. For instance, gate-on-drain overlap method was proposed in [14] to improve the ambipolar behaviour of the TFETs. This approach cannot be scaled below a certain L_G due to requirement of about 30 nm overlap for suppressing the ambipolar current (I_{AMB}). Therefore, techniques that can suppress ambipolar conduction at small device dimensions are highly desirable.

Further, the scalability of TFETs, which is critical for employing them in futuristic circuits, has not been investigated adequately. It is worthy to note that, the I_{OFF} in a TFET is sensitive to gate lengths, especially when the gate lengths are small due to dominant direct source-to-drain tunneling at small channel lengths [6], [17]. This leads to increased I_{OFF} and degraded average subthreshold swing (SS_{avg}). As a result, the biggest advantage of TFET to achieve steeper subthreshold swing is lost at smaller gate lengths [6], [7], [17], [18]. Additionally, TFETs are prone to short-channel effects (SCE) such as drain-induced barrier lowering (DIBL) and threshold voltage (V_T) roll-off [7], [17]. These problems must be addressed before employing TFETs in future technologies.

In this paper, we investigate silicon-on-insulator (SOI) TFET with ground plane (GP) inserted in the buried oxide (BOX) to ameliorate the above mentioned problems. We refer to the SOI-TFET with ground plane as GP-TFET.

Ground plane in buried oxide (GPB structure) has been demonstrated earlier to improve the performance of the MOSFET in [19]. It has been demonstrated that GBP

2168-6734 © 2019 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

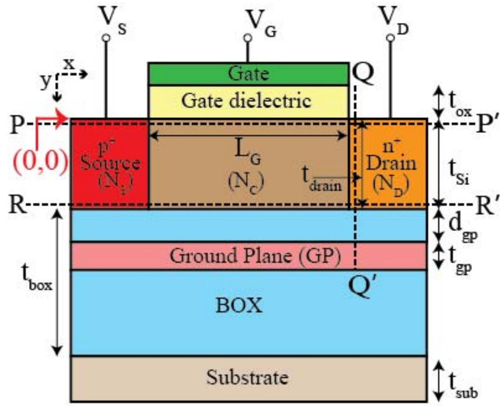

FIGURE 1. Schematic cross-sectional view of GP-TFET.

suppresses DIBL in SOI-MOSFET by acting as a sink to the drain electric-field. However, since the operating principle of MOSFETs and TFETs are different, the application of GP in TFETs is not straight-forward. Additionally, as demonstrated in this work, the mechanism of improvement in electrical characteristics in TFETs due to GP is quite different from that in a MOSFET. It is also worthy to point out that the focus of the paper is to demonstrate the effectiveness of GP in improving the scalability of TFET and not to propose TFET as a better device compared to the-state-of-the-art MOSFETs. Since, Si-based TFET is analyzed in this work, the reported ON-state current is comparatively low, in agreement with literature [4], [5], [10], [11], [15], [20], [21]. Moreover, it must be pointed out that the main objective of this work is to demonstrate the relative impact of addition of the ground plane on the electrical characteristics of the TFET rather than demonstrating the absolute current and voltage levels for the proposed device.

In this paper, we have shown that adding GP to SOI-based TFETs leads to increased effective drain-to-source distance thus suppressing the direct source-to-drain tunneling in small channel length SOI-TFETs. In effect, a lower I_{OFF} and a better average subthreshold swing (SS_{avg}) is obtained, even at smaller gate lengths, thus improving the scalability of the device. The short-channel effects such as DIBL and V_T roll-off are also reduced by the addition of the GP. Moreover, I_{AMB} is fully suppressed due to the increased tunneling barrier width at the drain-channel interface in GP-TFET.

The rest of this paper is organized as follows. In Section II, the proposed device structure and simulation model are explained. The device operation, characteristics and scalability are discussed in Section III. In Section IV, the ambipolar behaviour of the device is analyzed. In Section V, we have described the mechanism of suppression of ambipolar current in a GP-TFET in detail. Section VI concludes the paper.

II. DEVICE STRUCTURE AND SIMULATION MODEL

Fig. 1 shows the schematic cross-sectional view of a GP-TFET. SOI-based n-TFET consists of a thin silicon film over buried oxide (BOX) made up of (SiO_2) with p^+ doped source and n^+ doped drain. The gate dielectric material is assumed to be Hfo_2 ($\epsilon_r \approx 21$). In addition, GP-TFET consists of a heavily doped p^+ layer, known as ground plane (GP), inside BOX at depth d_{gp}. The device without GP is referred as conventional TFET (C-TFET). The GP-TFET structure can be created by using the Silicon-on-insulator-with-active-substrate (SOIAS) technology [22], [23]. The GP is created by ion-implantation of boron through the silicon film [19]. Since, the GP is throughout the length of the device, GP can be formed before the formation of the gate, drain and source areas in the device fabrication flow. The device parameters used in our simulations are listed in Table 1.

TABLE 1. Device parameters used in the simulation of conventional TFET and GP-TFET.

Parameter	Value
Supply voltage (V_{DD})	1.0 V
Silicon film thickness (t_{si})	10 nm
Gate oxide thickness (t_{ox})	3 nm (EOT≈ 0.5)
Gate work function (ϕ_m)	4.17 eV
Source doping (N_S) (p-type)	$1 \times 10^{20} atoms/cm^3$
Drain doping (N_D) (n-type)	$5 \times 10^{18} atoms/cm^3$
Channel doping (N_C) (p-type)	$1 \times 10^{17} atoms/cm^3$
Gate length (L_G)	10-50 nm
BOX thickness (t_{box})	60 nm
GP doping (N_{gp}) (p-type)	$1 \times 10^{20} atoms/cm^3$
GP Depth (d_{gp})	2-10 nm
GP Thickness (t_{gp})	10 nm

In this paper, all the simulations have been carried out using ATLAS version 5.22.1.R [24]. We have used non-local band-to-band tunneling (BTBT) model to compute the tunneling current [24]. We have used bandgap narrowing (BGN) model to account for highly doped regions in the devices. Fermi-Dirac statistics and Shockley-Read-Hall recombination models are also included in our simulations. All doping profiles are assumed to be abrupt. The tunneling through the gate oxide is ignored, as in earlier works [10], [13]–[15], [20], [21]. Since, the silicon film thicknesses is 10 nm, we have not considered the quantum confinement effects arising due to thin SOI body [25]–[27]. We have calibrated the simulation setup using [10], [15] and have also used in [11], [20].

III. SCALABILITY ANALYSIS OF GP-TFET

To evaluate the performance of GP-TFET, we use the following definitions in this work as shown in Fig. 2: a) I_{ON} is defined as the drain current at gate voltage (V_{GS}) = drain voltage (V_{DS}) = supply voltage (V_{DD}), b) I_{AMB} is defined as the drain current at $V_{DS} = V_{DD}$ and $V_{GS} = -V_{DD}$, c) the drain current at which the transfer characteristics start to take off is defined as I_{OFF} (i.e., minimum drain current in the transfer characteristics) and the corresponding voltage is known as $V_{OFF,1}$, d) threshold voltage (V_T) is the positive

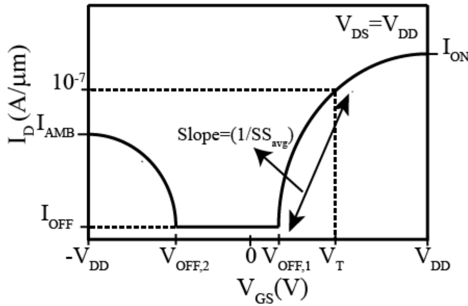

FIGURE 2. Definition of Electrical Parameters [11].

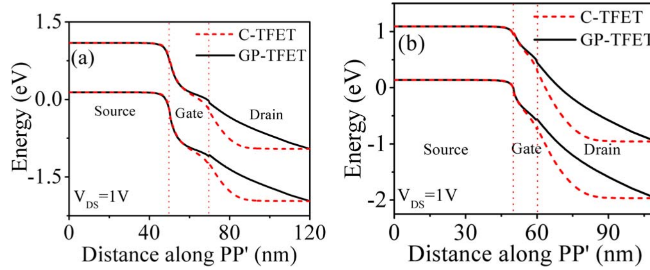

FIGURE 3. Band diagram in C-TFET and GP-TFET along PP′ in OFF-state (a) $L_G = 20\ nm$ (b) $L_G = 10\ nm$.

gate voltage at which the $I_D = 10^{-7} A/\mu m$ at $V_{DS} = V_{DD}$ and e) $V_{OFF,2}$ is the gate voltage ($V_{GS} < 0$) at which the drain current starts rising. Ideally $V_{OFF,2}$ should be $-V_{DD}$, f) SS_{avg} is the inverse slope extracted from $V_{OFF,1}$ point to V_T point in the transfer characteristics as described below [7], [10], [11]:

$$SS_{avg} = \frac{V_T - V_{OFF,1}}{log(10^{-7}) - log(I_{OFF})}. \quad (1)$$

A. TRANSFER CHARACTERISTICS AT SMALLER L_G

The motivation behind the introduction of ground plane is to deplete the drain and increase the effective distance between the source and the drain. Fig. 3(a) shows the band diagrams of C-TFET and GP-TFET for $L_G = 20\ nm$ in the OFF-state. It can be seen that for the GP-TFET, the bending of the energy-bands extends more into the drain region compared to the C-TFET, indicating the extension of the depletion region in the drain. This results in an increased effective drain-to-source distance in GP-TFET compared to C-TFET. As a result, the direct source-to-drain tunneling is inhibited in GP-TFET. Moreover, the band diagrams for C-TFET and GP-TFET for $L_G = 10\ nm$ are shown in the Fig. 3(b). It can be observed that at $L_G = 10\ nm$, the problem is aggravated by an increased direct source-to-drain tunneling in C-TFET. However, direct source-to-drain tunneling is suppressed in GP-TFET even at $L_G = 10\ nm$.

The transfer characteristics of C-TFET and GP-TFET at $L_G = 20\ nm$ are compared in Fig. 4. From Fig. 4, it can be inferred that the I_{OFF} decreases from $5 \times 10^{-10} A/\mu m$ in C-TFET to $1 \times 10^{-15} A/\mu m$ in the GP-TFET. The reduction in I_{OFF} can be attributed to the increased effective source-to-drain distance which suppresses the direct source-to-drain

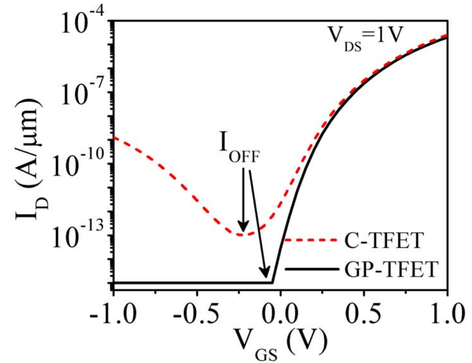

FIGURE 4. Transfer characteristics for $L_G = 20\ nm$.

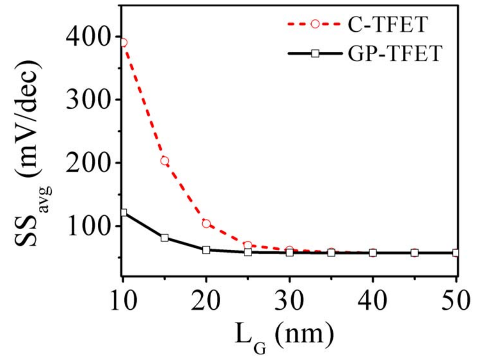

FIGURE 5. Scaling trend of SS_{avg} for C-TFET and GP-TFET.

tunneling in GP-TFET. Additionally, SS_{avg} (averaged over 8 decades of current) improves from 104 mV/dec in C-TFET to 62 mV/dec in GP-TFET. Fig. 5 shows the device scaling trend for SS_{avg} exhibiting the superior scalability of GP-TFET compared to C-TFET, especially for $L_G \leq 20\ nm$.

The improvement in the scalability of GP-TFET can be attributed to the depletion of majority carriers in the drain, as explained below.

Fig. 6(a) and 6(b), respectively, show the band diagrams along Y-axis in drain for the C-TFET and GP-TFET at equilibrium. It is evident that in GP-TFET, due to the insertion of GP, the drain gets depleted, especially close to the BOX, as shown in the encircled region. However, it should be noted that the depth of GP d_{gp} plays an important role in the depletion of drain region. Fig. 6(c) shows the impact of increase in d_{gp} on the band diagrams along Y-axis in drain for C-TFET and GP-TFET. It can be seen that as d_{gp} increases, the conduction band comes closer to the Fermi level and the drain depletion becomes comparatively low. For very high value of d_{gp}, the drain depletion ceases and band profile becomes almost similar to the C-TFET. Infact, the improvement in scalability is found to disappear when $d_{gp} > 10\ nm$.

Further, it is important to analyze the impact of N_{gp} on the electrical characteristics of GP-TFET. Using simulations, we found that varying the N_{gp} by 50% around $N_{gp} = 10^{20} atoms/cm^3$ do not degrade the ambipolar performance.

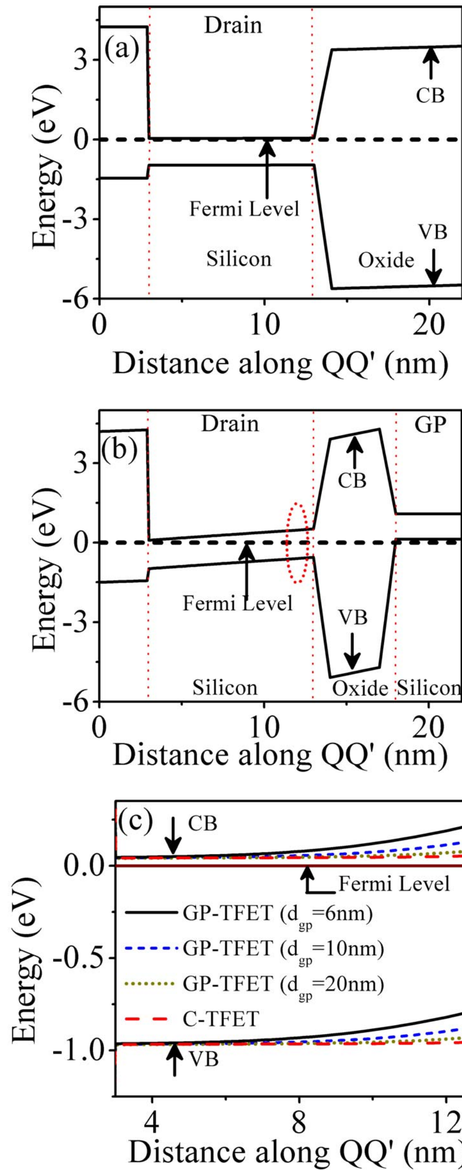

FIGURE 6. Band diagram in (a) C-TFET (b) GP-TFET (c) Impact of increase in d_{gp} on the band diagram in the drain region along QQ′ (as shown in Fig. 1) at $V_{DS} = V_{GS} = 0\ V$ for $L_G = 20\ nm$.

Moreover, maximum change in I_{ON} by the variation of N_{gp} in the above-mentioned range is 6.2%. Similarly, it is important to analyze the impact of t_{gp} on the performance of GP-TFET. Using simulations, it is observed that even 50% variation in t_{gp} around $t_{gp} = 10\ nm$ do not impact the characteristics of the GP-TFET. The maximum change in I_{ON} by the variation of t_{gp} in the above-mentioned range is 2.8% only.

Next, Fig. 7(a) and 7(b), respectively compares the electron concentration across the cutline PP′ and RR′ for $L_G = 20\ nm$. It is evident that the electron concentration in the drain region is much lower in GP-TFET compared to C-TFET, indicating the extension of the depletion region into the drain in GP-TFET. The effective source-to-drain

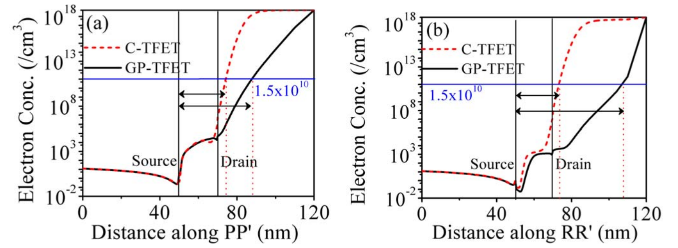

FIGURE 7. Electron concentration for C-TFET and GP-TFET at $V_{DS} = 1\ V$ and $V_{GS} = 0\ V$ for $L_G = 20\ nm$ (a) along PP′ (b) along RR′.

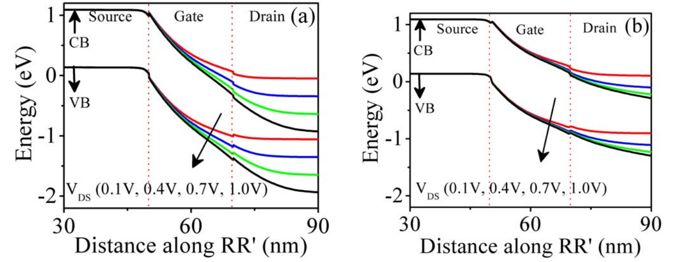

FIGURE 8. Band Diagram of (a) C-TFET and (b) GP-TFET along RR′ at $L_G = 20\ nm$ and $V_{GS} = 0.1\ V$.

distance can be defined as the distance between the metallurgical source-channel junction and the point in the drain where the electron concentration becomes equal to the intrinsic carrier concentration ($n_i = 1.5 \times 10^{10} atoms/cm^3$). It is observed that the effective source-to-drain distance increases from 22 nm in C-TFET to 34 nm for GP-TFET for cutline PP′ and from 22 nm in C-TFET to 54 nm for GP-TFET for cutline RR′. This results in improving the scalability using ground plane. Another important point to note is that the effective drain-to-source distance increases throughout the thickness of the silicon body (both along PP′ and RR′) in GP-TFET. This can be attributed to the thin silicon body ($t_{si} = 10\ nm$) and is important for improving the scalability of the device.

B. DIBL AND V_T SHIFT

In this section, the short-channel effects such as DIBL and threshold voltage roll-off are analyzed for C-TFET and GP-TFET.

Fig. 8(a) and 8(b) compare the effect of drain potential on the band diagrams of C-TFET ans GP-TFET, respectively. It is evident that the drain potential has a more pronounced effect on the tunneling barrier in the C-TFET compared to the GP-TFET. This implies that the GP-TFET is expected to exhibit a lower DIBL compared to C-TFET.

To quantify the DIBL effect, we measure the difference in the gate voltage required to attain the same drain current, at low drain voltage and at the drain voltage same as the supply voltage. The DIBL can be computed at drain current $I_{DIBL} = 10^{-9} A/\mu m$ as follows [20]:

$$DIBL = \frac{V_{GS,2} - V_{GS,1}}{V_{DS,2} - V_{DS,1}} \quad (2)$$

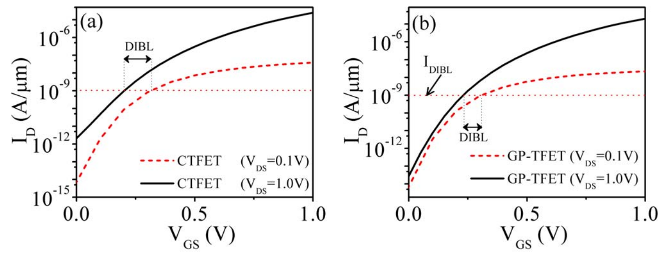

FIGURE 9. Transfer characteristics of (a) C-TFET (b) GP-TFET at $L_G = 20\ nm$ highlighting DIBL.

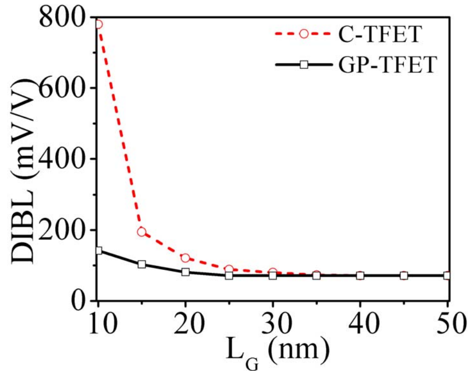

FIGURE 10. Scaling trend of DIBL characteristics for C-TFET and GP-TFET.

where, $V_{GS,2}$ is the gate voltage at which $I_D = I_{DIBL}$ and $V_{DS} = V_{DS,2} = V_{DD}$. Similarly, $V_{GS,1}$ is the gate voltage at which $I_D = I_{DIBL}$ and $V_{DS} = V_{DS,1} = 0.1\ V$.

Fig. 9(a) shows the transfer characteristics of C-TFET at $V_{DS} = 0.1\ V$ and $V_{DS} = 1.0\ V$ for $L_G = 20\ nm$. It is evident that for the C-TFET, the transfer characteristics are highly dependent on the drain voltage and the extracted value of DIBL is 121 mV/V. Fig. 9(b) shows the transfer characteristics of GP-TFET at $V_{DS} = 0.1\ V$ and $V_{DS} = 1.0\ V$. The extracted value of DIBL is 81 mV/V for GP-TFET, thus suppressing DIBL by 33%.

Fig. 10 shows the DIBL for GP-TFET compared to C-TFET at different gate lengths. For $L_G < 20\ nm$, the GP-TFET exhibits markedly lower DIBL compared to C-TFET.

Next, the threshold voltage (V_T) roll-off for the TFET is analyzed. Fig. 11 shows the threshold voltage of C-TFET and GP-TFET at different gate lengths. It is evident that there is an appreciable V_T roll-off in C-TFET compared to GP-TFET. To quantify V_T roll-off, we can compute the change in threshold voltage as follows:

$$\Delta V_T = V_{T,L_G=L1} - V_{T,L_G=L2} \tag{3}$$

where, $V_{T,L_G=L1}$ is the threshold voltage at $L_G = L1$ and $V_{T,L_G=L2}$ is the threshold voltage at $L_G = L2$. Here, $L1 = 50\ nm$ and $L2 = 10\ nm$. ΔV_T is found to be 155 mV for C-TFET. However, for GP-TFET, ΔV_T is 40 mV, thus suppressing the V_T roll-off by 74%.

It is worthy to point out that the addition of GP is known to improve the scalability of a MOSFET by improving the electrostatics of the device [19]. Therefore, it is important to assess if the improvement in the scalability in TFET can be attributed to the improved electrostatics. Our study shows that the mechanism of improvement in scalability due to GP is quite different in a MOSFET and a TFET. In a MOSFET, the scalability improvement is due to the GP providing sink to electric field such that the electric field lines from drain are not able to reach the source directly. However, in a TFET, introduction of GP results in the depletion of the drain region resulting in increased effective drain-to-source distance and suppression of direct source-to-drain tunneling that becomes dominant at smaller gate lengths. Therefore, in a TFET, the improvement in scalability cannot solely be attributed to improved electrostatics, but also to the increased effective drain-source distance that suppresses direct source-drain tunneling.

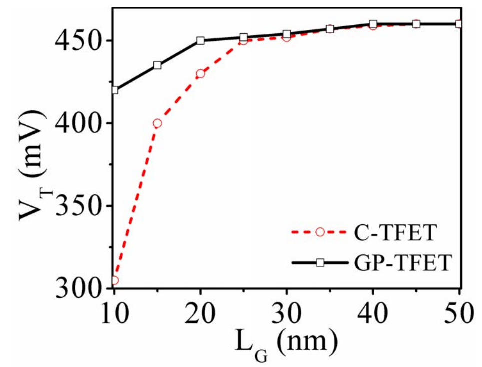

FIGURE 11. Comparison of V_T roll-off for C-TFET and GP-TFET.

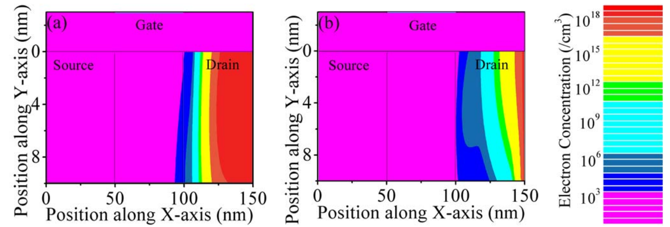

FIGURE 12. Electron concentration for (a) C-TFET and (b) GP-TFET at $V_{DS} = 1\ V$ and $V_{GS} = -1\ V$ for $L_G = 50\ nm$.

IV. AMBIPOLAR BEHAVIOUR OF GP-TFET

In TFETs, depending on the polarity of the gate voltage, the BTBT can occur at the source-channel junction as well as the drain-channel junction, resulting in ambipolar conduction [7], [11]. However, in CMOS circuits, the ambipolar behaviour is not desired. In this section, the ambipolar behaviour of GP-TFET is analyzed.

Since, addition of the GP results in the drain depletion at the drain-channel interface, hence, BTBT is expected to be suppressed in GP-TFET. Fig. 12 shows the electron concentration for GP-TFET and C-TFET in the ambipolar state. Using simulations, it is found that in the ambipolar state, the electron concentration in the drain region for GP-TFET is much lower compared to C-TFET, as depicted in Fig. 12.

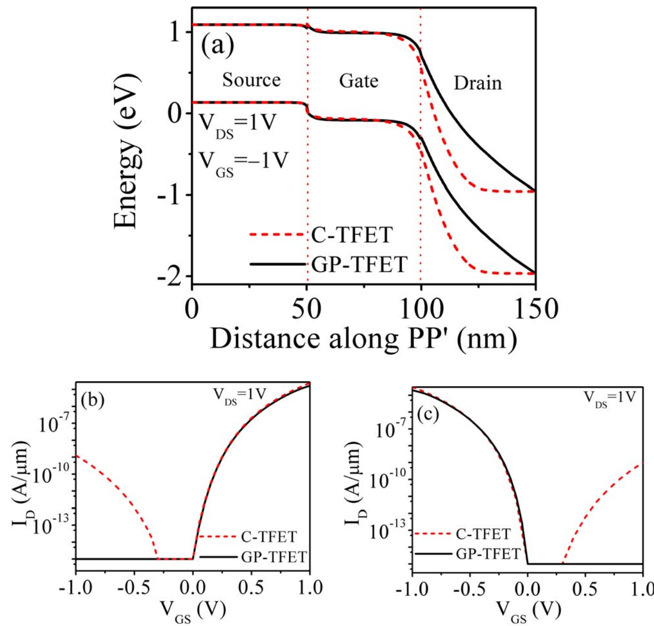

FIGURE 13. (a) Band diagram along PP′ (as shown in Fig. 1) (b) Transfer characteristics for n-type C-TFET and GP-TFET for $L_G = 50$ *nm* (c) Transfer characteristics for p-type C-TFET and GP-TFET for $L_G = 50$ *nm*.

The corresponding band diagrams in the ambipolar state are compared in Fig. 13(a) illustrating the increased tunneling barrier width in the GP-TFET. Consequently, there is a dramatic decrease in the $I_{AMB} = 1.3 \times 10^{-9}\ A/\mu m$ in C-TFET to $I_{AMB} = 1 \times 10^{-15}\ A/\mu m$ in the GP-TFET for $L_G = 50\ nm$, as shown in Fig. 13(b). The I_{AMB} decreases from $1.8 \times 10^{-9} A/\mu m$ in C-TFET to $1 \times 10^{-15} A/\mu m$ in GP-TFET for $L_G = 20\ nm$ (refer Fig. 4).

In this paper, we have primarily analyzed n-type TFETs. However, considering CMOS applications, it is important to examine the impact of addition of GP in mitigating the I_{AMB} in p-type TFETs. Our simulations show that addition of GP suppresses I_{AMB} in p-type TFET also. Fig. 13(c) compares the transfer characteristics of the p-type C-TFET with p-type GP-TFET for $L_G = 50\ nm$. It shows that addition of GP results in a decrease in I_{AMB} from $1 \times 10^{-9}\ A/\mu m$ to $1 \times 10^{-15}\ A/\mu m$. For a p-type TFET, the following parameters are used: N_S (n-type)= 1×10^{20} *atoms*/cm^3, N_D (p-type)= 5×10^{18} *atoms*/cm^3 and $\phi_m = 5.3\ eV$. The other device parameters of p-type TFET are same as in Table 1. The optimum parameter values for GP in p-type TFET are found to be: $d_{gp} = 6\ nm$ and N_{GP} (n-type)= 1×10^{20} *atoms*/cm^3.

Since the depth of the GP (d_{gp}) is the important parameter in the GP-TFET structure. It is important to analyze the impact of d_{gp} on the ambipolar behaviour of the device. Using simulations, it is found that $d_{gp} > 6\ nm$ is not able to fully suppress the I_{AMB} as shown in Fig. 14. As d_{gp} increases beyond 6 *nm*, the ground plane becomes less effective in depleting the drain in the ambipolar state. Therefore, a $d_{gp} \leq 6\ nm$ is desirable for fully suppressing the ambipolar current till $V_{OFF,2} = -V_{DD}$. However, it is important to mention that d_{gp} cannot be decreased arbitrarily to very small values, since for extremely small d_{gp} (for instance, 2 *nm*), the ON-state current decreases as shown in Fig. 14. The reduction in I_{ON} can be attributed to the reduced energy window available for BTBT at the source-channel interface. Hence, the optimum $d_{gp} \approx 6\ nm$ results in fully suppressed I_{AMB}, reduced I_{OFF}. However, it should be noted that the addition of GP does not impact the ON-state current for optimum d_{gp} (i.e., $d_{gp} = 6\ nm$). Additionally, it is worthy to note that in a TFET, the subthreshold swing depends on V_{GS} in contrast to a MOSFET. When V_{GS} is small, the subthreshold swing is very small (the drain current rises steeply) and as the V_{GS} is increased, the subthreshold swing increases (the drain current rises gently). The addition of GP does not impact the subthreshold characteristics as evident from Fig. 14.

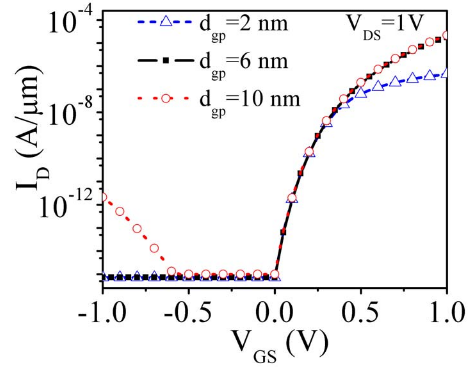

FIGURE 14. Transfer characteristics of GP-TFET at different d_{gp}.

TABLE 2. Comparison of ambipolar behaviour of GP-TFET with other reported techniques in literature [11].

Device Structure	L_G (nm)	N_D (atoms/cm^3)	V_{DD} (V)	I_{AMB} $(A/\mu m)$	$V_{OFF,2}$ (V)
Asymmetric TFET [10], [20]	100	5×10^{18}	1	5×10^{-8}	-0.2
Gate-Drain Overlap [14]	50	1×10^{19}	1	10^{-9}	-0.5
HDB TFET [15]	50	5×10^{18}	1	10^{-13}	-0.8
Non-uniform drain-doped TFET [28]	100	1.5×10^{19} and 1×10^{20}	1	6×10^{-7}	-0.1
DP-DGTFET [11]	100	1×10^{20}	1	10^{-14}	-1
This work	20	5×10^{18}	1	10^{-15}	-1

The ambipolar performance of the GP-TFET is compared with respect to the other reported techniques in Table 2 [11]. The distinguishing advantage of the GP-TFET is that it can fully suppress the I_{AMB} at maximum negative gate bias,

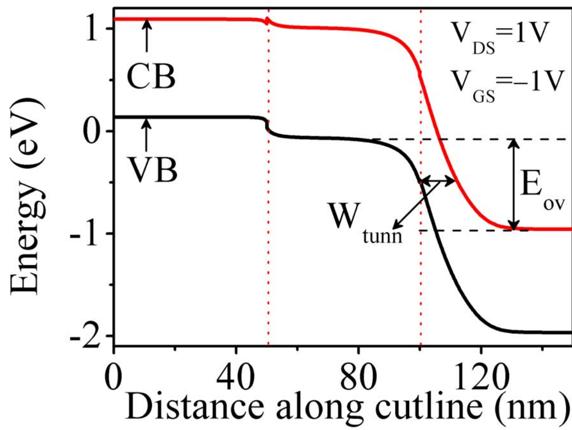

FIGURE 15. Illustration of W_{tunn} and E_{ov} in a GP-TFET (band diagram along RR').

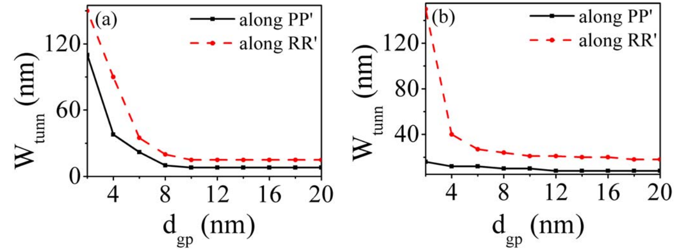

FIGURE 16. W_{tunn} vs d_{gp} at $V_{GS} = -V_{DD}$ and $V_{DS} = V_{DD}$ for (a) $t_{si} = 10\ nm$ (b) $t_{si} = 20\ nm$.

i.e., $V_{OFF,2} = -V_{DD}$. Moreover, the suppression of ambipolar current can be achieved at smaller gate lengths also, which can be attributed to the scalability of the GP-TFET as demonstrated in the previous section.

V. MECHANISM OF SUPPRESSION OF AMBIPOLAR CURRENT IN GP-TFET

In a GP-TFET, as mentioned above, when the d_{gp} is decreased, the drain becomes more depleted of the carriers, and the ambipolar current is suppressed. In this section, we examine the mechanism of suppression of the ambipolar current (I_{AMB}) in more detail. The tunneling current in a TFET primarily depends on two parameters: [7]

1) Tunneling barrier width (W_{tunn})
2) Energy band overlap (E_{ov})

These parameters are illustrated in Fig. 15. When W_{tunn} is small or E_{ov} is large, then more tunneling current flows in a TFET. These parameters are modulated by the existence of the GP, and the combined effect of these modulations suppresses the I_{AMB}, as described in the following paragraphs [7], [29].

A. IMPACT OF GP ON W_{TUNN}

In a TFET, an unwanted tunneling occurs at the drain-channel interface in the ambipolar mode ($V_{GS} = -V_{DD}$ and $V_{DS} = V_{DD}$). For the full suppression of the ambipolar current, the drain throughout its thickness (represented by t_{drain} in Fig. 1), should be depleted. In GP-TFETs with small silicon body thickness such as $t_{si} = 10\ nm$, addition of the GP results in depletion of the drain throughout its thickness. Thus, an increase in the W_{tunn} at the top (along cutline PP'), as well as, at the bottom (along the cutline RR') is observed, as shown in Fig. 16(a). This results in full suppression of I_{AMB} for $d_{gp} \leq 6\ nm$ (as already shown in Fig. 14).

Further, it should be noted that the thickness of the silicon body also plays an important role in deciding whether the complete drain along its thickness is depleted. For instance, if the thickness of the silicon body (t_{si}) is 20 nm, then though the W_{tunn} is increased at the bottom of the drain (along cutline RR'), it is not increased at the top of the drain (along cutline PP') even for $d_{gp} < 6\ nm$, as illustrated in Fig. 16(b). As a result, the ambipolar current in a GP-TFET with $t_{si} = 20\ nm$ is $8 \times 10^{-10} A/\mu m$ even at $d_{gp} = 6\ nm$ in contrast to $1 \times 10^{-15} A/\mu m$ for $t_{si} = 10\ nm$ at $d_{gp} = 6\ nm$.

B. IMPACT OF GP ON E_{OV}

The addition of GP decreases the energy band overlap (E_{ov}) at the drain-channel interface. As the GP is brought closer to the drain, the band overlap decreases further. In Fig. 17, the decrease in the energy band overlap (ΔE_{ov}) extracted using device simulations is shown. The ΔE_{ov} is defined as Eq. (4):

$$\Delta E_{ov} = E_{ov,20} - E_{ov} \tag{4}$$

where, $E_{ov,20}$ is the energy band overlap at $d_{gp} = 20\ nm$ and E_{ov} is the energy band overlap at a given d_{gp}. It can be noticed that with the decrease in the d_{gp}, the impact of the GP becomes prominent and ΔE_{ov} increases. The increase in ΔE_{ov} can be attributed to the modulation in the potential in the drain due to the application of the GP. As the d_{gp} is decreased, the potential in the drain (ψ_d) is modulated and the bands in the drain move upwards, resulting in an increase in ΔE_{ov}. The ψ_d in the drain, which is depleted of the carriers, can be computed as follows [30]:

$$\psi_d = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{DD} - V_{FB})}\right)^2 \tag{5}$$

where, $\gamma = \frac{\sqrt{2q\epsilon_s N_D} d_{gp}}{\epsilon_{ox}}$, ϵ_{ox}= permittivity of silicon dioxide, ϵ_s= permittivity of silicon and V_{FB}=flat band voltage.

In Fig. 17, the ψ_d (with respect to ψ_d at $d_{gp} = 20\ nm$) computed using Eq. (5), is also shown. The trend of ψ_d and ΔE_{ov} with respect to d_{gp} is showing a good match. Since, Eq. (5) is a very simplistic model, the mismatch in ψ_d and ΔE_{ov} are expected. However, Fig. 17 illustrates that decrease in the band overlap (ΔE_{ov}) in GP-TFET can be attributed to the modulation of the potential in the drain ψ_d. Since the decrease in the energy band overlap suppresses tunneling, this analysis shows that the decrease in ΔE_{ov} due to the

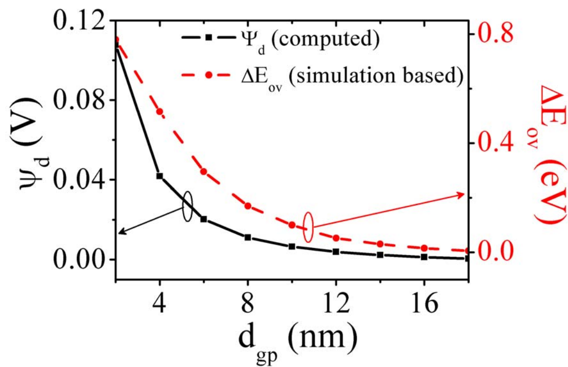

FIGURE 17. Trend of variation of ψ_d and ΔE_{ov} w.r.t d_{gp} at $V_{GS} = -V_{DD}$ and $V_{DS} = V_{DD}$.

existence of the GP contributes to the suppression in the ambipolar current in a GP-TFET.

VI. CONCLUSION

In this paper, using 2-D simulations, we have demonstrated that including the ground plane in the buried oxide at an appropriate depth in an SOI-TFET improves the scalability, mitigate the problem of ambipolar conduction and is helpful in ameliorating the short-channel effects. The proposed technique highlights the importance of depleting the drain of the majority carriers as an effective technique to suppress the direct source-to-drain tunneling in the short-channel TFETs. Therefore, interesting attributes of the GP-based TFETs are worth experimenting.

REFERENCES

[1] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007. doi: 10.1109/LED.2007.901273.

[2] A. Tura and J. C. S. Woo, "Performance comparison of silicon steep subthreshold FETs," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1362–1368, Jun. 2010. doi: 10.1109/TED.2010.2047066.

[3] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010. doi: 10.1109/JPROC.2010.2070470.

[4] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011. doi: 10.1038/nature10679.

[5] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-Art," *J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014. doi: 10.1109/JEDS.2014.2326622.

[6] J. Wu and Y. Taur, "Reduction of TFET OFF-current and subthreshold swing by lightly doped drain," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3342–3345, Aug. 2016. doi: 10.1109/TED.2016.2577589.

[7] S. Saurabh and M. J. Kumar, *Fundamentals of Tunnel Field-Effect Transistors*. New York, NY, USA: CRC Press, 2016. doi: 10.1201/9781315367354.

[8] D. H. Morris, U. E. Avci, R. Rios, and I. A. Young, "Design of low voltage tunneling-FET logic circuits considering asymmetric conduction characteristics," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 4, no. 4, pp. 380–388, Dec. 2014. doi: 10.1109/JETCAS.2014.2361054.

[9] U. E. Avci, D. H. Morris, and I. A. Young, "Tunnel field-effect transistors: Prospects and challenges," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 88–95, May 2015. doi: 10.1109/JEDS.2015.2390591.

[10] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-*k* gate dielectric," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007. doi: 10.1109/TED.2007.899389.

[11] S. Garg and S. Saurabh, "Suppression of ambipolar current in tunnel FETs using drain-pocket: Proposal and analysis," *Superlattices Microstruct.*, vol. 113, pp. 261–270, Jan. 2018. doi: 10.1016/j.spmi.2017.11.002.

[12] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Tunnel field-effect transistor without gate-drain overlap," *Appl. Phys. Lett.*, vol. 91, no. 5, Jul. 2007, Art. no. 053102. doi: 10.1063/1.2757593.

[13] C. Anghel, Hraziia, A. Gupta, A. Amara, and A. Vladimirescu, "30-nm tunnel FET with improved performance and reduced ambipolar current," *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1649–1654, Jun. 2011. doi: 10.1109/TED.2011.2128320.

[14] D. B. Abdi and M. J. Kumar, "Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain," *IEEE J. Electron Devices Soc.*, vol. 2, no. 6, pp. 187–190, Nov. 2014. doi: 10.1109/JEDS.2014.2327626.

[15] S. Sahay and M. J. Kumar, "Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using heterodielectric BOX," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3882–3886, Nov. 2015. doi: 10.1109/TED.2015.2478955.

[16] S. Kumar *et al.*, "2-D analytical modeling of the electrical characteristics of dual-material double-gate TFETS with a SiO_2/HfO_2 stacked gate-oxide structure," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 960–968, Mar. 2017. doi: 10.1109/TED.2017.2656630.

[17] J. Wu, J. Min, and Y. Taur, "Short-channel effects in tunnel FETs," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3019–3024, Sep. 2015. doi: 10.1109/TED.2015.2458977.

[18] K. Boucart and A. M. Ionescu, "Length scaling of the double-gate tunnel FET with high-K gate dielectric," *Solid-State Electron.*, vol. 51, nos. 11–12, pp. 1500–1507, Nov./Dec. 2007. doi: 10.1016/j.sse.2007.09.014.

[19] M. J. Kumar and M. Siva, "The ground plane in buried oxide for controlling short-channel effects in nanoscale SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1554–1557, Jun. 2008. doi: 10.1109/TED.2008.922859.

[20] S. Saurabh and M. J. Kumar, "Novel attributes of a dual material gate nanoscale tunnel field-effect transistor," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 404–410, Feb. 2011. doi: 10.1109/TED.2010.2093142.

[21] B. R. Raad, S. Tirkey, D. Sharma, and P. Kondekar, "A new design approach of dopingless tunnel FET for enhancement of device characteristics," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1830–1836, Apr. 2017. doi: 10.1109/TED.2017.2672640.

[22] I. Y. Yang, A. Lochtefeld, and D. A. Antoniadis, "Silicon-on-insulator-with-active-substrate (SOIAS) technology," in *Proc. IEEE Int. SOI Conf.*, 1996, pp. 106–107. doi: 10.1109/SOI.1996.552516.

[23] I. Y. Yang, C. Vieri, A. Chandrakasan, and D. A. Antoniadis, "Back-gated CMOS on SOIAS for dynamic threshold voltage control," *IEEE Trans. Electron Devices*, vol. 44, no. 5, pp. 822–831, May 1997. doi: 10.1109/16.568045.

[24] Silvaco. (2015). *Atlas User's Manual*. [Online]. Available: http://www.silvaco.com

[25] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, "Quantum-mechanical effects on the threshold voltage of ultrathin-SOI nMOSFETs," *IEEE Electron Device Lett.*, vol. 14, no. 12, pp. 569–571, Dec. 1993. doi: 10.1109/55.260792.

[26] M. J. Kumar and S. Janardhanan, "Doping-less tunnel field effect transistor: Design and investigation," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3285–3290, Oct. 2013. doi: 10.1109/TED.2013.2276888.

[27] A. K. Jain, S. Sahay, and M. J. Kumar, "Controlling L-BTBT in emerging Nanotube FETs using dual-material gate," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 611–621, Apr. 2018. doi: 10.1109/JEDS.2018.2829633.

[28] E. Baravelli, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "TFET inverters with n-/p-devices on the same technology platform for low-voltage/low-power applications," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 473–478, Feb. 2014. doi: 10.1109/TED.2013.2294792.

[29] K.-F. You and C.-Y. Wu, "A new quasi-2-D model for hot-carrier band-to-band tunneling current," *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1174–1179, Jun. 1999. doi: 10.1109/16.766880.

[30] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*. New York, NY, USA: Oxford Univ. Press, 2011.

SHELLY GARG received the B.Tech. degree in electronics and communication engineering from Northern India Engineering College, Indraprastha University, New Delhi, India, in 2013, and the M.Tech. degree in VLSI design from Indira Gandhi Delhi Technical University for Women (IGDTUW), New Delhi, in 2015. She is currently pursuing the Ph.D. degree with the Department of Electronics and Communication Engineering, IIIT Delhi, India. Her current research interests are in the areas of semiconductor devices and energy-efficient circuits. She was a recipient of the Vice-Chancellor Gold Medal for Securing First Position in M.Tech. at IGDTUW.

SNEH SAURABH received the B.Tech. degree in EE from IIT Kharagpur in 2000 and the Ph.D. degree from IIT Delhi in 2012. He has worked in the Semiconductor Industry for around 16 years. In 2016, he joined IIIT Delhi, where he is an Assistant Professor with the Department of Electronics and Communication Engineering. His current research interests are in the areas of nanoelectronics, exploratory electronic devices and energy-efficient systems.