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Process Dependence of Soft Errors Induced by Alpha Particles, Heavy Ions, and High Energy Neutrons on Flip Flops in FDSOI

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ABSTRACT Soft-error tolerance depending on threshold voltage of transistors was evaluated by α-particle, heavy-ion, and neutron irradiation. Three chips were fabricated, one embeds low-threshold general-purpose (GP) transistors and the others embed high-threshold low-power (LP) transistors in a 65 nm fully depleted silicon on insulator (FDSOI) process. There were a few errors on LPDFFs (DFFs with LP transistors). Error probability (EP) of LPDFFs was 99.88% smaller than that of GPDFFs (DFFs with GP transistors) by α particles. Average cross sections (CSs) of LPDFFs by heavy ions were 50% smaller than those of GPDFFs. Average soft-error rates (SERs) of LPDFFs by neutrons were 68% smaller than those of GPDFFs. 3-D device simulations revealed that CSs of the LP and GP transistors are changed by fitting methods using the work function of the gate material and doping concentration of the substrate under the BOX layer. The difference is due to the number of carriers in diffusion and silicon thickness of the raised layer above drain and source terminals.

INDEX TERMS Soft error, α particle, neutron, heavy ion, FDSOI, flip flop, TCAD simulations, threshold voltage.

I. INTRODUCTION

Reliability issues have become a significant concern with technology downscaling such as temporal failures and aging degradation [1]. Soft errors are one of temporal failures that flip stored values in storage cells caused by α particles, neutrons and heavy ions. α particle is a radioactive particle originated from a package material. Neutrons are generated by nuclear reactions between cosmic rays and the atmosphere air. In outer space, heavy ions are dominant to cause failures. A flipped storage value can be recovered by rebooting or rewriting. However, it is a serious issue especially for critical devices dealing with human life or social infrastructures. In device level, the fully-depleted silicon on insulator (FDSOI) structure can suppress soft errors. FDSOI has 50x - 100x higher tolerance for soft errors than bulk because the buried-oxide (BOX) layer prevents charge from being collected from substrate [2].

The threshold voltage of thin BOX FDSOI transistors is generally controlled by the work function of the gate material and doping concentration of the substrate under the BOX layer [3].

Semiconductor chips for low power must reduce leakage current. Low-power operation is mandatory for numerously-distributed Internet of Things (IoTs) driven by battery. It is hard to reboot hang-up devices manually. Thus it is important to prolong operation time of IoT devices by increasing reliability.

We evaluated soft-error tolerance of several chips including low-threshold general-purpose (GP) and high-threshold low-power (LP) transistors in a 65 nm thin BOX FDSOI.

This paper is based on a paper entitled "Threshold Dependence of Soft-Errors induced by α particles and Heavy Ions on Flip Flops in a 65 nm Thin BOX FDSOI" presented

TABLE 1. Normalized EP and CS in a 28 nm bulk process [4].

FF	V_{th}	EP	CS				
			O	Ne	Ar	Cu	Xe
DFF	standard	1	1	1	1	1	1
	low	1.04	0.94	1.00	1.14	1.12	0.95
	high	1.03	1.06	0.85	1.07	0.96	1.00

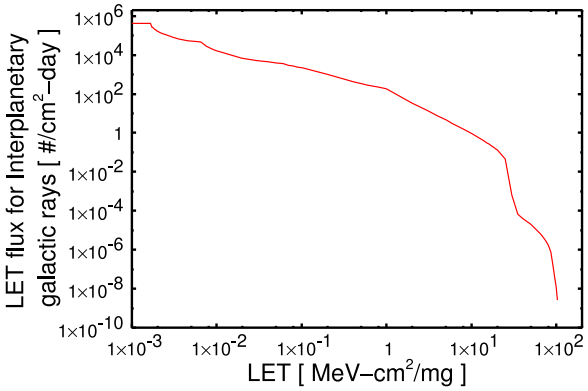

FIGURE 1. LET distribution of heavy ions in outer space [6].

at the 2018 IEEE S3S Conference. This paper has been supplemented by experimental results from spallation neutron irradiation and 3D device simulation results to reproduce heavy-ion irradiation.

Section II explains related works. Section III explains experimental results of fabricated chips including GP and LP transistors by α particle, heavy-ion and neutron irradiation. We explain simulation results in Section IV. Section V discusses inconsistency between measurement and simulation results. We conclude this paper in Section VI.

II. RELATED WORKS

Reference [4] evaluates soft-error tolerance of flip flops (FFs) with low, standard and high threshold transistors of a 28 nm bulk process. Table 1 shows the normalized error probability (EP) by α particles and cross section (CS) by O, Ne, Ar, Cu, and Xe irradiation. EP is calculated using Eq. (1). CS is equal to an area of upsets when a particle passes a storage cell [5]. Equation (2) shows how to calculate CS.

$$\mathrm{EP} = \frac{N_{\mathrm{error}}}{N_{\mathrm{FF}}} \tag{1}$$

$$\mathrm{CS}\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{N_{\mathrm{ion}} \times N_{\mathrm{FF}}} \tag{2}$$

N_{error} is the total number of errors by neutrons or heavy ions. N_{ion} is fluence that is the number of heavy ions per cm^2. N_{FF} is the number of FFs. The linear energy transfer (LET) is the amount of energy that an ionizing particle transfers to the material traversed per unit distance. Figure 1 shows the existence probability of heavy ions in outer space [6]. The number of particles with over 40 MeV-cm^2/mg is much less than that with less than 40 MeV-cm^2/mg in outer space [6]. Table 1 are the measurement results by heavy-ion irradiation. The irradiated ions are O, Ne, Ar, Cu and Xe with LET of 2.2, 3.5, 9.7, 21.2 and 58.8 MeV-cm^2/mg respectively.

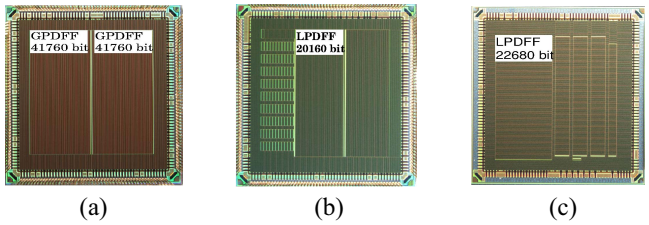

FIGURE 2. Fabricated chip micrographs including GPDFFs and LPDFFs. (a) Chip in GP. (b) Chip in LP. (c) Chip in LP.

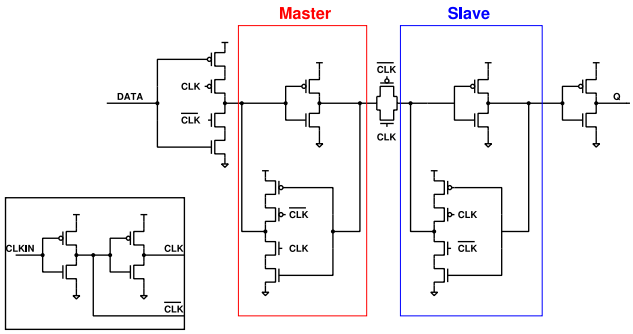

FIGURE 3. DFF structure.

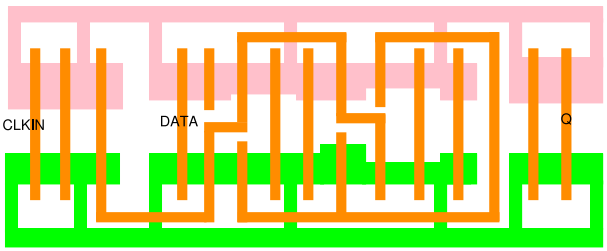

FIGURE 4. Simplified layout of DFF.

As a result, the soft-error rates of them were within 15% difference.

In the bulk process, the main cause of soft errors is the charge collection to drain by drift and funneling from substrate. It is independent or weakly dependent on threshold voltage. However, in the FDSOI process generated carriers in substrate cannot go to drain. Transistor characteristics such as threshold voltage, doping concentration and transistor structures may affect soft-error resilience.

III. EXPERIMENTAL RESULTS

A. EXPERIMENTAL SETUP

Three chips were fabricated in the 65 nm thin BOX FDSOI process with 12 nm SOI and 10 nm BOX layers in order to evaluate their soft-error tolerance [7]. Figure 2 show the chip micrographs that contain 83,520 bit GPDFFs (DFFs with GP transistors), 20,160 bit LPDFFs (DFFs with LP transistors), and 22,680 bit LPDFFs respectively. Figures 3 and 4 show the structure and the simplified layout of the standard DFF embedded in the three chips. We evaluated soft-error tolerance of chip (a) and (b) by α-particle and heavy-ion irradiation. Soft-error tolerance of chip (a) and (c) were also evaluated by neutron irradiation. Figure 5 shows the

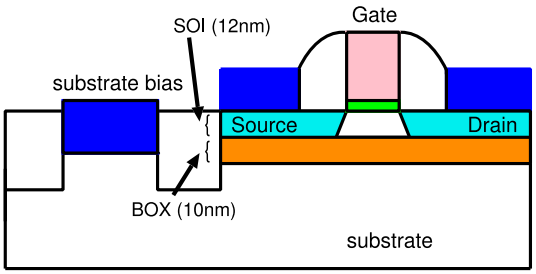

FIGURE 5. Cross sectional view of Thin BOX FDSOI.

TABLE 2. LET, energy, fluence of heavy ions.

Ion	Ar	Kr
LET [MeV-cm^2/mg]	17.5	40.9
Energy [MeV]	107	230
Fluence on GP transistors [n/cm^2]	2.62×10^6	2.44×10^6
Fluence on LP transistors [n/cm^2]	2.75×10^6	2.88×10^6

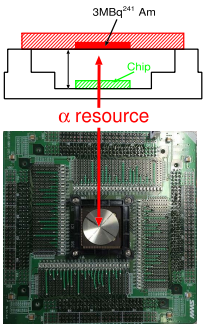

FIGURE 6. α-particle irradiation setup.

cross section of an NMOS transistor in the 65 nm thin-BOX FDSOI process [7].

α-particle irradiation tests were conducted using a 3 MBq ^{241}Am source. Each irradiation time was 300 sec. and irradiation was repeated for 10 times. Figure 6 shows an experimental setup of the α-particle irradiation test.

Heavy-ion irradiation tests were conducted by Ar and Kr ions at Takasaki Ion accelerators for Advanced Radiation Application (TIARA), Japan. Figure 7 shows the experimental setup of the heavy-ion irradiation tests. Device under tests (DUTs) are sealed in the chamber in order not to attenuate ion energy. Each irradiation time was 30 sec. and irradiation was repeated for 5 times. Table 2 shows LET, energy and average fluences of heavy ions.

Spallation neutron tests were conducted at the research center for nuclear physics (RCNP), Osaka University, Japan [8]. Figure 8 shows the experimental setup of neutron irradiation tests. Figure 9 shows the normalized neutron beam spectrum in comparison with the terrestrial neutron spectrum at the sea level in New York City (NYC). The average acceleration factor (AF) is 3.7×10^8 in average compared with the sea level in NYC. In order to increase the number of upset FFs within a limited time, five stacked DUT boards with two test chips were exposed to the neutron beam. 10 chips were measured simultaneously. Each irradiation time was 300 sec.

FIGURE 7. Heavy-ion irradiation setup.

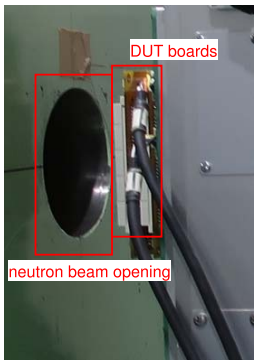

FIGURE 8. Spallation neutron irradiation setup.

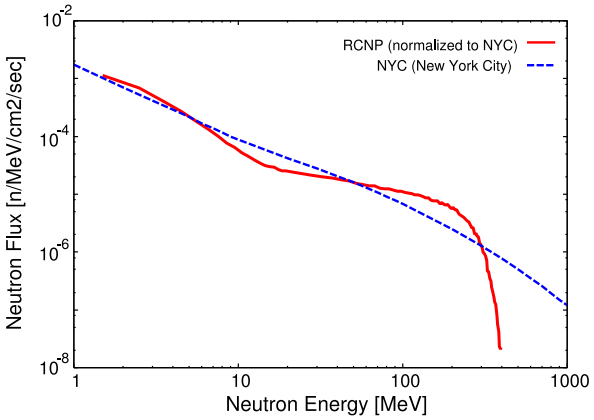

FIGURE 9. Normalized energy spectrum of spallation neutron beam at RCNP and neutron at the sea level of NYC.

and irradiation was repeated for 43 times. Soft-error rates (SERs) are calculated using Eq. (3).

$$SER\ [\mathrm{FIT/Mbit}] = \frac{N_{\mathrm{error}} \times 10^9\ \mathrm{h} \times 1024^2\ \mathrm{bit}}{300\ \mathrm{sec}/3600\ \mathrm{sec} \times AF \times N_{\mathrm{FF}}} \quad (3)$$

Irradiation was done at static conditions of (DATA, CLK) = (0,0), (0,1), (1,0), and (1,1). The supply voltage (V_{dd}) was 0.8 V by α-particle and heavy-ion irradiation. There was no error on LPDFFs at V_{dd} of 0.8 V

TABLE 3. Average numbers of upsets and total numbers of FFs on GPDFFs and LPDFFs in the 65 nm thin-BOX FDSOI process by α particles.

chip (FF)	(DATA,CLK)				average
	(0,1)	(1,1)	(0,0)	(1,0)	
GP (a) (83520 bit)	1449.9	108.9	8.9	960.4	632.0
LP (b) (20160 bit)	0.1	0.1	0	0	0.05

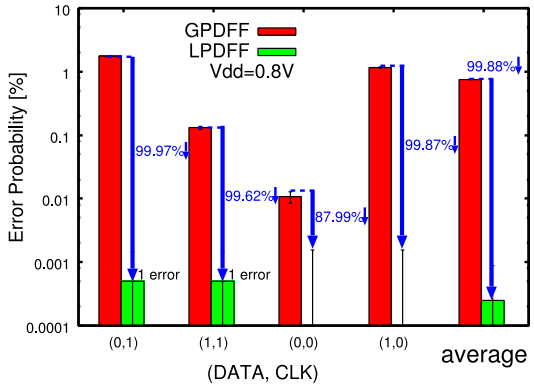

FIGURE 10. Error probability by α particle.

TABLE 4. Average numbers of upsets and total numbers of FFs on GPDFFs and LPDFFs in the 65 nm thin-BOX FDSOI process by Ar and Kr irradiation.

Ion	chip (FF)	(DATA,CLK)				average
		(0,1)	(1,1)	(0,0)	(1,0)	
Ar	GP (a) (83520 bit)	285.8	141.2	144.8	167.4	148.8
	LP (b) (20160 bit)	29.0	23.0	21.2	20.2	23.4
Kr	GP (a) (83520 bit)	473.0	156.4	162.4	271.6	265.9
	LP (b) (20160 bit)	55.0	32.4	28.2	27.2	35.7

by neutrons. In order to increase errors on LPDFFs, V_{dd} of GPDFF was 0.8 V and that of LPDFF was 0.6 V by neutron irradiation because the SERs increase as V_{dd} decreases [9]. Irradiation procedures were as follows.

1) Initialize serially-connected FFs by all 0 or all 1
2) Stabilize CLKIN to 0 or 1
3) Expose α particles, heavy ions or neutrons
4) Read out stored data of FFs
5) Count the number of upsets
6) Repeat 1) - 5) for four (DATA, CLK) conditions.

B. MEASUREMENT RESULTS

Table 3 shows the average numbers of upsets on GPDFFs and LPDFFs by α particles. The results of GPDFFs are quoted from [10]. Figure 10 shows the experimental results by α particles. The error bars are 95% confidence. LPDFFs are stronger against soft errors than GPDFFs at all static conditions. There are no error or a few errors on LPDFFs at all static conditions.

Table 4 shows the average numbers of upsets on GPDFFs and LPDFFs by Ar and Kr. Figures 11 and 12 show the experimental results by Ar and Kr with error bars of 95% confidence. LPDFFs are stronger against soft errors than GPDFFs at all static conditions. These results clearly reveal that the average CSs of LPDFFs are 50% and 54% smaller than those of GPDFFs by Ar and Kr respectively.

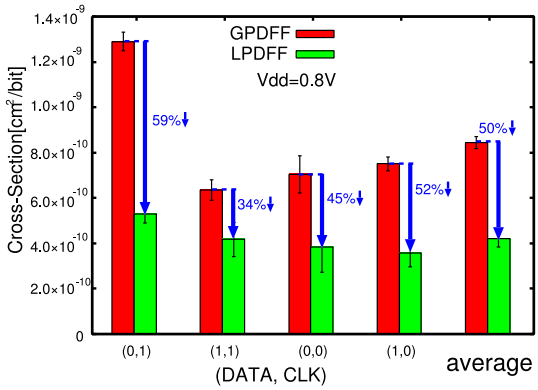

FIGURE 11. CSs by Ar irradiation.

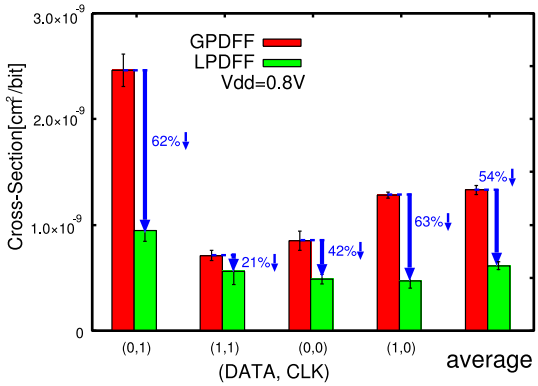

FIGURE 12. CSs by Kr irradiation.

TABLE 5. Average numbers of upsets and total numbers of FFs on GPDFFs and LPDFFs in the 65 nm thin-BOX FDSOI process by neutrons.

chip (FF) (Vdd)	(DATA,CLK)				average
	(0,1)	(1,1)	(0,0)	(1,0)	
GP (83520 bit) (0.8 V)	1.95	0.4	0.65	1.65	1.16
LP (22680 bit) (0.6 V)	0.23	0.09	0.09	0.05	0.12

Table 5 and Fig. 13 show the average numbers of upsets and SER on GPDFFs and LPDFFs by neutrons. The error bars are 95% confidence. LPDFFs are stronger against soft errors than GPDFFs at all static conditions. The average SER of LPDFFs is 68% smaller than that of GPDFFs by neutron irradiation.

Results from α-particle, neutron and heavy-ion irradiation in the FDSOI process prove that LPDFFs are stronger against soft errors than GPDFFs.

IV. SIMULATION RESULTS

Table 6 shows normalized leakage current, threshold voltage and D-Q delay of FFs with the GP and LP transistors in the 65 nm thin BOX FDSOI process by circuit simulations. Figure 14 show the current-voltage (Ids-Vgs) curve of the GP and LP transistors by circuit simulations. Leakage current of the LP transistors is 99% lower than that of the GP transistors. The LP transistors are suitable for IoT devices that are working periodically for a long battery life.

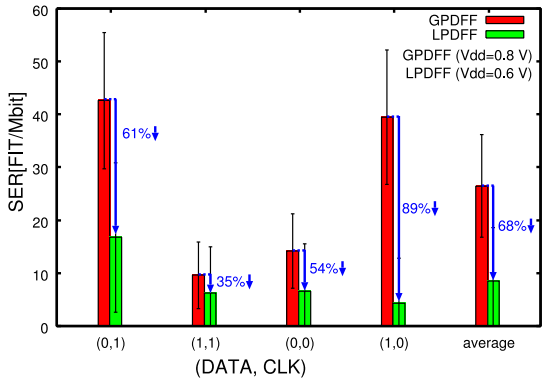

FIGURE 13. SERs by neutrons.

TABLE 6. Normalization of leakage current, threshold-voltage and D-Q delay of FF about GP and LP transistors.

	GP	LP
Threshold-Voltage	1	1.31
Leakage current	1	0.008
D-Q Delay of FF	1	1.64

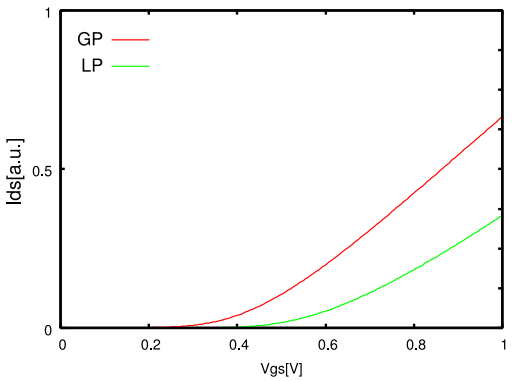

FIGURE 14. Ids-Vgs curve of GP and LP transistors on circuit simulations.

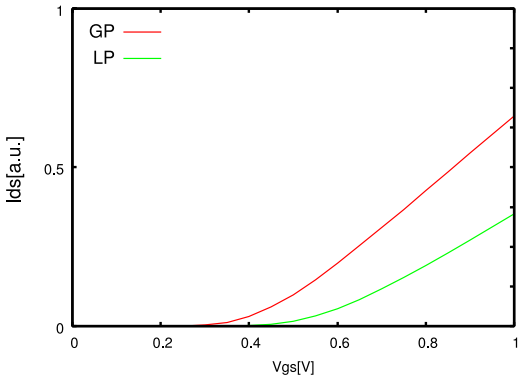

FIGURE 15. Ids-Vgs curve of GP and LP transistors on 3D device simulations. They are adjusted to the models on circuit simulations by changing the gate work function and the doping concentration under the BOX layer in substrate.

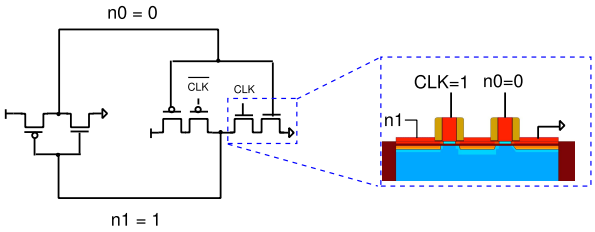

FIGURE 16. Latch on device and circuit simulations. NMOS of the tristate inverter is implemented by 3D device model. Other transistors are in a circuit level.

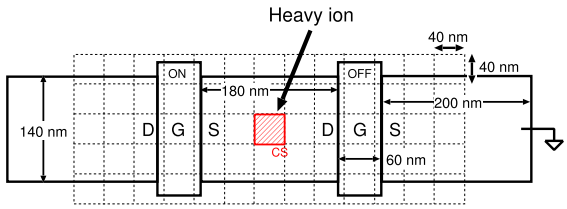

FIGURE 17. Top view of the 3D device model to evaluate CS on the tristate invertor.

We carried out three dimensional TCAD simulations using Synopsys Sentaurus to evaluate radiation hardness of the latch in Fig. 16 with the GP and LP transistors constructed in the 65 nm FDSOI process. Figure 15 shows the Ids-Vgs curve of the GP and LP transistors on 3D device simulations. The Ids-Vgs curve of those transistors are adjusted to the models on circuit simulations by changing the work function of gate material and the doping concentration in substrate under the BOX layer. The channel doping is equal on both types of transistors. The doping concentration in the channel is influenced by ion implantation under the BOX layer in substrate. But the influence to transistor characteristics is limited. Thus we ignore the influence. Those adjusted the LP and GP transistors are used in TCAD simulations to evaluate CSs.

The structure of the latch is equivalent to that of the master latch of the standard DFF. Soft-error tolerance of the latch at V_{dd} of 0.8 V is evaluated. The initial values of n0, n1 and CLK are set to 0, 1 and 1 respectively. The two NMOS transistors in the tristate inverter are implemented by 3D device models, while the other transistors are in the circuit level.

It has been revealed that NMOS transistors are weaker against soft errors than PMOS transistors mainly due to the difference of the mobility [11], [12]. We evaluated CS by hitting Ar (LET = 17.5 MeV-cm^2/mg) and Kr (LET = 40.9 MeV-cm^2/mg) vertically on NMOS region. Figure 17 shows a top view of the 3D device model to evaluate CS on the tristate invertor. The width of the tristate inverter and that in the fabricated chips are both 140 nm. A heavy ion hits every 40 nm grid. If a heavy ion makes the latch flip at a point, the 40 nm $\times$ 40 nm square region around the hit point is included in CS.

In this simulation, the following physical conditions were validated: Mobility (Doping Dependence, High Field Saturation, Enormal), Fermi, Effective Intrinsic Density (Old Slotboom), Recombination (Shockley Read Hall, Auger).

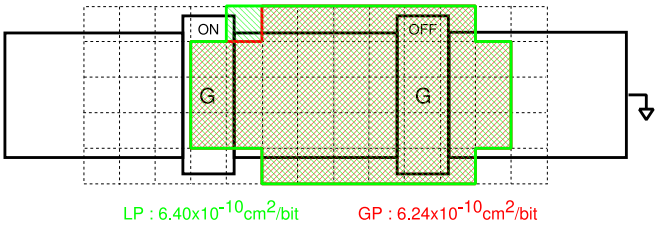

FIGURE 18. CS of GP and LP transistors in the tristate inverter by Ar ion irradiation.

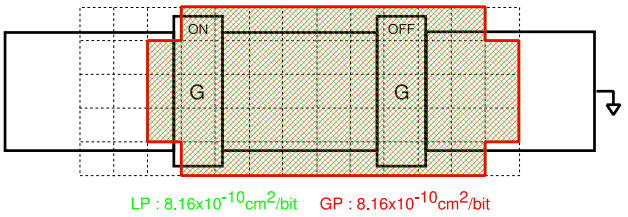

FIGURE 19. CS of GP and LP transistors in the tristate inverter by Kr ion irradiation.

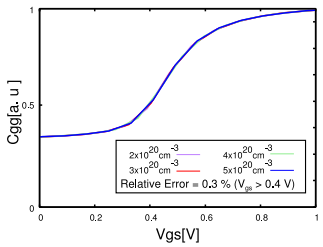

FIGURE 20. Cgg-Vgs curve of LP transistor by changing doping concentration in diffusion.

Figures 18 and 19 show the results of CS of the tristate inverter with the GP and LP transistors by Ar and Kr irradiation respectively. CS of the GP transistors is 3% smaller than that of the LP transistors by Ar ion. CSs with the LP and GP transistors are same by Kr ion. The GP transistors become stronger against soft errors than the LP transistors by 3D device simulations.

V. DISCUSSIONS

The measurement results were inconsistent to the simulation results. Our assumption is that it is due to the difference of the number of carriers in diffusion on GP and LP transistors. Equation (4) expresses auger recombination originated from electrons and holes. It is in proportion to the cube of the number of carriers.

$$R_{\text{auger}} = C_{\text{n}} n\left(np - {n_{\text{i}}}^2\right) + C_{\text{p}} p\left(np - {n_{\text{i}}}^2\right) \tag{4}$$

C_{n} and C_{p} are the constants of auger recombination. n and p are the electron and the hole density. n_{i} is the intrinsic carrier density.

The number of carriers collected in diffusion depends on doping concentration, which affects soft-error tolerance. The larger the rate of auger recombination is, the smaller CS becomes. Capacitance-voltage (Cgg-Vgs) and Ids-Vgs curves

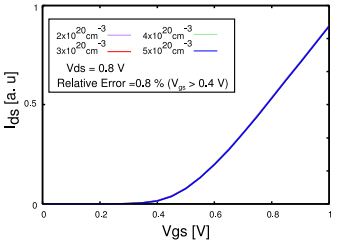

FIGURE 21. Ids-Vgs curve of LP transistor by changing doping concentration in diffusion.

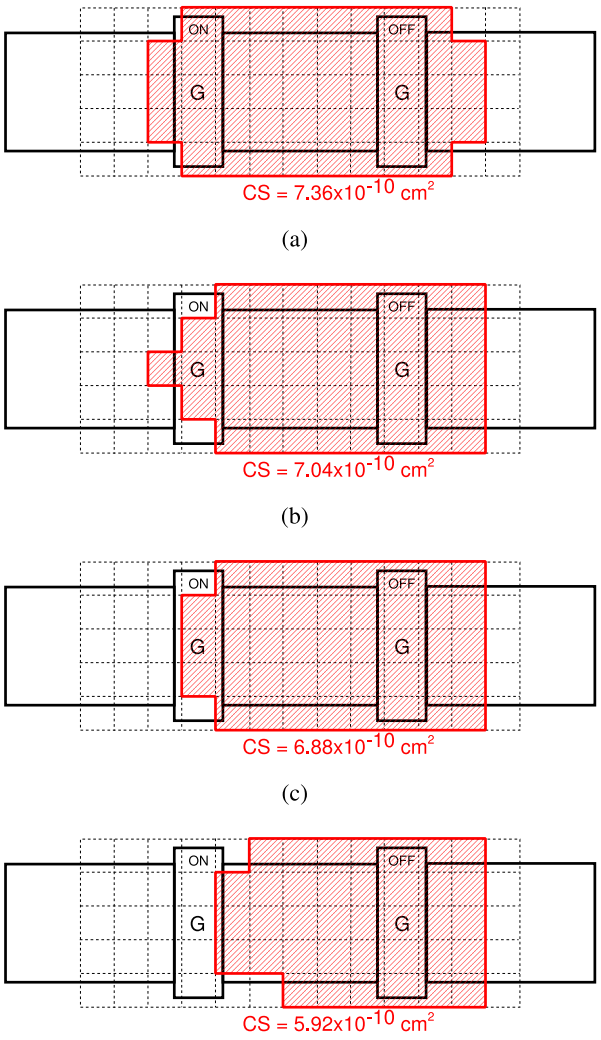

FIGURE 22. Transition of CS by changing doping concentration in diffusion. (a) 1×10^{20} cm^{-3} (b) 2×10^{20} cm^{-3} (c) 3×10^{20} cm^{-3} (d) 4×10^{20} cm^{-3}.

of the transistor are drawn by TCAD simulations by changing doping concentration. From the results in Figs. 20 and 21, doping concentration in diffusion has a small impact on transistor performance. We carried out TCAD simulations to see how soft-error tolerance is influenced by doping concentration in diffusion. CS by Ar ion irradiation computed

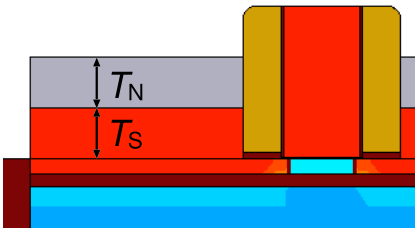

FIGURE 23. Structure of raised layer, definition of thickness of silicon (T_S) and thickness of nickel silicide (T_N) [13].

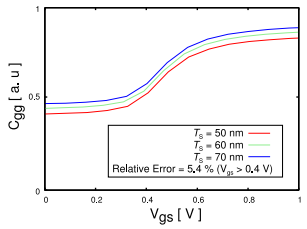

FIGURE 24. Cgg-Vgs curve of LP transistor by changing T_S in the raised layer.

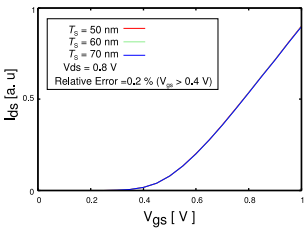

FIGURE 25. Ids-Vgs curve of LP transistor by changing T_S in the raised layer.

as the same manner as in Section IV. Doping concentration is changed from 1×10^{20} cm^{-3} to 4×10^{20} cm^{-3}.

Figure 22 show the results of CS when an Ar ion hits vertically on the NMOS region. CS is decreasing as increasing doping concentration. CS by 4×10^{20} cm^{-3} doping concentration in diffusion is 20% smaller than that by 1×10^{20} cm^{-3}.

For further discussions, silicon thickness (T_S) in the raised layer on the GP and LP transistors are parameterized on device simulations in Fig. 23 [13]. CS is evaluated by changing T_S in the raised layer from 50 nm to 70 nm with the doping concentration of 1×10^{20} cm^{-3}. From the results in Figs. 24 and 25 the raised layer has a small impact on transistor performance. CS at 50 nm T_S is 19.0% smaller than CS at 70 nm T_S.

Taking doping concentration in diffusion and T_S of the raised layer of LP and GP transistors into account, it is possible to reproduce the measurement results by device simulations.

VI. CONCLUSION

Soft-error tolerance of flip flops including low-threshold GP and high-threshold LP transistors in a 65 nm FDSOI process was evaluated by α particle, neutron and heavy-ion irradiation and 3D device simulations. At 0.8 V supply voltage (V_{dd}), the error probability of LPDFFs was 99.88% smaller than that of GPDFFs by α particle. The average CSs of LPDFFs were 50% and 54% smaller than those of GPDFFs by Ar and Kr ions respectively. There was no error on LPDFFs at V_{dd} of 0.8 V by neutron irradiation. In order to increase the number of errors on LPDFFs, V_{dd} of GPDFFs was 0.8 V and that of LPDFFs was 0.6 V. The average SER of the LPDFFs is 68% smaller than those of GPDFFs by neutrons. The 3D simulations revealed CS of GP transistors is 3% smaller than that of LP transistors by Ar ion. CSs with the LP and GP transistors are same by Kr ion.

The cause of the inconsistence between the measurement and simulation results by Ar ion is originated from the number of carriers in diffusion, the substrate under BOX layer and silicon thickness (T_S) of the raised layer over drain and source terminals. CS on the tristate inverter with LP transistors of 4×10^{20} cm^{-3} doping concentration becomes 20% smaller than that of 1×10^{20} cm^{-3}. CS at 50 nm T_S is 19.0% smaller than CS at 70 nm T_S.

Considering doping concentration in diffusion and silicon thickness of the raised layer of LP and GP transistors, the simulation results become closer to the measurement results.

LPDFF has smaller leakage current and is stronger against soft errors than GPDFF on FDSOI. FDSOI achieves both of low power and radiation hardness by using high-threshold transistors which are adequate to IoT devices operated by battery and hard to reboot.

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