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Employing Drain-Bias Dependent Electrical Characteristics of Poly-Si TFTs to Improve Gray Level Control in Low Power AMOLED Displays

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ABSTRACT With development of high efficiency organic light emitting diodes (OLEDs), and high mobility polycrystalline silicon (poly-Si) thin-film transistors (TFTs), low power and high resolution active matrix OLED (AMOLED) displays are becoming popular for mobile applications. However, they suffer from poor control of lower gray levels, with the driving TFT being operated in the subthreshold regime. In this paper, with help of non-ideal drain-bias dependent electrical characteristics of poly-Si TFTs, operation of the driving TFT can be moved out from the subthreshold regime to allow better control of the gray levels. As a result, a dynamic voltage scaling (DVS) method is developed, and shown to be able to improve the luminous uniformity for better image quality, while effectively reducing the static power consumption.

INDEX TERMS Thin-film transistor, polycrystalline silicon (poly-Si), active matrix organic light emitting diode (AMOLED), low power.

I. INTRODUCTION

Active matrix organic light emitting diode (AMOLED) displays own a set of attractive features, such as a much thin and simple structure, being flexible, excellent contrast ratio, and ultra-fast response, for mobile and wearable applications [1], [2]. The simplest pixel circuit for AMOLED displays is composed of two thin-film transistors (TFTs) and one capacitor (2T1C) based on voltage driving as shown in Fig. 1(a). However, in such a simple configuration, the OLED current is very sensitive to performance variation of the driving TFT (T_2). Although the current driving approach is able to provide better tolerance, it suffers long sampling time especially in the lower gray levels with lower current. Therefore, for practical applications, more complicated voltage driving pixel circuits, such as the 6T1C one in Fig. 1(b), are required to compensate the process or operation induced luminance non-uniformity [3]–[5]. With significant improvement of luminance efficiency of OLEDs for low power and also reduction of pixel area for high resolution, the required largest pixel current has been continuously decreased and become less than 10^{-7} A for state-of-the-art mobile displays [6], [7]. Such low current levels would cause design challenges for gray level control. Since the switching TFTs need high mobility to realize fast refresh rate, the driving TFT in the same technology will be operated in the subthreshold regime for low current levels. It thus becomes challenging to finely define the lower gray levels, since a small data voltage fluctuation of several millivolts might cause current change more than one gray-level. Moreover, the compensation schemes used in AMOLED displays to suppress the luminance non-uniformity may not work properly when the driving TFT is operated in the subthreshold regime [7].

Meanwhile, as shown in Fig. 1(a), in conventional design, the power supply (V_{DD}-V_{SS}) is selected to accommodate the largest OLED current for the maximum luminance. For that, in addition to a voltage drop on the OLED (V_{OLED}), a large enough drain-to-source voltage of the driving TFT ($>V_{TFT}$) is also needed to allow the device to be operated in the saturation regime. However, at lower gray levels, the OLED voltage decreases, and the voltage over the TFT is larger than what is required, causing power loss [8]. To reduce the power loss, several approaches on dynamic scaling of the supply voltage according to the displayed gray

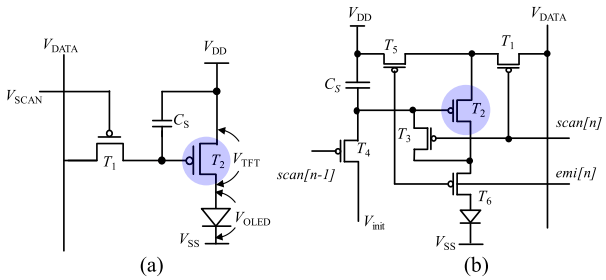

FIGURE 1. **(a) The simplest pixel circuit for AMOLED displays composed of two TFTs and one capacitor (2T1C). (b) The pixel circuit with compensation capability composed of six TFTs and one capacitor (6T1C). In both circuits, T_2 is driving TFT, and other TFTs function as switches.**

TABLE 1. **List of the model parameter values for fitting the experimental data based on the RPI poly-Si TFT model.**

Model Parameter	Values	Model Parameter	Values
V_{on} (V)	0	AT ($m \cdot V^{-1}$)	1×10^{-8}
V_{th} (V)	-1.9	BT ($m \cdot V^{-1}$)	0
VTO(V)	0	DELTA	4.0
V_{FB} (V)	0.1	VKINK (V)	9.1
MU0 ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	120	LKINK (m)	3.2×10^{-6}
MU1 ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	3×10^{-3}	I0 ($A \cdot m^{-1}$)	8.0
MUS ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	1.0	I00 ($A \cdot m^{-1}$)	9×10^{4}
MMU	4.2	BLK (mV)	1×10^{-3}
ASAT	1.05		

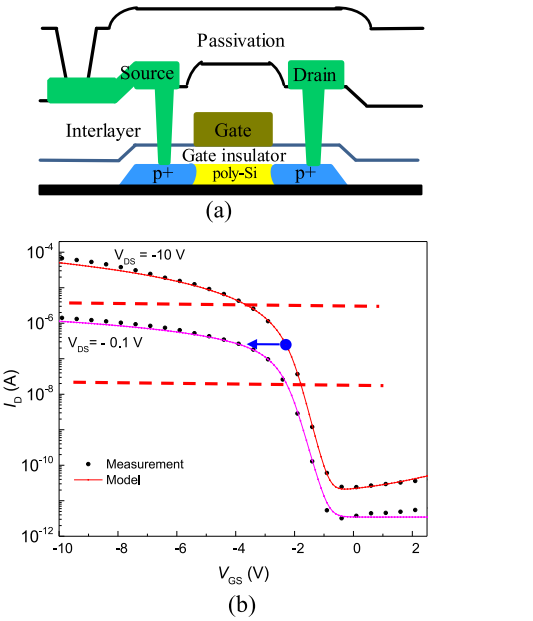

FIGURE 2. **(a) Illustration of the cross-sectional structure of the poly-Si TFT. (b) Fitting of the simulated transfer characteristics (I_D-V_{GS}) with the RPI poly-Si TFT model and the measurement results for a poly-Si TFT with a channel length of 10 μm and channel width of 10 μm.**

levels have been proposed [8]–[10]. For a TFT with ideal field effect transistor behaviors, if it is operated in subthreshold regime, such supply voltage scaling will not affect the current. However, due to presence of kink effect, poly-Si TFTs normally present drain-bias dependent electrical characteristics [11], [12]. Therefore, the drain bias change induced by supply voltage scaling will cause current change. Normally, such non-ideal electrical behaviors should be suppressed [13]–[15]. In this work, it is shown that, with the help of such drain-bias dependent electrical characteristics, operation of the driving TFT can be moved out from the subthreshold regime to allow better control of the gray levels. As a result, a dynamic voltage scaling (DVS) method is developed, and shown to be able to improve the luminous uniformity for better image quality, while reducing the static power consumption.

II. METHOD

A p-type poly-Si TFT fabricated using the industry standard processes is used in this study for describing the method. Its cross-sectional structure is depicted in Fig. 2(a) with a 300 nm thick silicon oxide as the gate insulator layer. Based on the RPI poly-Si TFT model [16], the simulated transfer characteristics (I_D-V_{GS}) can fit well with the measurement results for the device with a channel length of 10 μm and channel width of 10 μm as shown in Fig. 2(b). The extracted model parameter values are listed in Table 1.

It can be seen that the poly-Si TFT exhibits obvious drain bias dependent electrical characteristics in the subthreshold and near-subthreshold regimes due to the presence of kink effect. Normally, such characteristics are not desired and need to be suppressed for circuit applications [13]–[15]. Here, as shown in Fig. 2(b), with the help of such characteristics in the near-threshold regime, less negative drain-to-source voltage (V_{DS}) and more negative gate-to-source voltage (V_{GS}) can move the operation of the TFT from the subthreshold regime to the above-threshold regime while remaining the same current. In the above threshold regime, the current becomes less sensitive to the gate voltage fluctuation for better control of the gray scale, and the compensation scheme might also work better. Therefore, the drain-bias dependent electrical characteristics of poly-Si TFTs can be employed to develop a DVS scheme for addressing the issues of controlling lower gray scales in low power AMOLED displays. Scaling of V_{DS} and V_{GS} can be implemented through the supply voltage (V_{SS}) and the data voltage (V_{DATA}) of the pixel circuits, respectively, as shown in Fig. 1.

To verify the potential of the method for practical applications, it was implemented in FPGA (Xilinx AX7020) as depicted in Fig. 3. The pre-stored look-up tables in the memory with mapping between the gray level and I_{OLED}, I_{OLED} and V_{SS}, I_{OLED} and V_{DATA} for designed pixel circuits were obtained through measured data and circuit simulations. Based on these look-up tables, the DVS method in the FPGA can convert any input images or video streams into corresponding V_{SS} and V_{DATA} values for matrix of pixels. The generated V_{SS} and V_{DATA} values were used to reconstruct the images or video streams through MATLAB using the same look-up tables for image quality and power analysis. The reconstructed images based on the conventional

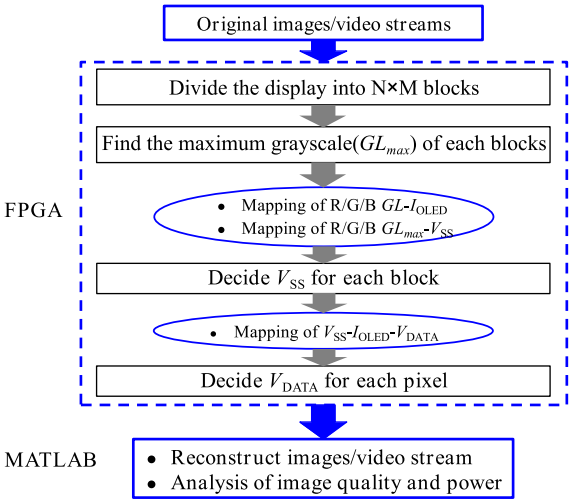

FIGURE 3. The flow for verification of the proposed method in display panels with FPGA and MATLAB.

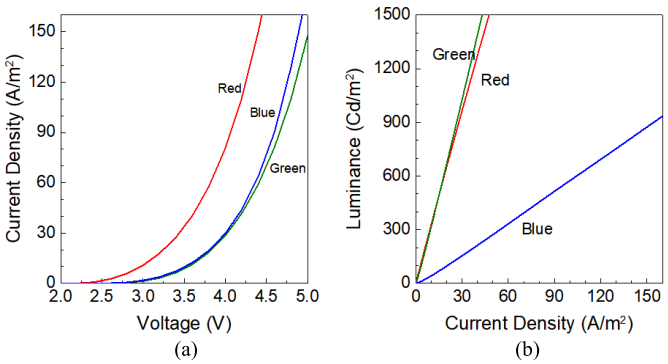

FIGURE 4. The measured (a) current density versus voltage and (b) brightness versus current density characteristics for the used red, green and blue OLEDs.

driving method without the DVS scheme were processed for comparisons.

A 420 dpi resolution display of 1080×1920 with a luminance of 500 cd/m^2 (D65 white light) and an aperture ratio of 50% is taken as an example for the study. Based on the characteristics of red (R), green (G) and blue (B) OLEDs in Fig. 4, the maximum currents for each sub-pixel are calculated to be 18.0 nA (R), 14.06 nA (G) and 127.9 nA (B), respectively. The whole display was divided into 40×48 blocks. Each block is composed of 27×40 pixels with V_{SS} being individually controlled. Both 2T-1C and 6T-1C pixel circuits as shown in Fig. 1 were designed with $W/L = 6$ μm/3 μm for the switching TFTs, and $W/L = 3$ μm/3 μm for the driving TFTs. The storage capacitor (C_S) was 0.3 pF. V_{DD} was fixed as 4.9 V, and V_{SS} varied.

III. RESULTS AND DISCUSSIONS

Circuit simulations based on the extracted RPI poly-Si TFT model were performed using the Smart-SPICE circuit simulator to obtain the relationships between the OLED current

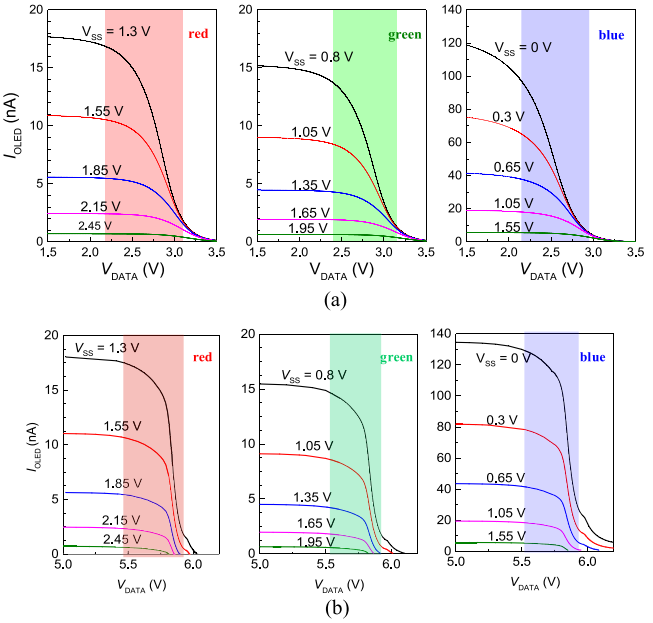

FIGURE 5. The simulated relationships of the OLED current with V_{DATA} at different V_{SS} for the red, green and blue pixels based on different pixel circuit designs: (a) 2T1C pixel circuit and (b) 6T1C pixel circuit.

and V_{DATA} at different V_{SS} for the R/G/B sub-pixels based on the two pixel circuit designs. Different V_{SS} values are selected to accommodate the required current levels, while having enough intervals. The simulation results are given in Fig. 5(a) and (b), respectively. It can be seen that, with increase of V_{SS} (e.g., decrease of V_{DD}-V_{SS} and thus less negative V_{DS}) and decrease of V_{DATA} (e.g., more negative V_{GS}) to achieve the same current levels, the dependence of OLED current on the V_{DATA} change becomes less sharp in the highlighted regions. When V_{DATA} decreases, $|V_{GS}|$ of the driving TFT increases, resulting in less resistive TFT. More voltage drop is then on the OLED, thus the current increases. However, the maximum current is limited by the supply voltage range (V_{DD}-V_{SS}). Therefore, when the V_{DATA} decreases to a certain value, the current starts to saturate, since most of V_{DD}-V_{SS} is on the OLED.

Assuming a V_{DATA} fluctuation of 20 mV, the resulted relative OLED current (I_{OLED}) errors at different current levels were obtained for R/G/B sub-pixels based on the 2T1C pixel circuit as shown in Fig. 6(a). The relative I_{OLED} error is defined as the ratio of the difference between the theoretical current and the actual current considering the V_{th} variation or V_{DATA} fluctuation over the theoretical current. It can be seen that, as the OLED current deceases, the relative I_{OLED} error increases due to the presence of V_{DATA} fluctuation, and scaling of V_{SS} can effectively reduce such current error. The simulation results in Fig. 6(b) show that, for the 6T1C pixel circuit with capability of compensating threshold voltage (V_{th}) variation, it still generates obvious current errors with presence of V_{th} variation of 0.2 V and

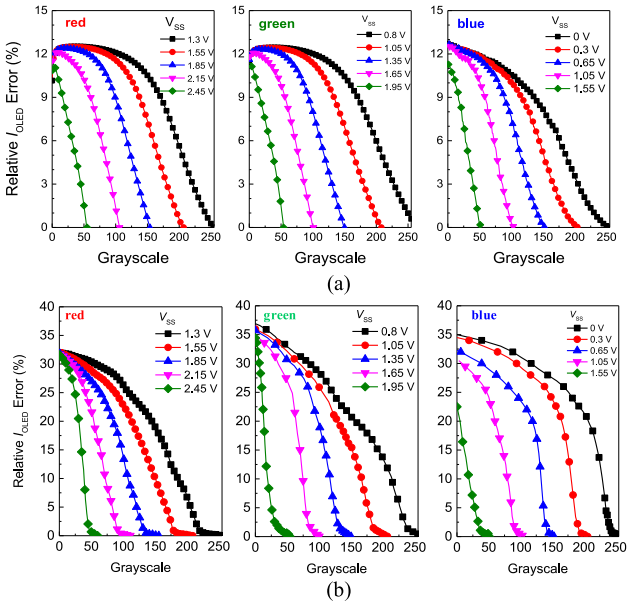

FIGURE 6. **(a) Simulated relative OLED current error at different OLED current levels for the 2T1C pixel circuit with scaling of V_{SS} and assuming only V_{DATA} fluctuation of 20 mV. (b) Simulated relative OLED current error at different OLED current levels for the 6T1C pixel circuit with scaling of V_{SS} and assuming both V_{th} variation of 0.2 V and V_{DATA} fluctuation of 20 mV.**

V_{DATA} fluctuation of 20 mV. Scaling of V_{SS} can also significantly reduce the resulted current errors. Based on these results, it can be concluded that with the drain dependent near-threshold characteristics in poly-Si TFTs, more accurate control of the lower gray levels can be achieved by scaling V_{SS} and V_{DATA}. Scaling of V_{SS} would also bring benefit of reducing the power loss on the driving TFTs at lower gray levels [8].

For various input images, the reconstructed images using the DVS approach with different pixel circuit designs were compared to those without DVS, as shown in Fig. 7. The structural similarity index (SSIM) was used to quantitatively measure the similarity between the reconstructed image and the original one [17]. SSIM=1 denotes no image distortion, and a lower value means poorer image quality. V_{DATA} fluctuation of 20 mV, and column to column V_{th} variation of 0.2 V simulating excimer laser annealing induced device performance variations are added in the study. It can be seen that the 2T1C pixel circuit is very sensitive to V_{th} variations, causing so called "mura" as expected with very low SSIM values. With DVS, the SSIM was lightly improved attributed to suppressed influence of V_{DATA} fluctuation. The 6T1C design with compensation capability can greatly improve the display quality with a much higher SSIM compared to the 2T1C one, but still shows certain non-uniformity. With the DVS approach, the display quality is further improved with high SSIM values around 0.95 being achieved for all test images. The results prove that the DVS method can effectively improve the display quality by suppressing the influence from V_{DATA} fluctuation and V_{th} variation.

FIGURE 7. **Comparison of the reconstructed images using the DVS approach with different pixel circuit designs for various input images. The structural similarity index (SSIM) values were obtained to quantitatively measure the similarity between the reconstructed images and the original ones.**

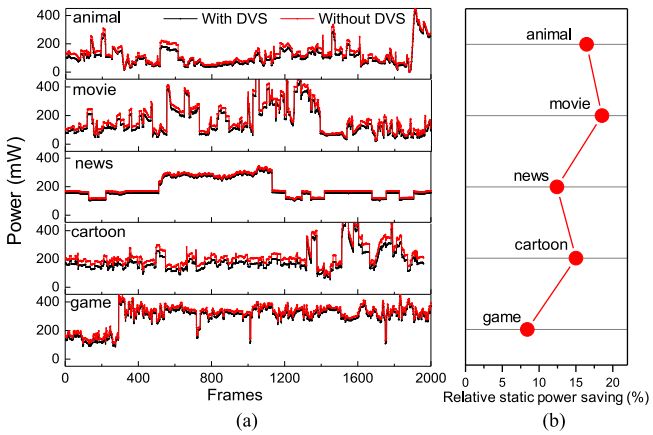

FIGURE 8. **(a) Static power consumption for each frame in various video flips with and without using the DVS approach. (b) The calculated relative static power saving with the sum of the power for all the frames of each video flip.**

The consumed static power for each frame in various video flips with and without using the DVS approach was calculated as a sum of $(V_{DD}\text{-}V_{SS})\times I_{OLED}$ for all the pixels, as shown in Fig. 8(a). With the sum of the power for all the frames, the relative static power saving was calculated to be about 8%-18%, depending on the video content (Fig. 8(b)).

Fig. 9 illustrates the possible way of implementing blocks of different V_{SS} in a display panel. Individual V_{SS} lines (R/G/B using different V_{SS} lines) are made to connect each block from the power supply through the source metal layer (Fig. 9(a)). In each block, the same color sub-pixels share the same V_{SS} through the interconnects on the gate metal layer and vias to the source metal layer, as shown in Fig. 9(b).

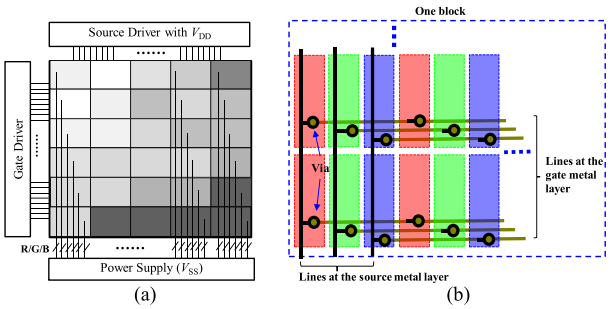

FIGURE 9. (a) Illustration of implementing blocks of different V_{SS} in a display panel with individual V_{SS} lines (R/G/B using different V_{SS} lines) connecting each block from the power supply. (b) In each block, the same color sub-pixels share the same V_{SS} through the interconnects on the gate metal layer and vias to the source metal layer.

This proves that physical implementation of such a DVS driving scheme in real display panels is possible.

IV. CONCLUSION

In summary, it is shown that, with help of the non-ideal drain-bias dependent electrical characteristics of poly-Si TFTs, operation of the driving TFT can be moved out from the subthreshold regime to allow better control of the gray levels for lower power AMOLED displays. By employing this feature, a DVS method is developed to improve the luminous uniformity for better image quality, while effectively reducing the static power consumption. Verification of the method with FPGA and MATLAB on both 2T-1C and 6T-1C pixel designs prove the potential of the method for practical applications. One of the remained issues with this DVS method is that the driving TFT operation might change from the saturation regime to the linear regime, causing current sensitivity to supply voltage fluctuations. Although the sensitivity would be less than that to the data voltage fluctuation in the subthreshold regime, the effect is worth further investigation.

REFERENCES

[1] J. Lee *et al.*, "5.8-inch QHD flexible AMOLED display with enhanced bendability of poly-Si TFTs," in *SID Tech. Dig.*, vol. 49, no. 1, May 2018, pp. 895–898. doi: 10.1002/sdtp.12247.
[2] N.-H. Keum *et al.*, "23-1: Distinquished student paper: An AMOLED pixel circuit for 1000 PPI and 5.87-inch mobile displays with AR and VR applications," in *SID Tech. Dig.*, vol. 49, no. 1, May 2018, pp. 283–286. doi: 10.1002/sdtp.12530.
[3] H.-K. Chung, Y.-W. Kim, C.-Y. Oh, O.-K. Kwon, and S.-M. Chio, "Organic light emitting device pixel circuit and driving method therefor," U.S. Patent 7 414 599 B2, Aug. 2008.
[4] W.-J. Wu, L. Zhou, R.-H. Yao, and J.-B. Peng, "A new voltage-programmed pixel circuit for enhancing the uniformity of AMOLED displays," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 931–933, Jul. 2011. doi: 10.1109/LED.2011.2148152.
[5] C.-L. Lin, W.-Y. Chang, C.-C. Hung, and C.-D. Tu, "LTPS-TFT pixel circuit to compensate for OLED luminance degradation in three-dimensional AMOLED display," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 700–702, May 2012. doi: 10.1109/LED.2012.2188270.
[6] T. Komoda, H. Sasabe, and J. Kido, "Current status of OLED material and process technologies for display and lighting," in *Proc. AM-FPD*, Jul. 2018, pp. 1–4. doi: 10.23919/AM-FPD.2018.8437406.
[7] X.-Y. Lin, Y.-H. Tai, C.-Y. Chang, and C.-W. Lu, "P-20: AMOLED driving circuit with subthreshold current compensating capability for high PPI display panel," in *SID Tech. Dig.*, vol. 47, no. 1, May 2016, pp. 1189–1192. doi: 10.1002/sdtp.10903.
[8] Q. Cui *et al.*, "P.16: Dynamic supply voltage scaling of pixel circuits for static power reduction in AMOLEDs," in *SID Tech. Dig.*, vol. 44, no. 1, Jun. 2013, pp. 1040–1043. doi: 10.1002/j.2168-0159.2013.tb06401.x.
[9] X. Chen, J. Zheng, Y. Chen, M. Zhao, and C. J. Xue, "Quality-retaining OLED dynamic voltage scaling for video streaming applications on mobile devices," in *Proc. Design Automation Conf.*, vol. 41, no. 3, Jul. 2012, pp. 1000–1005. doi: 10.1145/2228360.2228540.
[10] S. Hong, S.-W. Kim, and Y.-J. Kim, "LGC-DVS: Local gamma correction-based dynamic voltage scaling for android smartphones with AMOLED displays," *IEEE J. Electron Devices Soc.*, vol. 5, no. 6, pp. 432–444, Nov. 2017. doi: 10.1109/JEDS.2017.2745680.
[11] A. Valletta, P. Gaucci, L. Mariucci, G. Fortunato, and S. D. Brotherton, "Kink effect in short-channel polycrystalline silicon thin-film transistors," *Appl. Phys. Lett.*, vol. 85, no. 15, pp. 8113–8115, Oct. 2004. doi: 10.1063/1.1806252.
[12] K. W. Kim, J. Kang, H. Ku, K. Lee, and H. J. Kim, "Anomalous kink effect induced by bottom-shield-metal in LTPS TFTs on plastic substrates," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1524–1527, Oct. 2018. doi: 10.1109/LED.2018.2867942.
[13] T.-T. Chien *et al.*, "A high-current kink effect free Z-gate poly–Si thin-film transistor," *IEEE Electron Device Lett.*, vol. 37, no. 7, pp. 886–889, Jul. 2016. doi: 10.1109/LED.2016.2566959.
[14] T.-K. Kang *et al.*, "Reduction of kink effect of poly-Si TFT with bottom field plate by dispersing current density technique," *IEEE Trans. Electron Devices*, vol. 63, no. 7, pp. 2975–2979, Jul. 2016. doi: 10.1109/TED.2006.2563662.
[15] L. Mariucci *et al.*, "Polysilicon TFT structures for kink-effect suppression," *IEEE Trans. Electron Devices*, vol. 51, no. 7, pp. 1135–1142, Jul. 2004. doi: 10.1109/TED.2004.829860.
[16] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, "SPICE models for amorphous silicon and polysilicon thin film transistors," *J. ElectroChem. Soc.*, vol. 144, no. 8, pp. 2833–2839, May 1997. doi: 10.1149/1.1837903.
[17] Z. Wang, A. C. Bovik, H. R. Sheikh, and E. P. Simoncelli, "Image quality assessment: From error visibility to structural similarity," *IEEE Trans. Image Process.*, vol. 13, no. 4, pp. 600–612, Apr. 2004. doi: 10.1109/TIP.2003.819861.

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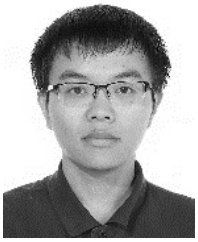

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