28-nm FDSOI nMOSFET RF Figures of Merits and Parasitic Elements Extraction at Cryogenic Temperature Down to 77 K

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ABSTRACT This paper presents detailed RF characterization of 28-nm FDSOI nMOSFETs at cryogenic temperatures down to 77 K. Two main RF figures of merit (FoM), i.e., current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}), as well as elements of small-signal equivalent circuit are extracted from the measured S-parameters. Increases of f_T and f_{max} by about 85 GHz and about 30 GHz, respectively, are demonstrated at 77 K. The observed behavior of RF FoMs versus temperature is discussed in terms of small-signal equivalent circuit elements, both intrinsic and extrinsic (parasitics). This paper suggests 28-nm FDSOI as a good candidate for future cryogenic applications.

INDEX TERMS FDSOI, UTBB MOSFETs, RF figures of merit (FoM), cryogenic temperature, parasitic elements.

I. INTRODUCTION

Motivation for the in-depth study of advanced technologies at cryogenic temperatures is two-fold: (i) space applications and (ii) control and read-out circuitry around quantum bits ("qubits") by an integrated control system [1]. The co-integration of the qubits and their control system can further reduce the thermal noise by removing the need for direct interconnections from the qubits to a control system operating at room temperature (RT). Thus, in a control system operating at cryogenic temperature, the analog/RF building blocks (multiplexers, low-noise amplifiers, oscillators etc.) should be designed in cryogenic CMOS electronics. As an advanced technology node, 28nm FDSOI is a good candidate for the design of these building blocks [2].

28nm FDSOI MOSFETs have already demonstrated improved DC, analog and RF performances at room temperature (RT) [3], [4]. Some previous works [2], [5], [6] analyzed the behavior of advanced MOSFETs at cryogenic temperatures. However, these works are mostly limited to static parameters (as short-channel effects, threshold voltage, subthreshold swing ...). Influence of cryogenic temperature

on 28 nm bulk and FDSOI devices with a main focus on analog parameters extraction and modelling has been discussed in [2], [5]. In [7], we investigated the properties of 28nm FDSOI transistors for cryogenic applications from DC to RF covering electrostatic, analog and RF figures of merit (FoM). We demonstrated strong improvement of transconductance (g_m) to drain current (I_d) ratio g_m/I_d, g_m, I_d, and cut-off frequency (f_T) at 77 K. However, in terms of RF performance that study was limited to f_T only. To our best knowledge there had been no extended studies of RF behavior of 28nm FDSOI MOSFETs at cryogenic temperatures. Our previous conference work [8] filled this gap and detailed cryogenic RF analysis of 28nm FDSOI process including f_{max} and equivalent circuit extraction. The present paper extends this work.

Firstly, RF Figures of Merit (FoMs) of nMOSFETs from 28nm FDSOI technology, with different gate lengths (L_g), are extracted in a temperature (T) range of 77-300 K. Then, our main focus is on the reconstruction of small-signal equivalent circuit of such UTBB MOSFET in a wide temperature range based on intrinsic and parasitic elements by which RF

FoMs are determined. Our conference work [8] is extended to include the effect of temperature lowering on the gate capacitances (intrinsic and extrinsic) as well as the channel conductance g_{ds}. Furthermore, the C_{gs}/C_{gd} ratio, as a measure of short channel effects, is investigated at RT and 77 K for different gate lengths. Additionally, the paper shows RF FoMs when MOSFET operates at low voltage conditions, with drain bias, down to $V_{ds} = 0.6$ V.

II. EXPERIMENTAL DETAILS

Devices studied in this work come from ST-M 28nm FDSOI process [9]. N-channel MOSFETs under study feature gate lengths (L_g) from 25 to 150 nm. The Si film, BOX and the equivalent gate oxide thicknesses are 7, 25 and 1.3 nm, respectively. More process details can be found in [9].

Studied nMOSFETs feature 60 fingers of 2 μm width, embedded in CPW pads for RF characterization. Lake Shore cryogenic probe station was used to extend DC I-V and RF S-parameters measurements temperature range from 300 K down to liquid nitrogen temperature of 77 K.

S-parameters are measured in a frequency range from 10 MHz up to 40 GHz under saturation ($V_{ds} = 1$ V and 0.6 V) and "cold" ($V_{ds} = 0$ V) conditions for different applied gate voltages (V_{gs}). The back gate was kept grounded. The CPW feed line pads are de-embedded by dedicated open structure for each device measured at every temperature.

## III. RESULTS AND DISCUSSION
A. RF FoMs
The two main RF FoMs, i.e., current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}), are obtained from extrapolation of H_{21} parameter and unilateral gain (ULG) to 0 dB, respectively, in saturation ($V_{ds} = 1$ V and 0.6 V) and at V_{gs} that corresponds to maximum g_m [3]. In this condition, the V_{th} variation is taken into account. The variation of these two RF FoMs versus (a) L_g and (b) T for $V_{ds} = 1$ V are shown in Figs. 1 and 2, respectively. This advanced technology node is known to feature high f_T and f_{max} reaching several hundreds of GHz at room temperature [3], [10]. As shown in Figs. 1 and 2, temperature reduction (from 300 K to 77 K) results in strong f_T and f_{max} improvements, by about 85 and 30 GHz (in a shortest device), respectively.

One can also note in Figs. 1b and 2b that f_T and f_{max} curves in the shortest device feature a maximum at ∼100 K and thus their improvement at 77 K is attenuated. This was discussed in our previous work [11] in terms of mobility (μ) and thus g_m behavior in such devices. This will be confirmed below by the extraction of intrinsic and extrinsic transconductances for the devices with different lengths and at various temperatures.

Fig. 3 shows f_T and f_{max} as a function of the gate length at 300 K and 77 K for the case of low V_{ds} of 0.6 V. Low voltage operation is indeed of high interest particularly for cryogenic operation where it is crucial to keep the heat
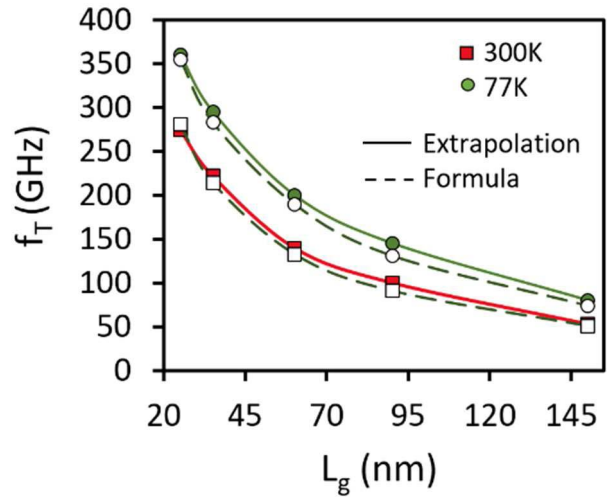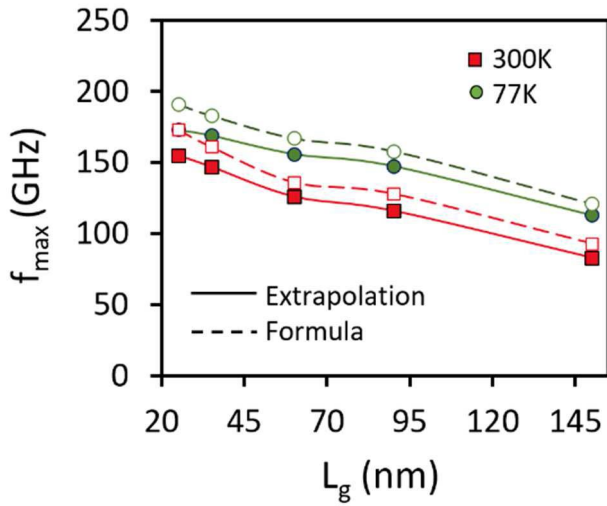

(a)
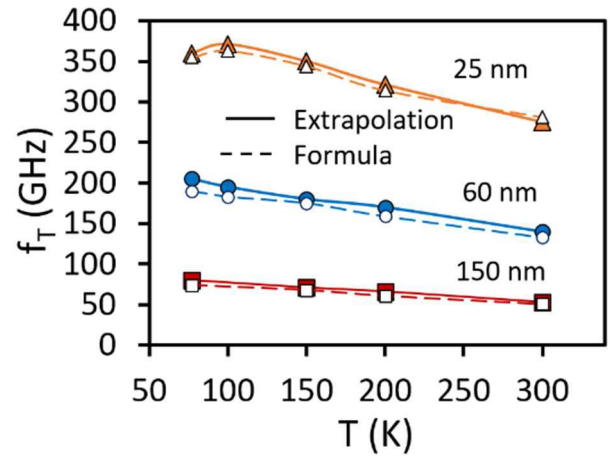
(b)

FIGURE 1. f_T vs. L_g for 77 K and 300 K (a) and vs. T for different L_g (b) by extrapolation (solid lines) and small-signal equivalent circuit extraction (dashed lines) in saturation for high V_{ds} ($V_{ds} = 1$ V) and at V_{gs} that corresponds to maximum g_m.

dissipation by the device itself as low as possible in order to not alter the ambience cryogenic temperature. One can see that even at $V_{ds} = 0.6$ V this technology allows for rather high $f_T \sim 240$ GHz and $f_{max} \sim 135$ GHz in shortest device at 300 K with further improvement up to $f_T \sim 323$ GHz and $f_{max} \sim 150$ GHz at 77 K proving the advantage of this technology for low-voltage cryogenic circuits.
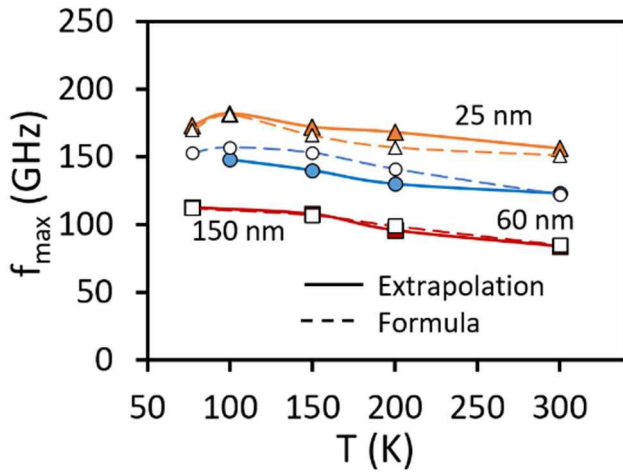
B. EXTRACTION OF SMALL-SIGNAL EQUIVALENT CIRCUIT ELEMENTS
Based on the MOSFET small-signal equivalent circuit shown in Fig. 4 (including intrinsic and parasitic elements), f_T and f_{max} are approximately expressed by Eqs. (1) and (2), respectively [12]:

$$f_T \approx \frac{g_{me}}{2\pi \left(C_{gs} + C_{gd} \right)} \quad (1)$$

(a)

(b)

FIGURE 2. f_max vs. L_g for 77 K and 300 K (a) and vs. T for different L_g (b) by extrapolation (solid lines) and small-signal equivalent circuit extraction (dashed lines) in saturation (V_ds = 1 V) and at V_gs that corresponds to maximum g_m.

FIGURE 3. f_T and f_max vs. L_g for 77 K and 300 K in saturation at low V_ds (V_ds = 0.6 V) and at V_gs that corresponds to maximum g_m.

FIGURE 4. RF model of FDSOI UTBB MOSFET small-signal equivalent circuit [3].

$$f_{max} \approx \frac{f_T}{2\sqrt{2\pi f_T R_g C_{gd} + (R_s + R_g)g_{ds}}} \quad (2)$$

Small-signal equivalent circuit elements were extracted from S-parameters measurements using the procedure explained in details in [3]. The intrinsic elements are extracted at the same bias condition as RF FoMs were obtained ($V_{ds} = 1$ V and V_{gs} at which maximum g_m is achievable. Extrinsic elements (e.g., parasitic capacitances, C_{gse}, C_{gde} and C_{dse}) and series resistances (R_s, R_d and R_g) are obtained in cold FET ($V_{ds} = 0$) at depletion and strong inversion regimes, respectively. Figs. 5–7 show variations of maximum intrinsic transconductance, g_{mi} (excluding source/drain resistance) and maximum extrinsic transconductance g_{me} (i.e., as measured including source/drain resistance), total gate capacitance ($C_{gg} = (C_{gdi} + C_{gde}) + (C_{gsi} + C_{gse})$) and both series source/drain and gate resistances (R_{sd} and R_g), respectively,
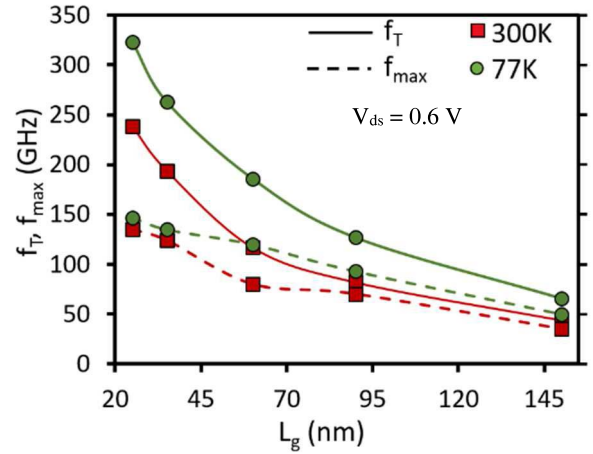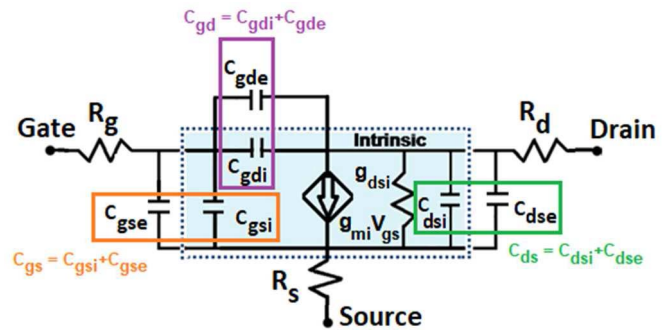
as a function of L_g at 300 K and 77 K (figures (a)) and as a function of T (figures (b)). Based on Eqs. (1) and (2), improvements of f_T and f_{max} with decreasing of L_g and T observed in Figs. 1 and 2 are directly correlated with increase of g_m (both by L_g and T reductions) and decrease of C_{gg} (by L_g reduction) as shown in Figs. 5 and 6.

Indeed, comparing Figs. 1, 2 and 5, based on Eqs. (1) and (2), one can observe similar trends in g_m, f_T and f_{max} improvements with T reduction. Furthermore, relative improvement both in g_m and f_T, f_{max} becomes smaller in the shortest device. As shown in Fig. 5b, for 25 nm device, improvement rate of both maximum "extrinsic", g_{me} (i.e., including R_{sd}), and maximum "intrinsic", g_{mi} (i.e., without R_{sd} effect) drops at 77 K exhibiting a maximum at ∼100 K similarly to RF FoMs shown in Figs. 1b and 2b. Temperature dependence of g_m can be treated in terms of μ temperature dependence and R_{sd} temperature dependence. The fact that both g_{me} and g_{mi} feature the same temperature trends suggests that R_{sd} temperature dependence can be excluded as a reason of those trends and explain them in terms of mobility variation. It is worth noting that maximum g_{me} and g_{mi} are achieved at about the same gate voltage overdrive (V_{gs}-V_{th}) for different T and thus about the same electric field.
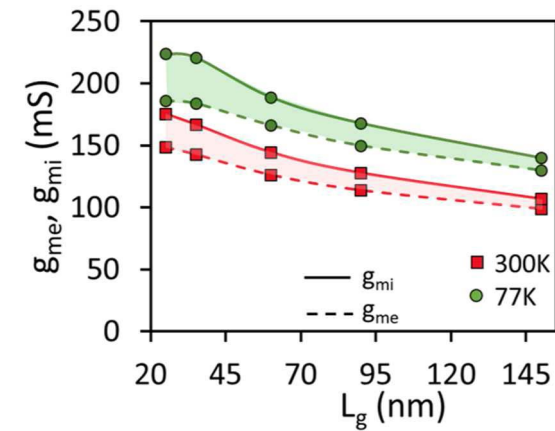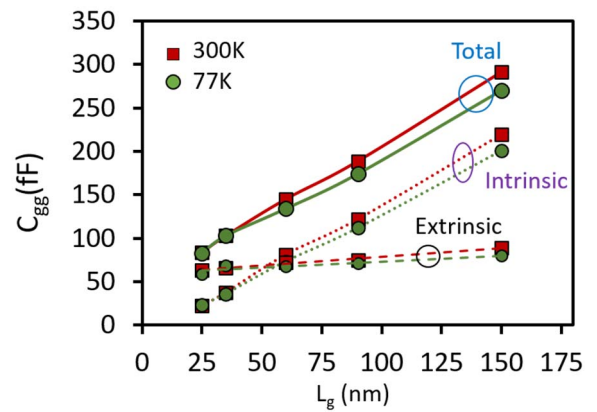
(a)
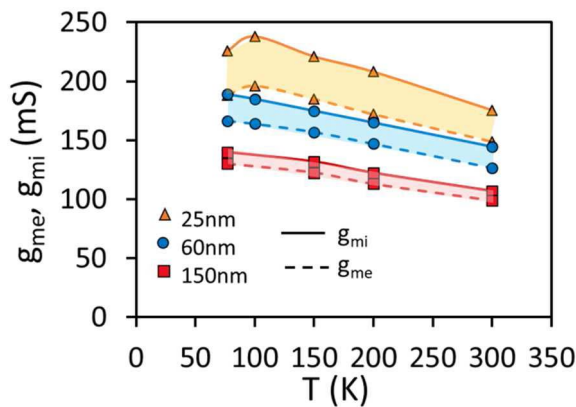
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FIGURE 5. Maximum g_{mi}, g_{me} vs. L_g for 77 K and 300 K(a) and vs. T for L_g = 25, 60 and 150 nm (b) in saturation (V_{ds} = 1 V) and at V_{gs} that corresponds to maximum g_m.

(a)

(b)

(c)

FIGURE 6. (a) Total, extrinsic and intrinsic gate capacitances C_{gg}, C_{gge} and C_{ggi} vs. L_g for 77 K and 300 K; (b) Total C_{gg} vs. T for L_g = 25, 60 and 150 nm. (c) Extrinsic (C_{gge}) and intrinsic (C_{ggi}) parts of the gate capacitances for L_g = 25, 60 and 150 nm. Extrinsic parts are extracted in cold and deep-depletion regime (V_{ds} = 0, $V_{gs} < V_{th}$) and intrinsic part in saturation (V_{ds} = 1 V) and at V_{gs} that corresponds to maximum g_m.
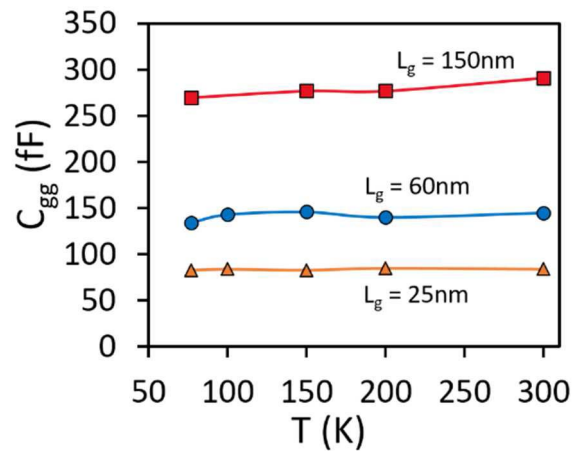
Therefore, observed g_{me} and g_{mi} trends versus temperature for different lengths are most probably related to the complex behavior of different mobility components as previously discussed in [7], [11].

Indeed, detailed studies of μ temperature behavior in devices with different lengths originated from such kind of process [6], [13] revealed the μ in short-channel devices is strongly degraded by the presence of process-induced defects in the extensions and near source/drain regions. Thus, resulting μ temperature dependence is defined through the balance between Coulomb scattering on the defects (with μ_c reduction with T lowering) and phonon scattering (with μ_{ph} increase with T lowering) [6], [7], [11], [13]. Detailed study of mobility in such kind of devices at different temperatures is out of scope of this paper and can be found in [6] and [13].
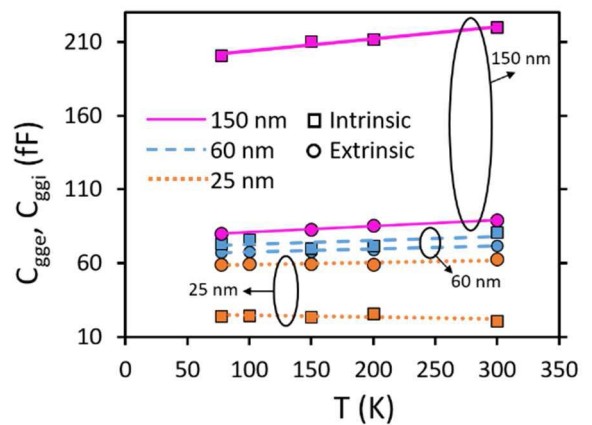
Next to that, R_{sd} can be seen to decrease slightly at 77 K (Fig. 6). The extracted R_{sd} is composed by different components, such as raised source/drain highly doped regions, metal-semiconductor contacts, metallic interconnection lines and vias. They were shown to feature a reduction of resistance at low temperatures [15]–[17], which might dominate overall R_{sd} temperature behavior in our case. Furthermore, it is worth emphasizing that the observed R_{sd} reduction lies close to the limit of extraction precision.
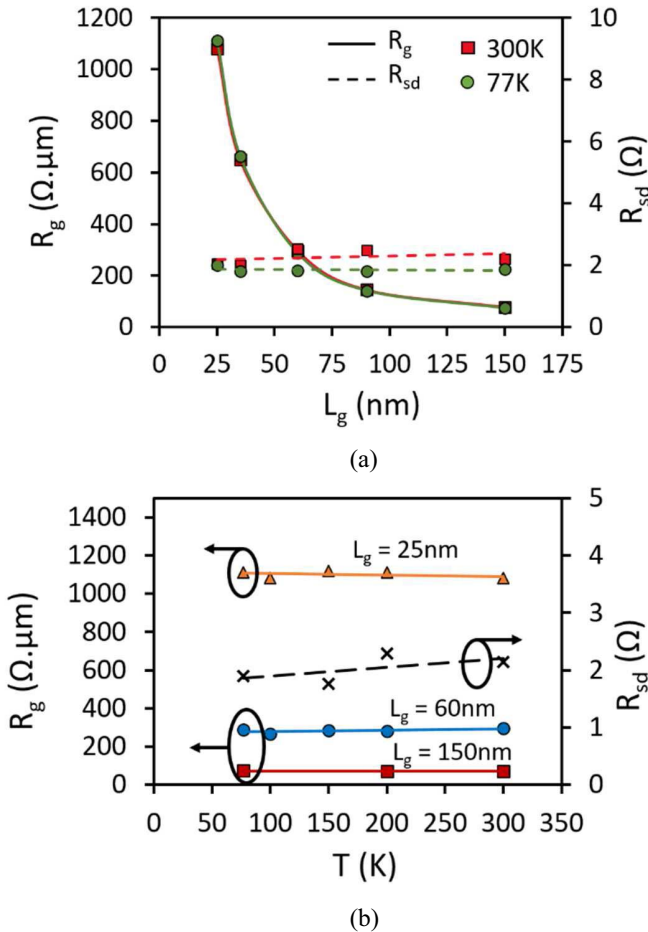
(a)

(b)

FIGURE 7. R_g, R_{sd} versus (a) L_g at 77 K and 300 K and (b) T for L_g = 25, 60 and 150 nm extracted from Bracal method [14].

FIGURE 8. C_{gs}/C_{gd} ratio versus L_g at 300 K and 77 K in saturation (V_{ds} = 1 V) and at V_{gs} that corresponds to maximum g_m.

FIGURE 9. Channel conductance g_{ds} and intrinsic gain A_v versus gate length L_g at 77 K and 300 K in saturation (V_{ds} = 1 V) and at V_{gs} that corresponds to maximum g_m.

As a result of very slight R_{sd} variation with T, Fig. 5b shows almost constant difference between g_{me} and g_{mi} for each length from 300 K down to 77 K. Nevertheless, the effect of R_{sd} in shorter devices is more pronounced and visible (via larger difference between g_{me} and g_{mi}) as these devices feature higher intrinsic g_m and current levels.

Comparing Fig. 1 and Fig. 2, one can see that f_{max} is lower than f_T, except for long-channel devices, similarly to our previous room-temperature observations in [3]. This is due to the gate resistance (R_g) which increases dramatically in shorter devices (Fig. 7a). T lowering down to 77 K has almost no effect on this trend. This is because gate stacked materials behavior remains unchanged by T lowering down to 77 K as shown in Fig. 7b.

Fig. 6a-c detail length and temperature dependences of "intrinsic" and "extrinsic" parts of total gate capacitance, C_{ggi} and C_{gge}, respectively. It is seen that the intrinsic part of total gate capacitance decreases proportionally with L_g reduction, whereas its extrinsic part stays almost unchanged for different L_g, so that C_{gge} dominates over C_{ggi} in short devices. From this figure, one can observe that both intrinsic and extrinsic parts are almost temperature independent which
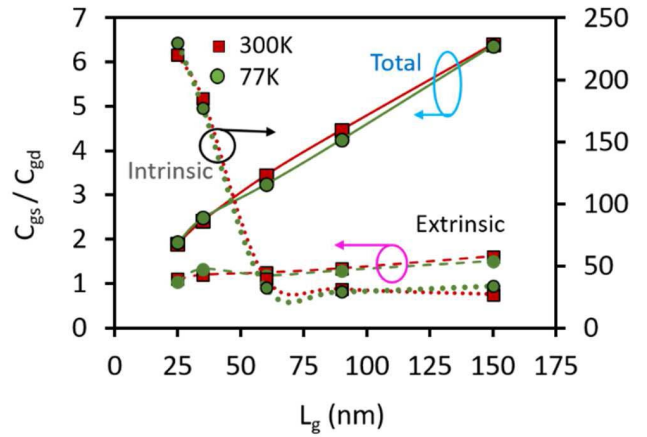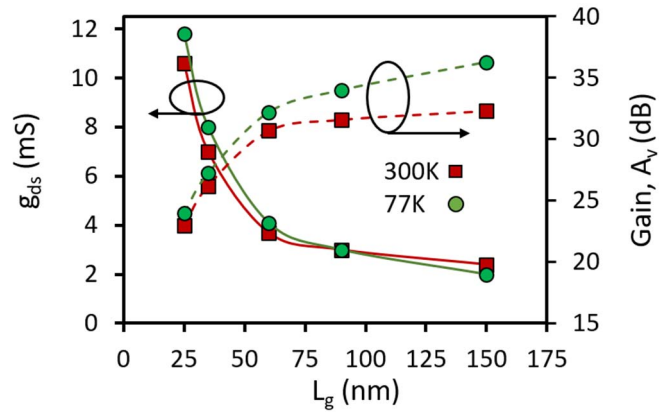
result in total gate capacitance temperature independency. The critical L_g at which C_{gge} dominates over C_{ggi} stays also almost invariable with temperature reduction.

The ratio C_{gs}/C_{gd} versus L_g for 300 K and 77 K is shown in Fig. 8. This ratio is one of the metrics used to measure (or assess) short channel effects in scaled transistors. One can see that, as expected, C_{gs}/C_{gd} decreases in shorter devices It can be seen that temperature lowering down to 77 K has almost no impact on this parameter which correlates with very weak (if any) temperature dependence of DIBL in 77 K-300 K range shown in [11].

In Fig. 9, the variation of channel conductance g_{ds} and intrinsic gain (A_v = g_{me} / g_{ds}) versus gate length at 77 K and 300 K are demonstrated. As expected, g_{ds} increases dramatically in shorter devices. One can observe that very slight effect of T reduction on g_{ds} starts to appear in devices shorter that 90 nm. Consequently, slight attenuation of f_{max} improvement at cryogenic temperature can be expected in shorter devices (see Eq. (2)). On the other hand, g_m (and f_T)
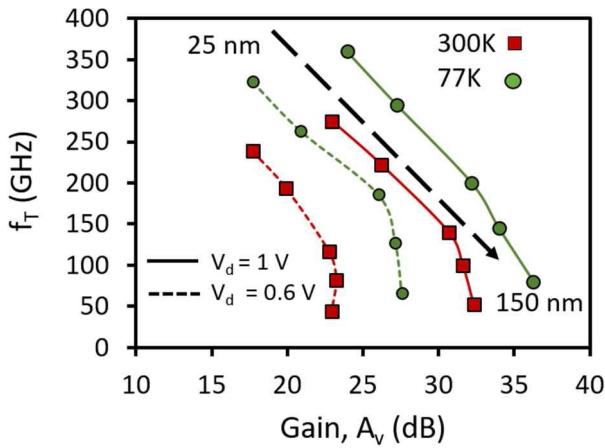
FIGURE 10. f_T versus intrinsic gain A_v for L_g = 25, 35, 60, 90 and 150 nm at V_{ds} = 1 V (solid line) and 0.6 V (dashed line) at 300 K and 77 K.

improvement is much stronger than g_{ds} degradation, and thus both f_{max} and gain are improving [11].

Fig. 10 plots f_T as a function of intrinsic gain extracted from S-parameters for V_{ds} of 0.6 and 1 V for the devices with various gate lengths. One can see that temperature reduction results in simultaneous f_T and gain improvements. This correlates with our previous findings on g_m-A_v temperature trends based on dc extractions [11].

To support the above analysis in terms of equivalent circuit elements, f_T and f_{max} were re-calculated based on Eqs. (1) and (2) using extracted parasitic and intrinsic elements and shown in Figs. 1 and 2. One can see that "recalculated" f_T and f_{max} are in good agreement with the values obtained by extrapolation of H_{21} and ULG, confirming the above discussion.

IV. CONCLUSION
In this work, the potential of 28 FDSOI nMOSFETs for future cryogenic RF applications has been assessed by analysis of RF FoMs and complete small-signal equivalent circuit elements. Temperature reduction down to 77 K has been shown to result in improvement of f_T ($\sim$85 GHz) and f_{max} ($\sim$30 GHz) both for high-V_d and low-V_d cases. Great potential of this technology for low-power applications, of critical importance at cryogenic temperatures, was illustrated. Temperature evolution of RF FoMs was explained in terms of small-signal equivalent circuit elements behavior. This was supported by the fact that f_T and f_{max} reconstructed based on the MOSFET small-signal equivalent circuit model agree well with those extracted by extrapolation of H_{21} and ULG in a temperature range down to 77 K. It has been revealed that C_{gg}, R_g, g_{ds} and C_{gd}/C_{gs} do not change much with T lowering and therefore, f_T and f_{max} T-dependencies are mostly related to g_m (due to μ and R_{sd}) T-dependence.

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N. PLANES, photograph and biography not available at the time of publication.

M. HAOND, photograph and biography not available at the time of publication.

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