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Evaluation of Bulk and SOI FeFET Architecture for Non-Volatile Memory Applications

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ABSTRACT The stress induced by the capping electrode is critical to stabilizing the ferroelectric phase in Si-doped HfO_2 which is being actively explored for embedded non-volatile memory applications. While TiN is commonly used as the electrode of choice owing to its thermodynamic stability with HfO_2, its work function (WF) (=4.8eV) results in reduced memory window (MW), and higher interlayer field (E_{IL}) in bulk Ferroelectric FETs (FeFETs). This is attributed to the built-in electric-field that arises from the WF difference between the metal and the semiconductor. This effectively reduces the ferroelectric hysteresis, and thus, the MW at the read current. Optimizing the MW and the E_{IL} would entail changing the WF, and thus, the capping electrode—essential to retaining the desired ferroelectric properties. We, therefore, propose using the silicon on insulator (SOI)-FeFET architecture which provides an additional knob—back-gate bias (V_{bg})—to optimize the MW while reducing the E_{IL}. Further, we show that unlike the bulk FeFET, where a small deviation from the optimal WF dramatically shrinks the MW, the SOI-FeFET facilitates a relatively constant MW over a wide range of V_{bg}. Thus, the SOI-FeFET simplifies the MW & E_{IL} optimization and provides an improved MW versus E_{IL} trade-off in comparison to the bulk FeFET.

INDEX TERMS Ferroelectric FET (FeFET), interlayer field (E_{IL}), memory window (MW), silicon on insulator (SOI), non-volatile memory (NVM).

I. INTRODUCTION

With the recent discovery of ferroelectricity in doped hafnium oxide (f-HfO_2), there is a renewed interest in evaluating the 1T-FeFET architecture [1], [2] for embedded non-volatile memory (NVM) applications. This is because unlike classical perovskite based ferroelectrics (example PZT, $BaTiO_3$), f-HfO_2 is not only scalable (to t_{FE} < 10nm) but also CMOS compatible. The stabilization of the ferroelectric orthorhombic (o) phase in f-HfO_2 usually requires the incorporation of dopants such as silicon (considered here) as well as mechanical confinement [3], [4]. The mechanical confinement in f-HfO_2 is achieved using a capping electrode which restrains the shearing of the HfO_2 unit cell during nucleation in the tetragonal phase, and thus, suppresses transformation to the monoclinic phase [5]. TiN is usually the metal of choice for achieving this mechanical confinement since it not only provides the required tensile stress [10], but is also thermally stable and has high oxidation and wear resistance [11].

However, with a work function (WF) of 4.8eV [12], using TiN as the gate metal for the FeFET creates a built-in field, which shifts the traversed charge (Q_{FE}) vs. voltage (V_{FE}) characteristics of the ferroelectric to negative polarization values [13], [14]. This results in reduced ferroelectric hysteresis at the read current (charge), and thus, a smaller memory window (MW). Moreover, this asymmetry also entails a dramatic increase in the maximum interlayer field (E_{ILmax}) at negative polarization values (illustrated in the following sections). Therefore, the asymmetry not only degrades the read distinguishability in the array and limits array size (due to a lower MW) [15] but is also likely to compromise the reliability & the endurance (due to higher E_{IL}). Optimizing these parameters, i.e., enhancing the MW while keeping the E_{IL} at minimum, entails a reduction in the built-in field, which can be achieved in the bulk FeFET (Fig. 1(a))

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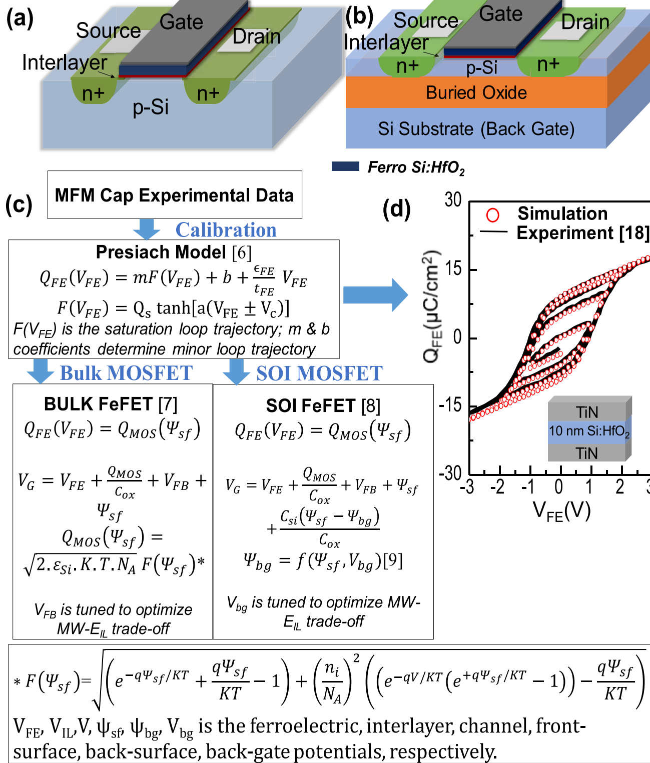

FIGURE 1. Schematic of (a) Bulk; (b) SOI FeFET; (c) Modeling framework used for the simulations; (d) Experimental & modeled Q_{FE}-V_{FE} characteristics. The simulated Q_{FE}-V_{FE} characteristics show excellent match with the experimental data reported by S. Mueller *et al.* [18].

TABLE 1. Device parameters used in simulation of bulk and SOI FeFET.

Symbol	Quantity	Value
P_r	Remnant Polarization	9 μC/cm²
P_s	Saturation Polarization	9.5 μC/cm²
E_c	Coercive Field	1.1 MV/cm
t_{FE}	Ferroelectric Layer Thickness	10 nm
t_{IL}	Interlayer Thickness	0.5 nm
t_{Si}	SOI Channel Thickness	5 nm
t_{BOX}	Buried Oxide Thickness	10 nm
ε_{IL}	Dielectric Constant of Interlayer	$7.5\varepsilon_0$ [22]
ε_{Si}	Dielectric Constant of Silicon	$11.8\varepsilon_0$
ε_{FE}	Dielectric Constant of FE	$32\varepsilon_0$
N_A	Substrate doping: Bulk [23] & SOI	5.5×10^{18} cm^{-3} (p-type)

by using a different metal with a lower WF. However, replacing TiN while retaining the ferroelectric property in f-HfO_2 can be challenging [16], [17].

Therefore, in this work, we investigate the SOI architecture for implementing the FeFET (Fig. 1(b)), wherein the back-gate bias (V_{bg}) provides an additional knob to target the optimal MW while reducing the E_{IL}, without requiring an electrode replacement. Further, we evaluate the advantages of the SOI FeFET in terms of the MW vs. E_{IL} trade-off compared to the bulk case.

II. SIMULATION FRAMEWORK

We use the Preisach's theory [6] to model the charge (Q_{FE}) vs. voltage (V_{FE}) characteristics of the ferroelectric. Fig. 1(d) shows the simulated Q_{FE}-V_{FE} characteristics calibrated to the experimental measurements shown by S. Mueller *et al.* [18]. It can be observed that our model (Fig. 1(c)) is not only able to emulate the minor Q_{FE}-V_{FE} loops but also captures the history dependent switching behavior of the ferroelectric. While remnant polarization (P_r) values as high as 24μC/cm^2 have been demonstrated in doped f-HfO_2 [19], we choose f-HfO_2 with a relatively low P_r of 9μC/cm^2(P_s = 9.5μC/cm^2) [18]. This is because even though higher P_r provides a larger MW [20], it comes at the cost of dramatically higher interlayer field (E_{IL}) which is well beyond the typical breakdown field of the interlayer. Further, we consider SiON as the interlayer of choice [21], since it exhibits a higher dielectric constant ($= 7.5\varepsilon_0$) [22] in comparison to SiO_2 which further reduces E_{IL}.

To evaluate the FeFET electrostatics, we model the gate stack as a series combination of a MFM (metal-ferroelectric-metal) capacitor and the baseline transistor, for both the SOI and the bulk architectures. A substrate doping of 5.5×10^{18} cm^{-3} [23] is considered for the bulk as well as the SOI FeFET. The bulk FeFET requires higher doping in order to constrain the short channel effects, and maintain low OFF state leakage which is essential for ensuring proper array operation [15]. While conventional SOI transistors (which have a floating body) usually use lower channel doping, a higher substrate doping is required in case of the SOI FeFET to ensure sufficient GIDL current during the program operation (i.e., to write the high V_T state) in order to supply hole carriers to the channel [24], [25].

In contrast to the stand-alone MFM capacitors, the additional capacitive contributions in the FeFET arising from the interlayer capacitance (C_{IL}) and semiconductor capacitance (Cs) take up a significant portion of the applied gate voltage (V_{GS}) which consequently reduces the net voltage drop across the ferroelectric layer (V_{FE}). The reduced V_{FE} along with the condition for charge conservation in the gate stack results in the ferroelectric operating on a minor loop trajectory with reduced charge and hysteresis in comparison to the saturation loop. The flow chart and the equations to compute the minor loop trajectory for the ferroelectric in the FeFET for both the bulk and the SOI architectures is shown in Fig. 1(c). The parameters used in the simulation are specified in Table I.

III. RESULTS AND DISCUSSIONS

Fig. 2(a-b) shows the evolution of the semiconductor potential (ψ_s) and the interlayer field (E_{IL}) as a function of the write voltage, V_{write}, (applied to the gate) in case of the bulk FeFET; a positive write voltage ($V_{write} = V_{erase}$) is used to program the device to the low V_T state while a negative write voltage ($V_{write} = V_{prog}$) is used to program the FeFET to the high V_T state; $|V_{prog}| = |V_{erase}|$, unless specified otherwise. The resulting Q_{FE}-V_{FE} characteristics of the ferroelectric are shown in Fig. 2(c). Here, we consider two cases: bulk FeFET with TiN as gate electrode ($\Delta WF = 0V$),

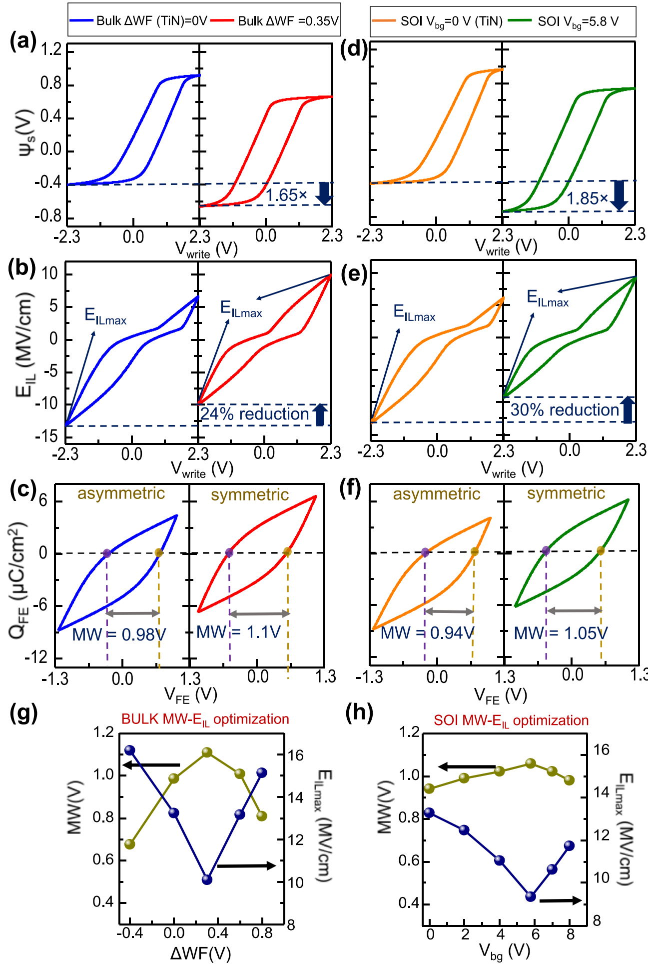

FIGURE 2. Comparison of (a) semiconductor potential (Ψ_S) (b) Interlayer Field (E_{IL}), and (c) Q_{FE}-V_{FE} characteristics of bulk FeFET with TiN (ΔWF = 0V), and ΔWF = 0.35V, respectively, at $V_{write} = \pm 2.3$V. Similar plots are generated in (d), (e), (f) for the SOI FeFET with V_{bg} = 0V and V_{bg} = 5.8V, respectively, for $V_{write} = \pm 2.3$V; the maximum E_{IL} (E_{ILmax}) occurs when the FeFET is in accumulation. Variation of the MW and the E_{ILmax} as a function of (g) WF & (h) V_{bg} for bulk & SOI FeFET, respectively.

and ΔWF = 0.35V, which is required to obtain an optimized MW and E_{IL}; the latter case would require replacing TiN with a lower WF metal. Similar characteristics are also evaluated for the SOI FeFET architecture for V_{bg} = 0V (unoptimized MW and E_{IL}), and V_{bg} = 5.8V (optimized MW and E_{IL}) as shown in Fig. 2(d-f).

In case of the bulk FeFET with TiN electrode, we observe a MW of 0.98V (evaluated at a charge density of 0.02μC/cm^2 to enable MW measurement at a constant current of 1μA) which is less than the maximum width (=1.13V) of the hysteresis loop (minor) traversed by the ferroelectric. Additionally, this relative asymmetry in the Q_{FE} vs. V_{FE} characteristics also increases the E_{IL} (=13.2MV/cm) during the program operation when the FeFET channel is in accumulation (Fig. 2(b)).

In the bulk FeFET, recovering the reduced MW necessitates a reduction in the WF by 0.35eV in comparison

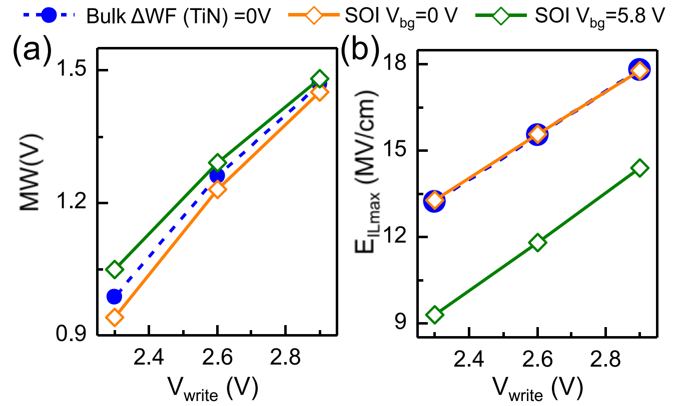

FIGURE 3. Evolution of (a) MW (b) maximum Interlayer field (E_{ILmax}) as a function of write voltage (V_{write}) for both bulk and SOI FeFET. The SOI architecture with back gate bias of 5.8V shows significantly lower (30%) E_{ILmax} and slightly improved MW (7% improvement) in comparison to bulk FeFET (TiN, ΔWF = 0V) at $V_{write} = \pm 2.3$V.

to TiN, as shown in Fig. 2 (a-c). Subsequently, this also minimizes the interlayer field and makes the E_{IL} vs. V_{write} curve symmetric during the erase (semiconductor channel in inversion) & the program (semiconductor channel in accumulation) operation. Achieving this symmetry would typically entail replacing TiN with a lower WF metal which can be a challenge for maintaining the desired ferroelectric properties. Substituting TiN with other metals usually offsets the ferroelectric properties (Pr, coercive field, E_c) [16] as well as affects the symmetry of the Q_{FE}-V_{FE} characteristics, which is unfavorable for the FeFET's application as NVM. TiN also facilitates lower leakage in comparison to other metal electrodes owing to the relatively high Schottky barrier at the TiN/*o*-HfO_2 interface [17]. Therefore, optimization of the bulk FeFET by replacing TiN with a lower work-function metal may be practically challenging.

In contrast, the SOI architecture for the FeFET provides an additional knob - the back-gate bias (V_{bg}) - which can help tune the built-in field to achieve maximum ferroelectric hysteresis resulting in enhanced MW as well as lower E_{IL}. This is confirmed in Fig. 2 (d-f), where it can be observed that using an appropriate V_{bg} = 5.8V enhances the MW to 1.05V (MW for V_{bg} = 0V is 0.94V) while reducing the E_{ILmax} to 9.3MV/cm (E_{ILmax} for V_{bg} = 0V is 13.3MV/cm) at $V_{write} = \pm 2.3$V. The back-gate bias is applied only during the program/erase operation, and hence does not contribute to static power consumption.

The back-gate bias ensures that the ferroelectric hysteresis loop is symmetric, and hence, the effective hysteresis width (and MW) observed at read bias (conditions specified above) is higher than the case with V_{bg} = 0V (Fig. 2(f)) even though the maximum hysteresis width for V_{bg} = 0V (centered at -1.85μC/cm^2) is higher than the maximum hysteresis for V_{bg} = 5.8V. We also note that the back-gate bias (V_{bg} = 5.8V) results in E_{IL} = 9.3MV/cm for both the program and the erase operation. This magnitude

is higher in comparison to the E_{IL} observed during the erase operation (=6.2MV/cm), but significantly lower when compared to the E_{IL} observed during the program operation (=13.3MV/cm) when $V_{bg} = 0V$ (Fig. 2(e)). Therefore, applying the back-gate bias reduces the maximum field experienced by the device, which is likely to improve the endurance.

The symmetric Q_{FE} vs. V_{FE} characteristics (Fig. 2(f)), facilitated by the back-gate bias ($V_{bg} = 5.8V$), also reduces the maximum depolarization field ($E_{dep} \propto P_r$ [26]) (=0.17MV/cm at $V_{write} = \pm 2.3V$) in comparison to the maximum E_{dep}(=0.31MV/cm at $V_{prog} = -2.3V$) for $V_{bg} = 0V$. The lower E_{dep} is likely to improve the retention of the device [18].

Further, we evaluate the MW and the E_{ILmax} as a function of the shift in the gate metal work function (ΔWF), and the back-gate bias (V_{bg}) for the bulk and the SOI FeFET, respectively, as shown in Fig. 2(g) and Fig. 2(h). It can be observed that for the bulk FeFET, there is a dramatic roll off in the MW along with a significant increase in the interlayer field as we move away from the optimal WF point. This would imply a considerable degradation in the FeFET performance for a small deviation from the target work function of the metal. In contrast, the MW remains relatively constant for the SOI FeFET over a wide range of V_{bg} while minimizing the E_{IL}. This can be attributed to the reduced sensitivity of the threshold voltage (and therefore, MW) to the back-gate bias [27]. In the device configuration simulated here, this corresponds to an optimal back-gate bias (=5.8V) where E_{ILmax} is at its lowest value (=9.3MV/cm) while enabling a maximum MW (=1.05V). The relatively constant MW is likely to simplify the FeFET design. Moreover, the magnitude of V_{bg} can be scaled down to ~4V by reducing the buried oxide thickness to ~5nm [28].

In addition, we consider the evolution of the MW and the E_{ILmax} as a function of the write voltage (V_{write}), as shown in Fig. 3(a-b). It can be observed that in comparison to the baseline bulk FeFET (with TiN), the SOI FeFET with appropriate V_{bg} (=5.8V) consistently exhibits lower E_{ILmax} and higher MW; at $V_{write} = \pm 2.3V$, a 30% reduction in the E_{ILmax} along with a slight enhancement (7%) in the MW is achieved (compared to the bulk FeFET with TiN gate metal). Furthermore, we also assessed the possibility of using asymmetric programing conditions, i.e., $V_{prog} < V_{erase}$ instead of back-gate bias to improve the MW vs. E_{ILmax} trade-off. However, since the hysteresis width and MW are strong functions of the write voltage (Fig. 3), there is a steep reduction in the MW as V_{prog} is reduced. The back-gate bias still offers a better MW vs. E_{IL} trade-off in comparison to the asymmetric program voltage scheme.

Thus, the SOI architecture provides a better MW vs. E_{IL} trade-off enabling a MW of ~1V for write voltages as low as ±2.3V with E_{IL} below the typical breakdown field of the interlayer. This provides a pathway to realizing a FeFET-based NVM technology with sub-1fJ/bit program energies.

IV. CONCLUSION

In summary, we show that the SOI architecture can be leveraged to overcome the design constraints of the bulk FeFET imposed by the work function of the TiN gate electrode. Besides eliminating the need for WF tuning, the SOI FeFET with appropriate V_{bg} enables lower E_{IL} and slightly higher MW making the SOI FeFET a promising architecture for ferroelectric NVM technology.

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