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A Compensation Method for Variations in Subthreshold Slope and Threshold Voltage of Thin-Film Transistors for AMOLED Displays

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ABSTRACT In this paper, we propose a compensation method for variations in the subthreshold slope (SS) and threshold voltage (Vth) of the low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) in an attempt to improve the image quality of the active matrix organic light-emitting diode (AMOLED) displays for mobile applications. The proposed compensation method provides a uniform voltage to the OLED according to the gray level without being affected by variations in the SS and Vth of the LTPS TFTs. To verify the performance of the proposed compensation method, a test pattern, including two pixel circuits designed for 5.7-inch quadruple high-definition AMOLED display was fabricated and measured. The measurement results showed that the proposed compensation method achieved an emission current error of the pixel circuit of only ± 3.1 LSB at the 255^{th} gray level. Therefore, the proposed compensation method is very suitable for AMOLED displays requiring high image quality.

INDEX TERMS Thin film transistors, organic light-emitting diode displays, pixel circuit, high image quality.

I. INTRODUCTION

Recently, active-matrix organic light-emitting diode (AMOLED) displays have been widely used for mobile applications. To realize high spatial resolution over 500 ppi of mobile displays, low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been employed in the AMOLED displays of mobile devices because of their high mobility and high reliability [1]–[5]. However, they suffer from variations in the electrical characteristics of the LTPS TFTs, which severely degrades the image quality of AMOLED displays. To solve these problems, external and internal compensation methods for the electrical characteristic variation have been researched [1]–[8].

The external compensation methods in [6]–[8] sense the electrical characteristics of the LTPS TFTs and compensate for their variations by modulating the data signal of the display image using external logic blocks and memories, which increase the system complexity and cost. Therefore, these methods have been generally adopted only for large-sized display applications such as TVs.

The internal compensation methods can be categorized into the voltage- and current-programming methods [1]–[5]. The voltage-programming method provides a data signal to the pixel circuit in the form of a voltage. The diode-connection method, which is a typical voltage-programming method, has been widely used to compensate for variation in the threshold voltage (Vth) of an LTPS TFT [1]–[4]. However, this method suffers from a large emission current error (ECE) due to variation in the subthreshold slope (SS) of the LTPS TFTs when the emission current is less than several nA, which is within the subthreshold region, over the entire gray level [9]–[11].

The current-programing method provides a data signal to the pixel circuit in the form of a current to compensate for variation in SS [5]. However, this method takes a long time

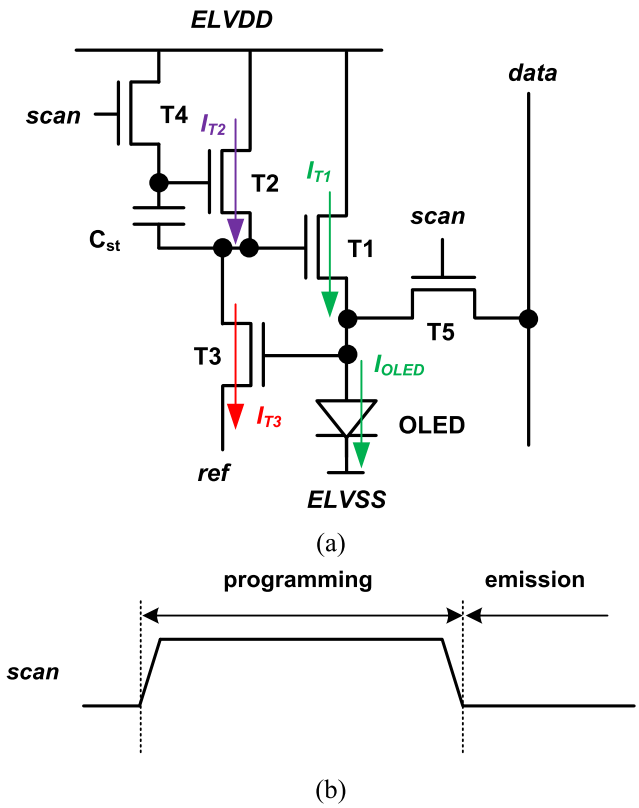

FIGURE 1. (a) Schematic and (b) timing diagram of the 5T1C pixel circuit using the proposed compensation method.

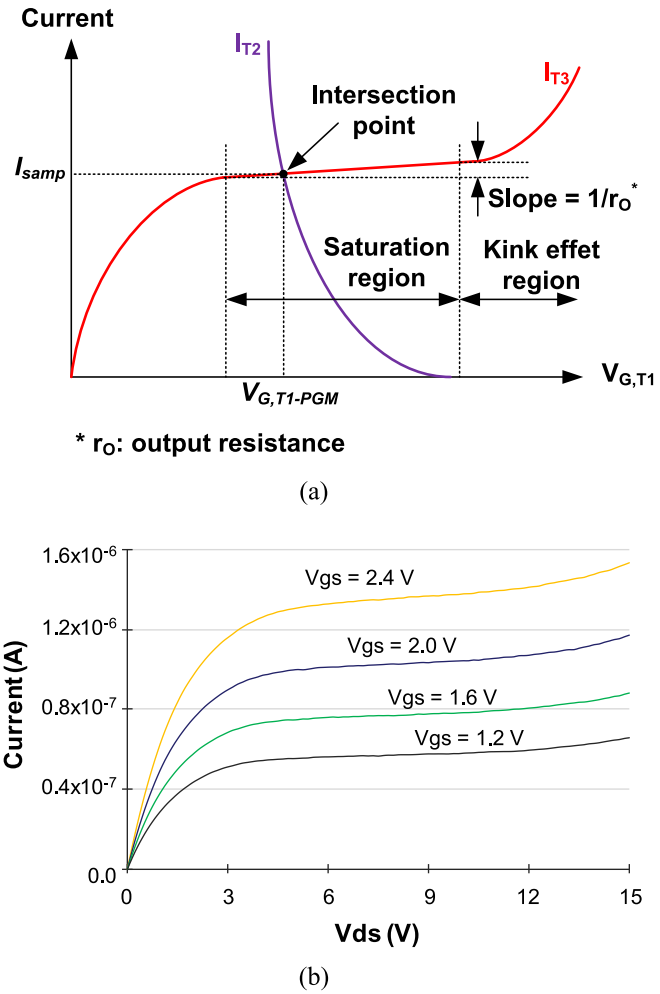

FIGURE 2. (a) Characteristics of I_{T2} and I_{T3} according to $V_{G,T1}$ and (b) measured output characteristics of T3.

to charge the data line. For example, when the capacitive load of the data line and the emission current at the maximum gray level are 30 pF and 3.7 nA, respectively, the charging time required to change the data line voltage by 1 V is 6.3 ms, which is much longer compared to a row line time of a few μs.

In this paper, a novel method that can compensate for variations in the SS and Vth of the LTPS TFTs is proposed. The proposed method significantly reduces the ECE caused by variations in the SS and Vth of the LTPS TFTs compared to the conventional diode-connection method. To verify the performance of the proposed compensation method, a test pattern including two pixel circuits, which were designed for a 5.7-inch quadruple high-definition AMOLED display, was fabricated and measured.

II. 5T1C PIXEL CIRCUIT USING PROPOSED COMPENSATION METHOD

Fig. 1(a) and (b) respectively show the schematic and timing diagram of the 5T1C pixel circuit using the proposed compensation method for variations in the SS and Vth of the LTPS TFTs. The *scan* signal is applied to the gate nodes of T4 and T5, and the *data* signal (V_{data}) is provided to the source node of T5. According to the *scan* signal, the 5T1C pixel circuit operates in the programming and emission phases as shown in Fig. 1(b).

In the programming phase, the *scan* signal becomes high to turn on T4 and T5 transferring the voltage at ELVDD (V_{ELVDD}) and V_{data} to the gate nodes of T2 and T3, respectively, thus generating a sampling current (I_{samp}) flowing through T2 and T3 according to V_{data}. When T3 operates in the saturation region, the currents of T2 (I_{T2}) and T3 (I_{T3}) according to the gate voltage of T1 ($V_{G,T1}$) and the measured output characteristics of T3 are depicted in Fig. 2(a) and (b), respectively. I_{T3} becomes constant with a value of I_{samp} in the saturation region regardless of $V_{G,T1}$, while T2 operates like a diode because the gate and drain nodes of T2 are connected through T4. Therefore, $V_{G,T1\text{-}PGM}$, which is $V_{G,T1}$ in the program phase, is determined at the intersection of I_{T2} and I_{T3} as shown in Fig. 2(a), and $V_{ELVDD}-V_{G,T1\text{-}PGM}$ is stored in C_{st}.

In the emission phase, the *scan* signal becomes low to turn off T4 and T5. At the beginning of this phase, $V_{G,T1}$ and the anode voltage of the OLED (V_{anode}) vary due to the difference between the currents of T1 (I_{T1}) and the OLED (I_{OLED}) until I_{T1} and I_{OLED} becomes the same. When I_{T1} is larger than I_{OLED}, V_{anode} increases,

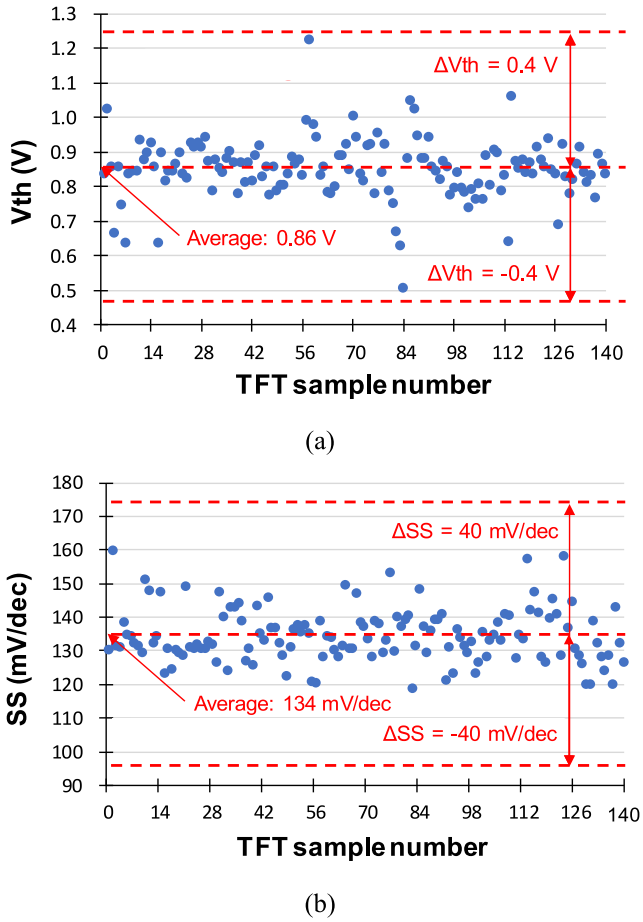

FIGURE 3. Measured (a) Vth and (b) SS of 140 unit TFTs in the fabricated test pattern.

thus increasing I_{T3} and decreasing $V_{G,T1}$. Consequently, I_{T1} decreases until it becomes equal to I_{OLED}. On the other hand, when I_{T1} is smaller than I_{OLED}, V_{anode} decreases, thus decreasing I_{T3} and increasing $V_{G,T1}$. Consequently, I_{T1} increases until it becomes equal to I_{OLED}. Therefore, when I_{T1} becomes equal to I_{OLED}, V_{anode} should be maintained as V_{data} in the programming phase because T2 supplies I_{samp} to T3 by its gate-to-source voltage, which is equal to (V_{ELVDD}–$V_{G,T1\text{-}PGM}$) stored in C_{st}. In this way, a uniform V_{anode} can be provided to the anode of the OLED without being affected by variations in the SS and Vth of T1, T2, and T3. The proposed compensation method, which is realized using the n-type LTPS TFTs in this work, can also be used for the pixel circuit using other TFTs such as the oxide, amorphous silicon, and organic TFTs because the Vth shifts, which may occur during the operation of the display using other TFTs, can be compensated.

III. ANALYSIS OF VARIATION IN V_{ANODE} IN EMISSION PHASE

Fig. 3(a) and (b) show the measured Vth and SS of the 140 unit TFTs, of which the standard deviations (σ) are 0.087 V and 8.32 mV/dec, respectively. The Vth and SS of 140 TFTs are measured when Vds is biased by 5.1 V, which is supplied by the parameter analyzer (Agilent, 4156C). The Vth is extracted using the derivative method. In the simulation, the respective variations in the SS and Vth of ±40 mV/dec and ±0.4 V are used to cover the range over $\pm 4\sigma$. Assuming that the values of the SS and Vth are independently determined in the Gaussian distribution, the probability that the values of both ΔVth and ΔSS will be $\pm 4\sigma$ is $6.3\times10^{-5}\times6.3\times10^{-5}$, indicating that only the one TFT out of 25 million TFTs will have the values of both ΔVth and ΔSS of $\pm 4\sigma$. Therefore, in this work, such TFTs having the values of $\pm 4\sigma$ will barely exist in a QHD (2560×1440) AMOLED display panel including 22,118,400 analog TFTs (T1, T2, and T3).

To investigate the performance of the 5T1C pixel circuit using the proposed compensation method, the variation in V_{anode} (ΔV_{anode}) according to the electrical characteristics of T1, T2, and T3 is analyzed. When $V_{G,T1}$ varies to control the current flowing through T1 at the beginning of the emission phase, the drain-to-source voltages of T2 ($V_{DS,T2}$) and T3 ($V_{DS,T3}$) vary, resulting in a variation in I_{samp} (ΔI_{samp}) and ΔV_{anode}. Here, ΔI_{samp} can be described as

$$\begin{aligned}\Delta I_{samp} &= g_{m,T2}\cdot\Delta V_{GS,T2} + g_{ds,T2}\cdot\Delta V_{DS,T2}\\ &= g_{m,T3}\cdot\Delta V_{GS,T3} + g_{ds,T3}\cdot\Delta V_{DS,T3},\end{aligned} \quad (1)$$

where $\Delta V_{GS,T2}$, $\Delta V_{GS,T3}$, $g_{m,T2}$, $g_{m,T3}$, $g_{ds,T2}$, and $g_{ds,T3}$, are variations in the gate-to-source voltages of T2 ($V_{GS,T2}$) and T3 ($V_{GS,T3}$), $\partial I_{T2}/\partial V_{GS,T2}$, $\partial I_{T3}/\partial V_{GS,T3}$, $\partial I_{T2}/\partial V_{DS,T2}$, and $\Delta I_{T3}/\partial V_{DS,T3}$, respectively. Since $\Delta V_{GS,T3}$ is equal to ΔV_{anode}, ΔV_{anode} can be derived from (1) and expressed as

$$\Delta V_{anode} = \frac{\left(g_{m,T2}\cdot\Delta V_{GS,T2} + g_{ds,T2}\cdot\Delta V_{DS,T2} - g_{ds,T3}\cdot\Delta V_{DS,T3}\right)}{g_{m,T3}}. \quad (2)$$

In (2), since $\Delta V_{GS,T2}$, which is a switching error caused by T4, is negligibly small compared to $\Delta V_{DS,T2}$ and $\Delta V_{DS,T3}$, which have opposite polarity each other, ΔV_{anode} is mainly affected by $\Delta V_{DS,T2}$ and $\Delta V_{DS,T3}$. In addition, the uniformity of V_{anode} is affected with different device performance and size. As expressed in (2), ΔV_{anode}, which represents the uniformity of V_{anode} in the proposed pixel circuit, can be improved (decreased) by decreasing the $g_{ds,T2}$ and $g_{ds,T3}$. Since the $g_{ds,T2}$ and $g_{ds,T3}$ represent the current changes of T2 and T3 according to the drain-to-source voltage change, respectively, the uniformity of V_{anode} can be further improved by increasing the lengths of T2 and T3.

To examine the validity of (2), V_{anode} was simulated when a variation in the Vth of T1 (ΔVth_{T1}) is ±0.4 V. The simulation results show that ΔV_{anode} in the emission phase is −26.2 mV and 27.2 mV at ΔVth_{T1} of +0.4 V and −0.4 V, respectively, as shown in Fig. 4. In addition, $g_{m,T2}$, $g_{m,T3}$, $g_{ds,T2}$, $g_{ds,T3}$, $\Delta V_{DS,T2}$, and $\Delta V_{DS,T3}$ were simulated to be 2.0 μA/V, 2.6 μA/V, 72.5 nA/V, 102.8 nA/V, ∓0.4 V, and ±0.4 V, respectively. By applying these simulated parameters to (2), ΔV_{anode} was calculated to be ±27 mV, which was

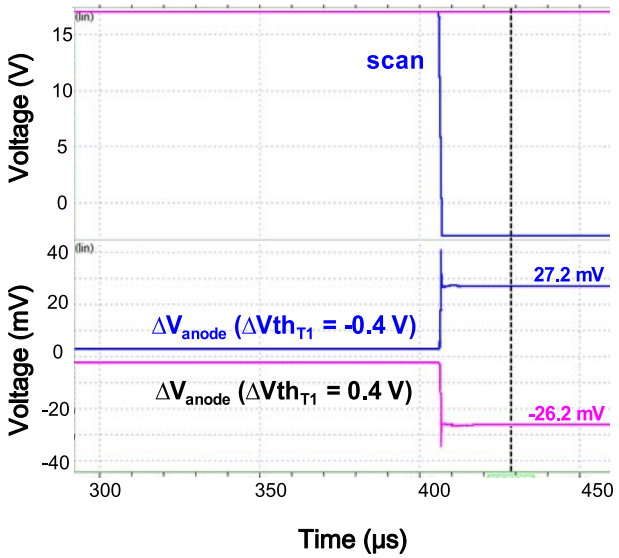

FIGURE 4. Simulation results of ΔV_{anode} when ΔVth_{T1} is ±0.4 V.

almost equal to the simulated ΔV_{anode} in Fig. 4, representing that (2) was in good agreement with the simulation results. Therefore, (2) is valid for accurate estimation of ΔV_{anode} so that the performance of the pixel circuit can be properly estimated using ΔV_{anode}.

IV. 7T2C PIXEL CIRCUIT USING PROPOSED COMPENSATION METHOD

The 5T1C pixel circuit in Fig. 1 has two issues. One of the issues is that ΔV_{anode} is affected by $\Delta V_{DS,T2}$ and $\Delta V_{DS,T3}$ as analyzed in Section III. In this regard, a cascode scheme can be adopted to reduce ΔV_{anode} by reducing $\Delta V_{DS,T2}$ and $\Delta V_{DS,T3}$. However, it increases the number of TFTs and the headroom voltage. The other issue is that I_{samp} flowing through T2 and T3 is static during the emission phase, thereby increasing the power consumption.

To solve the above issues, the 5T1C pixel circuit was modified as 7T2C pixel circuit using the same proposed compensation method as shown in Fig. 5(a). In this 7T2C pixel circuit, T6 is serially added only to T3 to make a cascode scheme, considering the trade-off between ΔV_{DS}, number of TFTs, and the headroom voltage. In addition, the current path between T2 and T3 is disconnected by controlling T6 using the *em* signal during the emission phase so as to prevent the static current. The *scan[n]* and *scan[n+1]* signals in the modified 7T2C pixel circuit represent the *scan* signals in the n^{th} and $(n+1)^{th}$ row lines, respectively. According to the *em*, *scan[n]*, and *scan[n+1]* signals, the 7T2C pixel circuit operates in the programming, biasing, and emission phases as shown in Fig. 5(b).

In the programming phase, the *scan[n]* and *scan[n+1]* signals are high to turn on T4, T5, and T7, and the *em* signal with V_{sat} is applied to T6 to operate it in the saturation

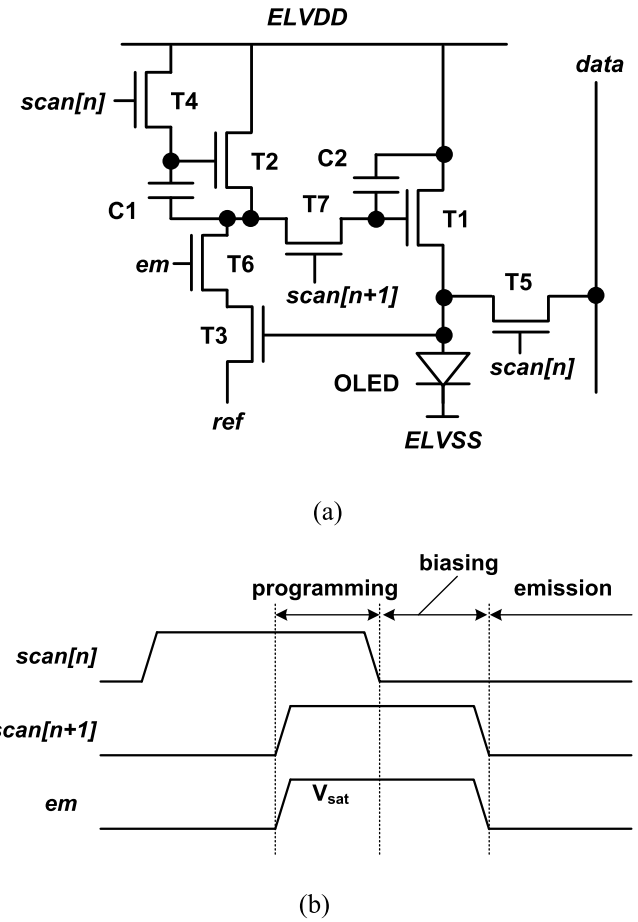

FIGURE 5. (a) Schematic and (b) timing diagram of the 7T2C pixel circuit.

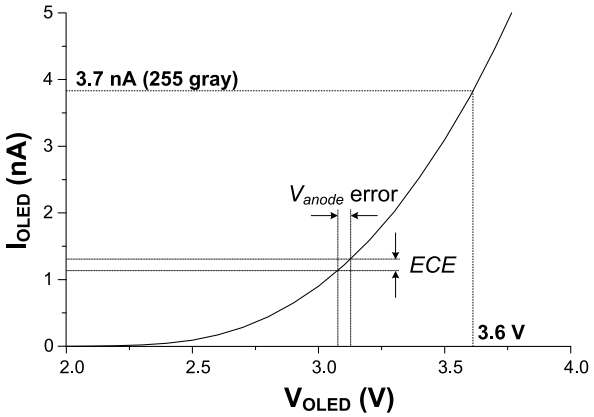

FIGURE 6. OLED characteristic used in the simulations.

region. Then, I_{samp} generated by T3 flows through T2 and T6, while $V_{GS,T2}$ is stored in C1.

In the biasing phase, the *scan[n]* signal becomes low to turn off T4 and T5, and the *scan[n+1]* signal stays high to turn on T7. The proposed 7T2C pixel circuit provides a uniform voltage to the anode of the OLED by generating the I_{samp} by T3 according to V_{data} and maintaining the I_{samp} by T2 after the scan signal becomes low. In this way, the

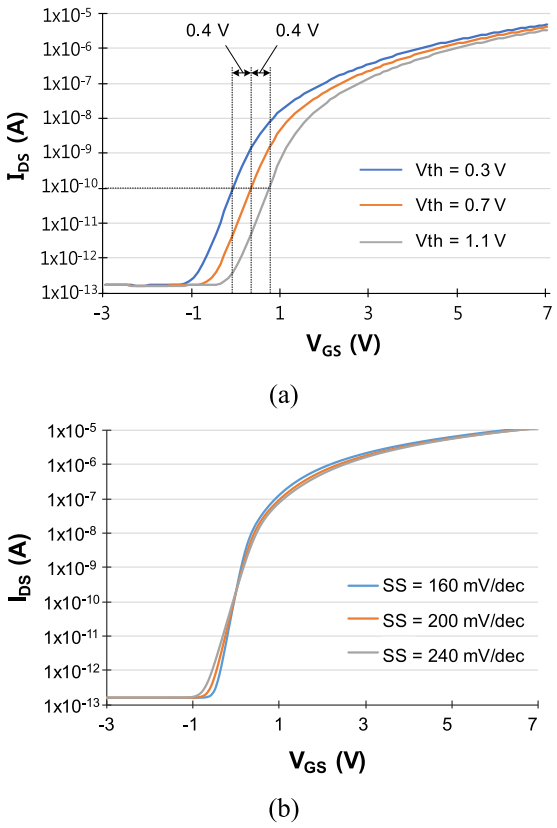

FIGURE 7. Simulated transfer curves of T1 when (a) Vth varies from 0.3 V to 1.1 V and (b) SS varies from 160 mV/dec to 240 mV/dec.

uniformity of V_{anode} in the proposed 7T2C pixel circuit can be improved. The above operation of the proposed 7T2C pixel circuit is the same as the operation of the 5T1C pixel circuit, which is described in detail in Section II. In addition, since T2 keeps supplying I_{samp} to T6 and the *em* signal maintains V_{sat}, the source voltage of T6, which is equal to the drain voltage of T3, hardly changes. Therefore, $\Delta V_{DS,T3}$ in the 7T2C pixel circuit becomes much smaller than that in the 5T1C pixel circuit, thus reducing ΔV_{anode}.

In the emission phase, the *scan[n]*, *scan[n+1]*, and *em* signals are low to turn off T4, T5, T7, and T6. Then, T6 prevents the static current from flowing through T2 and T3. In addition, due to the gate voltage of T1 stored in C2 during the biasing phase, T1 provides the OLED with the same emission current and V_{anode} as in the biasing phase.

V. VERIFICATIONS

Fig. 6 shows the simulated electrical characteristics of the OLED used in the simulations for 5T1C and 7T2C pixel circuits. The anode-to-cathode voltage of the OLED was simulated to be 3.6 V for the luminance at the 255th gray level. Fig. 7(a) and (b) show the simulated transfer curves of T1 used in both the 5T1C and 7T2C pixel circuits when the Vth and SS vary from 0.3 V to 1.1 V and from 160 mV/dec to 240 mV/dec, respectively.

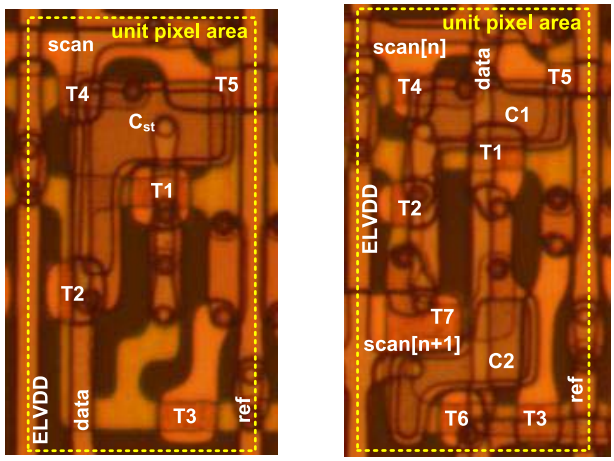

FIGURE 8. Photomicrographs of (a) 5T1C and (b) 7T2C pixel circuits in the fabricated test pattern.

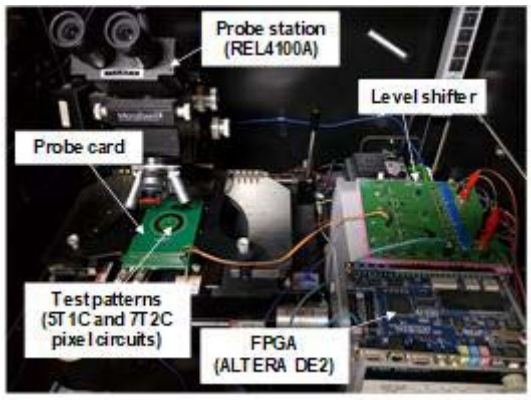

FIGURE 9. Measurement environment to apply the input signals to the test pattern and measure the anode voltage of the OLED in the proposed pixel circuits.

To verify the performance of the 5T1C and 7T2C pixel circuits using the proposed compensation method, a test pattern including 13 samples, each of which has 5T1C and 7T2C pixel circuits, and 140 unit TFTs, was fabricated for a 5.7-inch QHD AMOLED display. In the test pattern, a diode-connected TFT was used instead of an OLED in the 5T1C and 7T2C pixel circuits. Fig. 8(a) and (b) show the photomicrographs of the 5T1C and 7T2C pixel circuits, respectively, in a fabricated test pattern. The area of a unit pixel is 22 μm × 44 μm. The width-to-length ratios of the analog devices (T1, T2, and T3) and the switching devices (the rest of the TFTs) were 3.0 μm/7.0 μm and 3.0 μm/3.5 μm in the 5T1C and 7T2C pixel circuits, respectively.

Fig. 9 shows the measurement environment of the proposed pixel circuits. In the measurement, the probe station (Cascade Microtech, ALESSI REL 4100A), parameter analyzer (Agilent, 4156C), and FPGA board (Altera, DE2) are

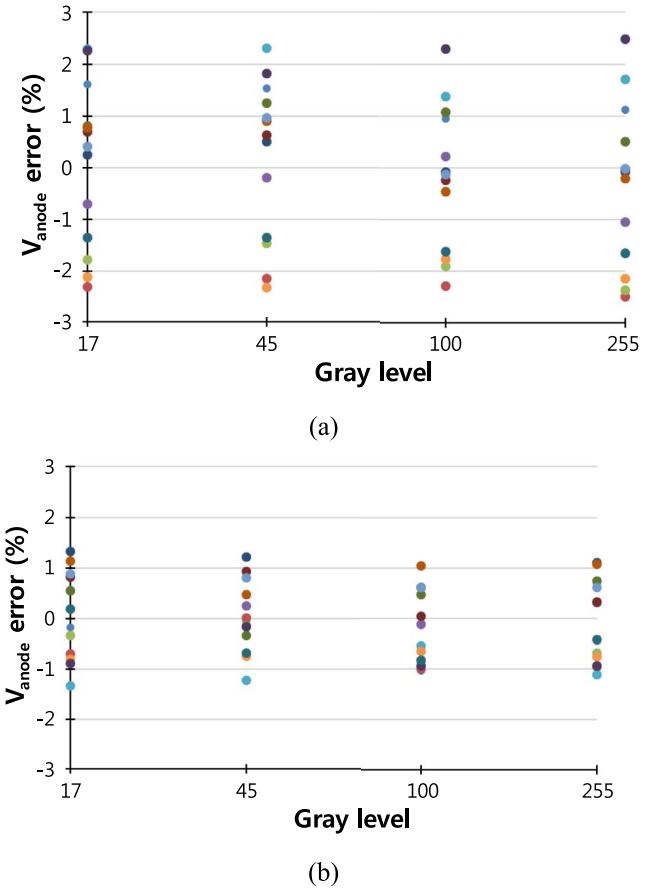

FIGURE 10. Measured V_{anode} errors of (a) 5T1C and (b) 7T2C pixel circuits using 13 samples according to the gray level.

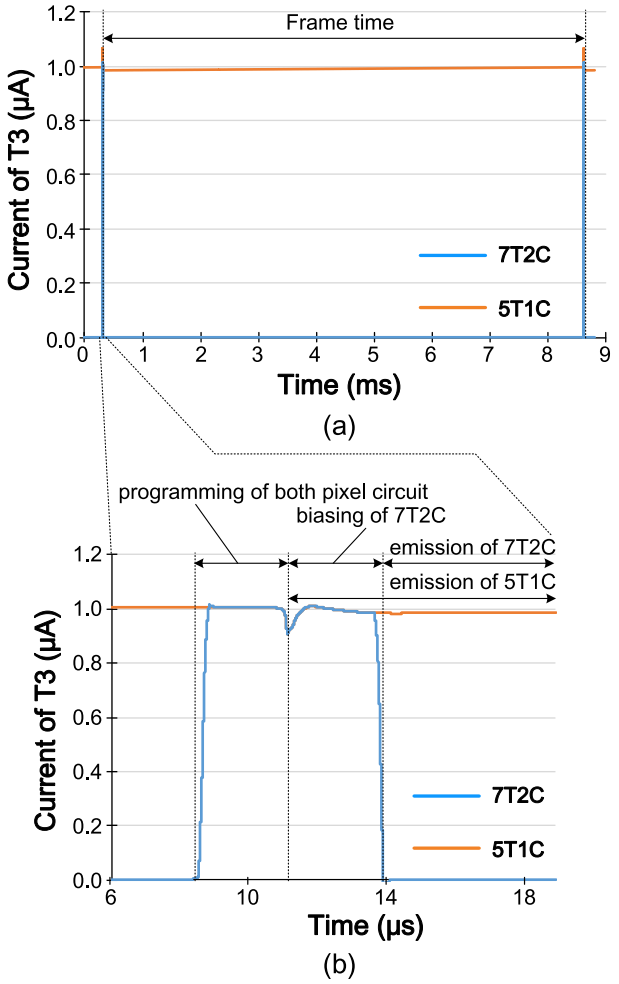

FIGURE 11. Simulated bias current of T3 in the 5T1C and 7T2C pixel circuits (a) during a frame time and (b) zoomed-in view of the programming and biasing phases.

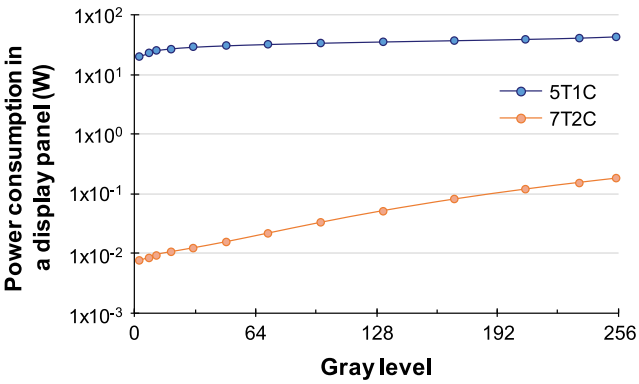

FIGURE 12. Simulated power consumption of the QHD display panel using 5T1C and 7T2C pixel circuits according to gray level when all OLEDs in a display panel emit light.

used. In addition, a level shifter is used to increase the voltage level of the output signal of the FPGA board up to ±10 V. The test pattern with the 5T1C and 7T2C pixel circuits is placed on the chuck of the probe station. The probe card is also placed on the chuck to make a contact with the test pattern. To prevent the light leakage current of TFTs, the probe station is installed in a dark box. The FPGA board is used to generate the input signals of which the voltage levels are increased using the level shifter. The parameter analyzer is connected to the probe card via coaxial cables from the outside of the dark box.

Fig. 10(a) and (b) respectively show the V_{anode} errors of the 5T1C and 7T2C pixel circuits measured from the 13 samples, according to the gray level. The measured V_{anode} error of the 7T2C pixel circuit at the 255th gray level was reduced to ±1.3% from ±2.5% achieved in the case of the 5T1C pixel circuit.

Fig. 11(a) and (b) show that the simulated bias current of T3 in the 5T1C and 7T2C pixel circuits during a frame time and zoomed-in view of the programming and biasing phases, respectively. In addition, Fig. 12 shows the power consumption of the QHD (2560×1440) display panels using the 5T1C and 7T2C pixel circuits. As shown in Fig. 11, the bias current of T3 in the 5T1C pixel circuit flows during all the phases, while that in the 7T2C pixel circuit flows only during the programing and biasing phases. Therefore, the power

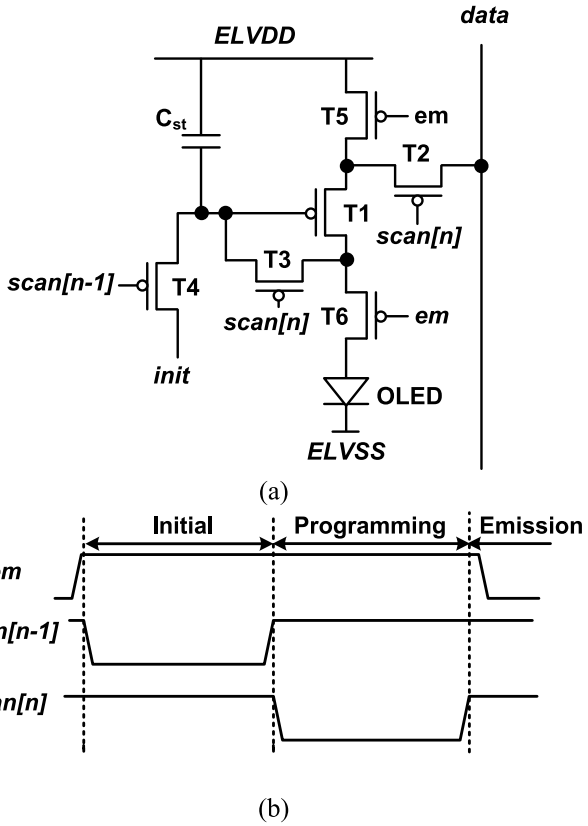

FIGURE 13. (a) Schematic and (b) timing diagram of the 6T1C pixel circuit using the conventional diode-connection method [3].

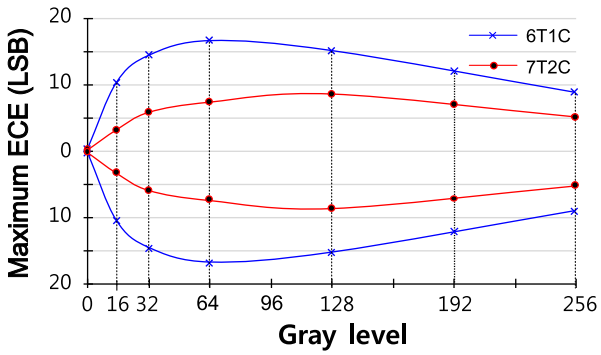

FIGURE 14. Simulated maximum emission current errors (ECEs) of the 6T1C pixel circuit using the conventional compensation method and 7T2C pixel circuit using the proposed compensation method according to the gray level at a frame rate of 120 Hz when variations in the SS and Vth are ±40 mV/dec and ±0.4 V.

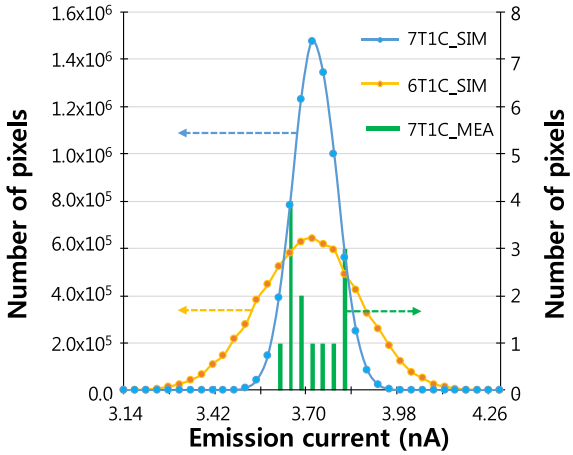

FIGURE 15. Histograms of the number of pixels according to the simulated emission current of the display panels using the 6T1C (6T1C_SIM) and 7T2C (7T1C_SIM) pixel circuits (left y-axis), and according to the measured emission current of the 13 samples of the 7T2C (7T2C_MEA) pixel circuit in the fabricated test pattern (right y-axis).

consumption of the 7T2C pixel circuit is much less than that of the 5T1C pixel circuit. In addition, as shown in Fig. 12, the power consumption of the QHD (2560×1440) display panels using the 7T2C pixel circuit is 238.6 to 2747.5 times less than that using the 5T1C pixel circuit over the entire gray level.

One of the drawbacks in the conventional diode-connection method is a slow compensation speed, which increases the ECE caused by variation in the SS [13]. On the contrary, the proposed compensation method does not require a long compensation time because it compensates for variations in the Vth and SS using high bias current during short compensation time. To compare the compensation speed of the proposed 7T2C pixel circuit with the 6T1C pixel circuit in Fig. 13 using the conventional diode-connection method, the maximum emission current error of both pixel circuits is simulated at a frame rate of 120 Hz, which has only half of the compensation time at a frame rate of 60 Hz.

Fig. 14 shows the simulated maximum ECEs of the 6T1C and 7T2C pixel circuits at the 0^{th}, 16^{th}, 32^{nd}, 64^{th}, 128^{th}, and 255^{th} gray levels at a frame rate of 120 Hz when variations in the SS and Vth are ±40 mV/dec and ±0.4 V, respectively. The figure reveals that the 7T2C pixel circuit using the proposed compensation method achieved much less maximum ECEs than the 6T1C pixel circuit using the conventional diode-connection method over the entire gray level.

Assuming that both the Vth and SS are randomly distributed with Gaussian profiles over a display panel with a 2560×1440 resolution, the emission currents of the 6T1C and 7T2C pixel circuits were simulated. Fig. 15 shows the histograms of the number of pixels according to the simulated emission current of the respective display panels using the 6T1C and 7T2C pixel circuits (left y-axis). In addition, it shows the histogram of the number of pixels according to the measured emission currents of the 13 samples of the 7T2C pixel circuit in the fabricated test pattern (right y-axis). It was observed that the standard deviation of the emission current of the 7T2C pixel circuit was reduced to 65.3 pA from 156 pA achieved in the 6T1C pixel circuit when the average simulated emission current of both the 6T1C and 7T2C pixel circuits was 3.7 nA. In addition, it was observed that the emission currents measured from the 13 samples of the

7T2C pixel circuit exhibited a relatively narrow variation from 3.6 nA to 3.8 nA, which corresponds to an ECE of ±3.1 LSB. Thus, the 7T2C pixel circuit using the proposed compensation method greatly improved the emission current uniformity of the AMOLED displays compared to the 6T1C pixel circuit using the conventional compensation method.

VI. CONCLUSION

This paper proposes a compensation method for variations in the SS and Vth of the LTPS TFTs to improve the image quality of AMOLED displays for mobile applications. The proposed compensation method provides a uniform voltage to the OLED according to the gray level without being affected by variations in the SS and Vth of the LTPS TFTs. The simulation results showed that the 7T2C pixel circuit using the proposed compensation method achieved much less maximum ECEs than the 6T1C pixel circuit using the conventional compensation method over the entire gray level. In addition, the measurement results showed that the proposed compensation method achieved an ECE of ±3.1 LSB at the 255th gray level. Therefore, the proposed method, which can be applied to the pixel circuits using either oxide, amorphous silicon, organic TFTs or LTPS TFTs, is very suitable for AMOLED displays requiring high image quality.

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