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A 6-TFT Charge-Transfer Self-Compensating Pixel Circuit for Flexible Displays

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ABSTRACT In this paper, a self-compensating 6 thin-film transistor (TFT) pixel circuit with special layout considerations has been proposed to mitigate the impact of the electrical instability of hydrogenated amorphous silicon TFTs as well as applied mechanical strain. The proposed pixel circuit has been fabricated onto flexible polyethylene naphthalate (PEN) substrate and the measurement results demonstrated less than $\pm 3\%$ variation of its output current after an accelerated 24-h stress test under flat, tensile strain, and compressive strain conditions. In addition, the proposed pixel circuit only required a pair of signals to operate, which reduced the complexity on external IC drivers.

INDEX TERMS Pixel circuit, threshold-voltage shift compensation, mechanical strain, flexible display.

I. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) technology is a popular and inexpensive technology of choice to realize active-matrix liquid-crystal displays (AM-LCDs) [1], [2]. The technology has its advantages in low-temperature processing and excellent device uniformity in large-area fabrication. These advantages may facilitate the realization of next-generation flexible displays. Recent advancements in micro-light-emitting-diode (μLED) fabrication and transfer have enabled the possibility of integrating μLED onto a-Si:H TFT backplane to achieve low-power and flexible emissive displays [3], [4]. Unlike organic-LEDs (OLEDs), μLEDs are inorganic devices with much lower power consumption to reach equivalent brightness [5]. Thus, a-Si:H technology with relatively lower carrier mobility compared to low-temperature poly-silicon (LTPS) which is commonly used in OLED display for smart-phones, becomes a potent candidate for the backplane circuits.

Even though a-Si:H technology possesses great advantages to realize flexible backplane circuits, its shortcomings are also well known. The voltage-bias induced degradation of electrical stability causes a reduction of output current over-time. This behavior is mainly due to defect-creation and charge-trapping in the a-Si:H channel and the gate dielectric layers, respectively [6]. The degradation is usually modeled as a threshold-voltage shift (ΔV_T) [7], [8]. If left uncompensated, the degradation can result in brightness loss over-time and lead to shortened life-time of a display panel. A number of circuit solutions have been proposed to tackle this issue including reverse-bias annealing of the emitting TFT [9], sensing the ΔV_T of the emitting TFT using external ICs [10], internally sensing the ΔV_T using feedback TFTs [11], and charge-transfer using a correlation between driving and compensation TFTs [12]. All these methods have compensation capabilities to varying degrees. Their drawbacks include: complex control signals, added pixel circuit complexity, high cost of external CMOS circuits, and slower operating speed due to internal sensing and reverse annealing.

Furthermore, when fabricated onto flexible substrates, a-Si:H TFTs have another degree of variation due to applied mechanical strain. Tensile and compressive strains cause a-Si:H TFTs to degrade differently under constant voltage bias [13]. The orientation of the TFT also affects the degradation under bending [14], [15]. This additional factor should be taken into account when designing pixel circuits on flexible substrates.

This paper presents a charge-transfer self-compensating 6-TFT (6T) pixel circuit with only two control signals implemented on a flexible substrate. It provides reliable compensation performance when laid flat or under mechanical strain. The proposed pixel circuit operates under an enhanced

charge-transfer method to provide stable output current to the display media. The layout of the pixel is also specifically designed to mitigate the impact of bending on the circuit performance. The paper presents detailed operation of the 6T pixel circuit with various bending simulation and measurement results.

II. THE DESIGN OF THE SELF-COMPENSATING 6T PIXEL CIRCUIT

Based on the specific ratio of TFT degradation in linear and saturation modes [16], a 6T pixel circuit has been proposed to mitigate the impact of electrical instability of flexible a-Si:H TFTs. It provides enhanced compensation performance through a self-compensating charge-transfer process. In addition, special consideration to the layout of TFTs has been given to ensure the correct behavior of the pixel circuit under different bending conditions. Furthermore, only a pair of signals is sufficient to control a row of such pixels, which reduces the complexity of external row drivers compared with previous solutions [10]–[12].

The schematic and control signals of the 6T pixel circuit are shown in Fig. 1. T_0 is the driving TFT that supplies current to the LED. The compensation TFT (T_2), which has its source and drain shorted to form a metal-insulator-semiconductor (MIS) capacitor, is connected between the gate and source terminals of T_0 electrically and provides compensation during the charge-transfer process. Another MIS capacitor (T_3) is used to store data prior to the emitting phase. The remaining TFTs (T_1, T_4, and T_5) are designed to act as switches. The control signal V_1 is the row-select signal and V_2 is the boosting signal. The operation of the pixel circuit is divided into two phases: programming and emitting, which are explained below.

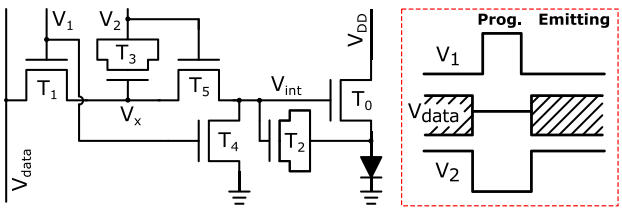

FIGURE 1. The schematic and control signals of the proposed 6T pixel circuit.

A. THE PROGRAMMING PHASE

In the programming phase shown in Fig. 2(a), control signal V_2 is set to low first so that T_5 is in high impedance mode which isolates the internal node V_{int} from the toggling V_{data}. At the same time, the gate voltage (V_x) of the storage capacitor T_3 is reduced and waiting for the new V_{data}. After a short delay, V_1 is set to high such that T_1 and T_4 are conducting. As a result, V_{int} node is drained through T_4 to clear the brightness level of the previous display cycle. When V_{int} reaches zero, T_0 is shut off and no current is flowing through the LED. Then, there will be no residual luminescence impact from the previous display cycle. Meanwhile, T_3 has acquired charge based on the new V_{data} value through T_1. In this phase, the reset of previous state and the acquisition of the new data are carried out without any cross-talk to neighboring pixels and power/ground rails.

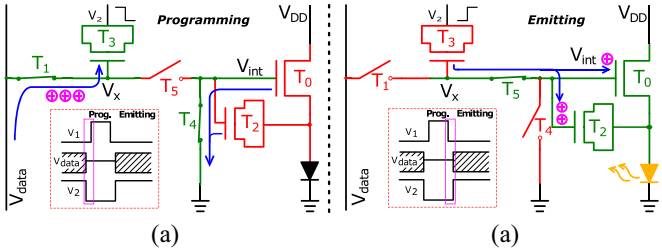

FIGURE 2. The switching behavior of TFTs and charge flow in the 6T pixel circuit in the (a) programming and (b) emitting phases. TFTs shown in red are turned off and shown in green are on. The charge flow is shown with blue arrows.

B. THE EMITTING PHASE

After the programming phase ends, the pixel enters the emitting phase, shown in Fig. 2(b), by switching the polarity of control signals V_1 and V_2 sequentially. This operation makes T_1 and T_4 in high impedance mode and T_5 conducting. Consequently, V_{int} is isolated from the interference of the toggling V_{data} signal and ground. Then, the majority of the charge on T_3 is injected to V_{int} and is stored on T_2, while a small portion is shared among parasitic capacitances of other TFTs.

C. THE CHARGE-TRANSFER SELF-COMPENSATING MECHANISM

The self-compensating charge-transfer mechanism of the proposed 6T pixel circuit is governed by balancing charge components and utilizing the ΔV_T ratio between T_2 and T_0. In the following analysis, the LED is neglected to ease the calculation because it has negligible impact on the compensation capability.

The derivation is to demonstrate that, under the same V_{data} voltage, the pixel circuit is always providing the constant current to the LED in spite of increasing $\Delta V_{T,0}$ conditions. Since the LED only glows in the emitting phase, all charge equations are based on transistor behaviors in this phase.

In the emitting phase, T_2 is operating in linear mode and T_0 in saturation mode, so that before any long-term voltage-bias stress (ΔV_T has not occurred), the initial charge in the channel of T_2 and T_0 is expressed as:

$$Q_{ch,2}^{initial} = C_{ch,2} \times \left(V_{int}^{initial} - V_{T,2}\right) \quad (1)$$

$$Q_{ch,0}^{initial} = \frac{2}{3} C_{ch,0} \times \left(V_{int}^{initial} - V_{T,0}\right) \quad (2)$$

In the above Eqs., $Q_{ch,2}^{initial}$ and $Q_{ch,0}^{initial}$ are the total charge in the channel of T_2 and T_0 at their initial state, respectively. $C_{ch,2}$ and $C_{ch,0}$ are the channel capacitance of these two

TFTs. The applied gate-source voltage and initial threshold voltages are expressed as $V_{int}^{initial}$ and $V_{T,2}$, $V_{T,0}$, respectively.

After the pixel circuit has been operated under voltage-bias stress, both T_2 and T_0 are degrading due to the disordered nature of the amorphous material [1], [17]. Consequently, the degradation causes ΔV_T on both T_2 and T_0. After biased-induced stress, the resulting new channel charge Eqs. become:

$$Q_{ch,2}^{stressed} = C_{ch,2} \times \left(V_{int}^{stressed} - V_{T,2} - \Delta V_{T,2}\right) \quad (3)$$

$$Q_{ch,0}^{stressed} = \frac{2}{3} C_{ch,0} \times \left(V_{int}^{stressed} - V_{T,0} - \Delta V_{T,0}\right) \quad (4)$$

The degradation of T_2 and T_0 still follows the correlation rule [16], where the degradation of a TFT in linear mode is 1.5 times faster than saturation mode when the gate bias voltage is the same. The correlation is expressed as:

$$\Delta V_{T,2} = \frac{3}{2} \Delta V_{T,0} \quad (5)$$

To achieve the self-compensating mechanism, $V_{int}^{stressed}$ should rise by the amount of $\Delta V_{T,0}$ from $V_{int}^{initial}$ automatically in the emitting phase. This relationship is expressed as:

$$V_{int}^{stressed} = V_{int}^{initial} + \Delta V_{T,0} \quad (6)$$

In order to realize the above relationship, the geometry of all TFTs needs to be designed correctly by balancing charge components in the emitting phase. As a result, the overlap capacitance that affects V_{int} node has to be also taken into account. The capacitor network in the emitting phase is shown in Fig. 3. It is assumed that the on-state of signal V_2 is equal to the supply voltage V_{DD}. The channel capacitance of T_5 is also neglected because its channel length is designed as minimum size to allow a fast charge-transfer from the programming phase to the emitting phase.

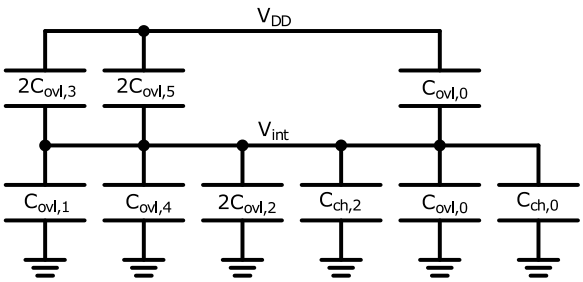

FIGURE 3. The channel and overlap capacitances that share charge in the emitting phase.

All the overlap capacitances between V_{DD} and V_{int} ($C_{ovl,top}$) from Fig. 3 are expressed as:

$$C_{ovl,top} = C_{ovl,0} + 2C_{ovl,3} + 2C_{ovl,5} \quad (7)$$

In addition, all the overlap capacitances between V_{int} and ground ($C_{ovl,bottom}$) from Fig. 3 are expressed as:

$$C_{ovl,bottom} = C_{ovl,0} + C_{ovl,1} + 2C_{ovl,2} + C_{ovl,4} \quad (8)$$

According to the law of charge conservation, the charge in the capacitor network is expressed as:

$$C_{ovl,top} \times (V_{DD} - V_{int}) = C_{ovl,bottom} \times V_{int} + Q_{ch,2} + Q_{ch,0} \quad (9)$$

$$C_{ovl,top} \times V_{DD} = \left(C_{ovl,top} + C_{ovl,bottom}\right) \times V_{int} + Q_{ch,2} + Q_{ch,0} \quad (10)$$

It is assumed that only the channel capacitances are affected by the threshold voltage but not the overlap. Also, due to the close proximity of T_2 and T_0 on the layout, their initial threshold voltages $V_{T,2}$ and $V_{T,0}$ are assumed equal. After substituting Eqs. (1) and (2) into in Eq. (10), the initial charge balance before any bias-stress can be expressed as:

$$C_{ovl,top} \times V_{DD} = \left(C_{ovl,top} + C_{ovl,bottom}\right) \times V_{int}^{initial} + C_{ch,2} \times \left(V_{int}^{initial} - V_{T,0}\right) + \frac{2}{3} C_{ch,0} \times \left(V_{int}^{initial} - V_{T,0}\right) \quad (11)$$

After substituting Eqs. (3), (4), and (5) into Eq. (10), the charge-balance Eq., after the bias-stress of the pixel circuit, becomes:

$$C_{ovl,top} \times V_{DD} = \left(C_{ovl,top} + C_{ovl,bottom}\right) \times V_{int}^{stressed} + C_{ch,2} \times \left(V_{int}^{stressed} - V_{T,0} - \frac{3}{2}\Delta V_{T,0}\right) + \frac{2}{3} C_{ch,0} \times \left(V_{int}^{stressed} - V_{T,0} - \Delta V_{T,0}\right) \quad (12)$$

A new relationship, after substituting Eqs. (11) and (12) into Eq. (6), is then obtained, which describes the relationship between capacitors. It is expressed as:

$$\frac{1}{2} C_{ch,2} = C_{ovl,top} + C_{ovl,bottom} \quad (13)$$

$$\frac{1}{2} C_{ch,2} = 2C_{ovl,0} + C_{ovl,1} + 2C_{ovl,2} + 2C_{ovl,3} + C_{ovl,4} + 2C_{ovl,5} \quad (14)$$

Here, Eq. (14) indicates that the geometry of the compensating TFT (T_2) is determined by the sum of overlap capacitances in TFTs (T_0, T_1, T_2, T_3, T_4, and T_5). Then, the capacitance values are substituted by the widths and lengths of relevant TFTs. In addition, the process parameters including the unit-square sheet capacitance of the channel (C_{ch}) and the overlap capacitance (C_{ovl}) are inserted in the Eq. (14). Lastly, the minimum overlap length L_{ovl} is dictated by the fabrication process. The relationship of capacitances shown in Eq. (14) is expressed as the channel width and length (W and L) of TFTs. The simplified Eq. (15) below serves the purpose to determine the sizes of TFTs in the 6T pixel circuit.

$$W_2 = \frac{2C_{ovl}L_{ovl}(2W_0 + W_1 + 2W_3 + W_4 + 2W_5)}{C_{ch}L_2 - 4C_{ovl}L_{ovl}} \quad (15)$$

The mathematical analysis has suggested that, with correct sizing, the circuit is capable to maintain the ΔV_T of

correlating T_2 and T_0 with a shift of the fixed 3 : 2 ratio. Therefore, the self-compensating mechanism is achieved by raising V_{int} with an amount equal to $\Delta V_{T,0}$ in the emitting phase. As a result, the output current is not affected by the bias-induced degradation of a-Si:H TFTs. Eq. (15) also provides information on L_{ovl} in terms of downsizing of TFTs. If a less overlap or a self-aligned process is used, the size of pixel TFTs, particularly T_2 and T_3 which are the largest TFTs in the pixel circuit, can be reduced. Indeed, a reduction in size can shrink the area occupied by the pixel circuit, thereby achieving a better fill factor.

D. IMPACT OF THE APPLIED MECHANICAL STRAIN

Previous reports [13], [18] have shown that, under tensile strain, the TFTs have slightly higher carrier mobility and much slower bias-induced degradation. On the other hand, when the TFTs are bent under compressive strain, they have slightly lower mobility and relatively faster bias-induced degradation. Such behavior of the TFT under bending could be explained by the defect creation model where the external strain is relieving or deteriorating the weak Si-Si bonds [13], [19]. Several reports [14], [15], [19] have further investigated the impact of orientation of TFTs under the applied mechanical strain. It has been found that when the bending direction is parallel to the current flow, *i.e.,* the TFT L direction, the impact of bending is at the highest, especially to the long-term biased-induced instability. When the bending direction is perpendicular to the current flow, the impact of mechanical strain is relatively less. As such, the layout of the pixel circuit should be given special consideration such that the correlating T_2 and T_0 are required to be in the same orientation and placed in close proximity. In this way, both TFTs experience the same mechanical strain so that their relative degradation ratio of 3 : 2 will be always maintained.

III. SIMULATION OF THE 6T PIXEL CIRCUIT

A charged-based level-61 a-Si:H TFT model [12], [14] was used to simulate the behavior of the 6T pixel circuit under different bending situations with increasing electrical instability. The circuit and its test-bench have been implemented in Cadence Virtuoso environment with parameters listed in Table 1. The process parameters (μ_{eff}, C_{ch}, and C_{ovl}) were obtained by extracting data from I-V and C-V curves of test TFTs with known geometries. The L_{ovl} was set to $5\,\mu m$. The W/L of T_0 was set to $100\,\mu m/20\,\mu m$ as a reference to size all other TFTs. Switches T_4 and T_5 were chosen to be $25\,\mu m/20\,\mu m$ and $25\,\mu m/10\,\mu m$, respectively, to minimize the pixel area guided by Eq. (15). Then, the size of T_2 was calculated to be $\approx 100\,\mu m/100\,\mu m$. Lastly, T_3 was chosen to match the size of T_2 to restore charge needed by T_2 in the emitting phase. Note that the maximum V_{data} needs to be less than the difference between the on-state of V_2 and the V_T of T_5 ($V_2^{high} - V_{T,5}$). This condition was to guarantee that the V_{data} is always fully transferred onto V_{int} in the emitting phase.

TABLE 1. Device and process parameters used in the simulation.

Parameter	Value	Parameter	Value
$W_0/L_0(\mu m/\mu m)$	100/20	$V_{data}(V)$	$5 \sim 15$
$W_1/L_1(\mu m/\mu m)$	50/20	$V_{DD}(V)$	20
$W_2/L_2(\mu m/\mu m)$	100/100	$V_1(V)$	$0 \sim 20$
$W_3/L_3(\mu m/\mu m)$	100/100	$V_2(V)$	$20 \sim 0$
$W_4/L_4(\mu m/\mu m)$	25/20	$\mu_{eff}(cm^2/Vs)$	1.0
$W_5/L_5(\mu m/\mu m)$	25/10	$C_{ch}(fF/\mu m^2)$	0.16
$L_{ovl}(\mu m)$	5	$C_{ovl}(fF/\mu m^2)$	0.22

First, to investigate the effectiveness of the self-compensating circuit on a flat substrate, $\Delta V_{T,0}$ was varied from $0\,V$ to $3\,V$ and $\Delta V_{T,2}$ from $0\,V$ to $4.5\,V$ to represent increasing electrical instability of the correlating TFTs. The simulation results indicated that the output current in the entire data range was able to retain more than 99% of its initial value when $\Delta V_{T,0} = 3\,V$ shown in Fig. 4.

Then, to simulate the impact of mechanical strain onto the flexible substrate, a higher $\Delta V_{T,0}$ value of $4\,V$ was chosen to represent a compressive stress and a lower $\Delta V_{T,0}$ value of $2\,V$ was chosen to represent a tensile stress. The mobility of the TFTs was also slightly adjusted due to bending. When placed under tensile strain, 0.3% was added to the TFT mobility, and when under compressive strain, 0.3% was subtracted from the original value [18], [19]. In order to maintain the desired correlation between $\Delta V_{T,2}$ and $\Delta V_{T,0}$, both T_2 and T_0 were assumed to have the same orientation and placed in close proximity in the layout. Therefore, their degradation could still have the 3 : 2 relationship. The pixel circuit was able to maintain $\sim$ 99% of its initial current under tensile and compressive stain tests shown in Fig. 4.

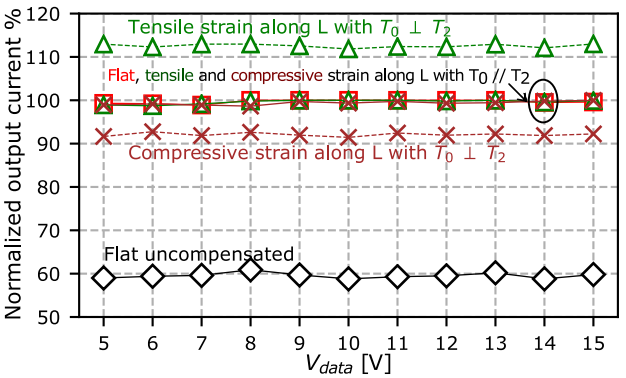

FIGURE 4. The simulation of normalized output current of the 6T pixel circuit in the entire V_{data} range under various bending conditions. The red, green, and brown solid lines show the compensation percentages under flat, tensile strain, and compressive strain conditions, respectively, when T_0 and T_2 are placed in parallel. The green and brown dashed lines represent the compensation under tensile and compressive strains, respectively, when T_0 and T_2 are placed perpendicularly. The black line shows a pixel circuit without compensation when placed flat.

Additionally, simulations with T_2 and T_0 having perpendicular orientation were conducted: the strain was applied in parallel to the L direction of T_0 and perpendicular to

the L of T_2. When tensile strain was applied, the pixel circuit exhibited over-compensation, showing that the output current was $\sim$ 112% compared to the initial value shown as the green dashed line in Fig. 4. This was due to $\Delta V_{T,2} : \Delta V_{T,0} > 3 : 2$, so that T_2 was providing more charge which raised V_{int} higher than expected. On the other hand, when compressive strain was applied, the pixel circuit demonstrated under-compensation. The output current only retained $\sim 92\%$ of its initial value due to $\Delta V_{T,2} : \Delta V_{T,0} < 3 : 2$ shown in as the brown dashed line in Fig. 4. The reason is that T_2 provided insufficient charge during the emitting phase, so that $V_{int}^{stressed}$ did not reach the correct value.

IV. FABRICATION, MEASUREMENTS, AND DISCUSSIONS

A. FABRICATION OF TFT PIXEL CIRCUITS

The 6T pixel circuits were fabricated using the conventional 5-mask back-channel-etched (BCE) a-Si:H TFT process on flexible polyethylene naphthalate (PEN) substrates at the maximum process temperature of 170°C. The cross-section schematic of the fabricated a-Si:H TFT and measured I_{DS} vs. V_{GS} curves are shown in Fig. 5(a) and (b), respectively. The test TFT showed carrier mobility (μ_{eff}) of $\sim 1\,cm^2/Vs$, sub-threshold slope (SS) $\sim 0.76V/dec$, and $V_T \sim 2.5\,V$. Details on the fabrication process can be found in [14].

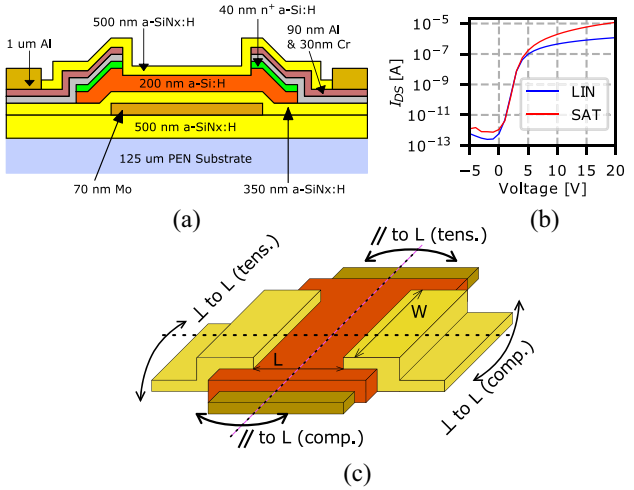

FIGURE 5. (a) The cross-section schematic of the TFT on flexible PEN substrate, (b) The I_{DS} vs. V_{GS} curves of the TFT ($W/L = 100\,\mu m/20\,\mu m$) in linear and saturation modes when laid flat, and (c) The schematic of various mechanical strain conditions applied to the TFT.

B. CHARACTERIZATION OF TFT STABILITY UNDER BENDING

The voltage-biased bending experiments of individual TFTs with four different modes have been conducted for three hours. The TFT was placed in tensile or compressive strain as well as in parallel or perpendicular to the L direction shown in Fig. 5(c). The output current was logged periodically and the result was compared with a flat TFT as reference.

The normalized drain-source current (I_{DS}) of test TFTs with the same geometry ($W/L = 100\,\mu m/20\,\mu m$) under four bending modes in saturation ($V_{DS} = 20\,V$ and $V_{GS} = 20\,V$) or linear ($V_{DS} = 1\,V$ and $V_{GS} = 20\,V$) voltage-bias condition is shown in Fig. 6. The bending radius was $\approx 40\,mm$ and the calculated strain was $\varepsilon = \pm 0.3\%$. TFTs under tensile strain showed lower bias-induced degradation compared to the reference flat TFT. On the other hand, compressive strain caused TFTs to degrade more under the same voltage bias. When the bending direction was in parallel with the L of TFTs, the impact of strain on degradation was generally more than the case of TFTs with strain perpendicular to L. Moreover, in all experiments, TFTs under linear mode were observed to degrade faster than in saturation mode under the same V_{GS}. The degradation ratio of linear to saturation modes was also confirmed to closely follow 3 : 2 [16] which is the crucial design parameter for the 6T compensation pixel circuit.

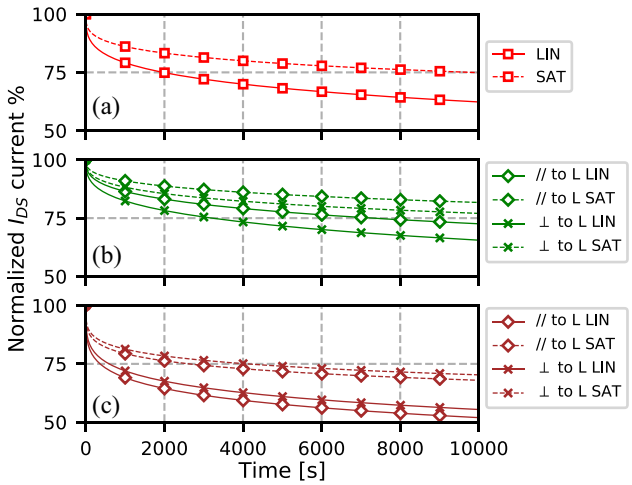

FIGURE 6. The normalized I_{DS} of a TFT ($W/L = 100\,\mu m/20\,\mu m$) under linear (LIN) and saturation (SAT) voltage-bias stress conditions for three hours when (a) laid flat, and under (b) tensile strain and (c) compressive strain. The bending experiments contain both configurations where the applied strain was parallel (//) and perpendicular (⊥) to L.

C. MEASUREMENT RESULTS OF THE 6T PIXEL CIRCUIT

The optical micro-graph of the fabricated 6T pixel circuit is shown in Fig. 7(a). The bending experiments were conducted by taping the substrate onto a convex (Fig. 7(b)) or a concave (Fig. 7(c)) metal sample holder with the same radius to obtain tensile or compressive strain, respectively. The power-supply voltage, data input, and control signals were generated according to Table 1 by an Arduino-Mega micro-controller with external digital-to-analog converters and operational amplifiers shown in Fig. 7(d).

The pixel circuit on the same PEN substrate was driven at the maximum $V_{data} = 15\,V$ to mimic a worst-case TFT degradation while laid flat and bent with tensile or compressive strain of 0.3% for 24 hours under 60 Hz frequency. Note that the bending direction was parallel to

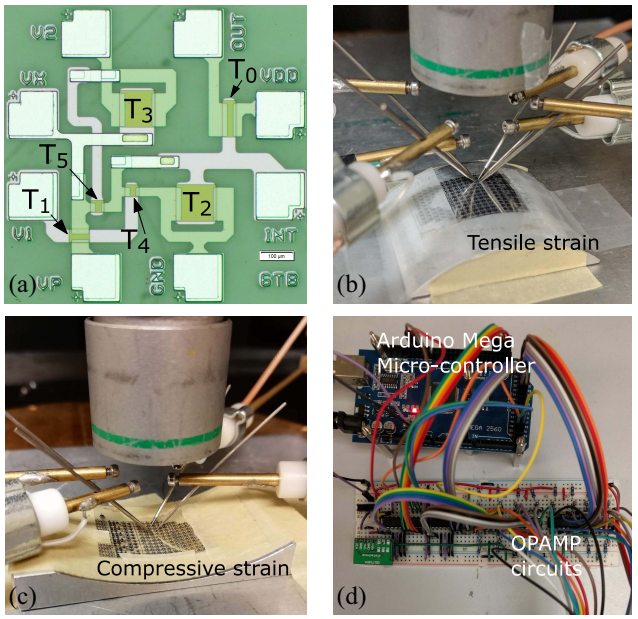

FIGURE 7. (a) A micro-graph of the pixel circuit, (b) The bending test setup with tensile strain, (c) The bending test setup with compressive strain, and (d) The Arduino Mega micro-controller and external IC components for control-signal generation and data logging.

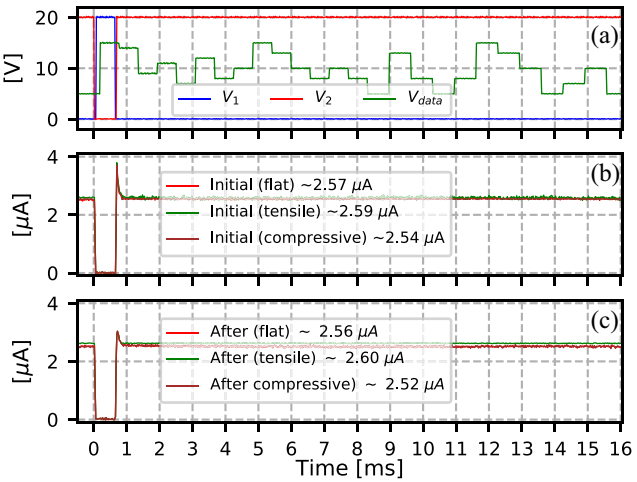

FIGURE 8. The measured transient waveforms of (a) the input signals. (b) The output current of the 6T pixel circuit at the initial time before bias stress. (c) The output current after 24 hours of bias stress test with maximum V_{data} when the pixel was laid flat, and under tensile and compressive strains.

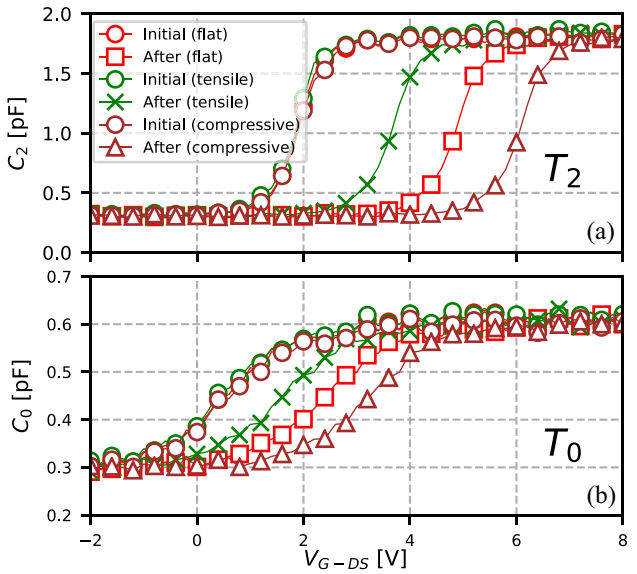

FIGURE 9. The C-V curves of the correlating TFTs (a) T_2 and (b) T_0 measured initially and after long-term (24 hours) bias-stress test under flat (red), tensile (green), and compressive (brown) strain conditions.

the L of T_0 and T_2 so that the impact of mechanical strain was at its maximum [13], [14]. The output current of the pixel circuit was logged every 10 minutes through an analog-to-digital converter on-board the Arduino-Mega micro-controller.

Fig. 8(a) shows the control signals of V_1, V_2, and V_{data}. The initial output current waveforms during a display cycle (60 Hz refresh rate) of the 6T pixel circuit are shown in Fig. 8(b). All three cases with the pixel circuit being laid flat, and under tensile strain and compressive strain showed a slight variation in the initial output current values due to mobility change under bending [18], [20]. After 24-hour bias stress, all the pixel circuits demonstrated the correct compensation behavior with less than $\pm 1\%$ variation (Fig. 8c)) compared to the initial output current values with the same strain conditions in Fig. 8(b). In contrast, the output current of a 2T uncompensated pixel circuit with the same initial current experienced more than 40% loss when placed flat (not shown here).

To investigate the effectiveness of the self-compensating charge-transfer mechanism of the 6T pixel circuit, C-V measurements were also performed on the correlating TFTs (T_2 and T_0). All the terminals of T_2 and T_0 were made available for probing in the pixel circuit shown in Fig. 7(a). According to Eq. (5), the correlation ratio should be $\Delta V_{T,2} : \Delta V_{T,0} = 3 : 2$ [16]. In the experimental results shown in Fig. 9 (a) and (b), when the pixel circuit was laid flat during the test, $\Delta V_{T,2} = 3.15\,V$ and $\Delta V_{T,0} = 2.08\,V$, and the correlation value was 1.51. When under tensile strain, the measured C-V curves showed $\Delta V_{T,2} = 1.78\,V$ and $\Delta V_{T,0} = 1.16\,V$, and the correlation value was 1.53. When under compressive strain, the C-V curves showed $\Delta V_{T,2} = 4.17\,V$ and $\Delta V_{T,0} = 2.80\,V$, and the correlation value was 1.49. As a result, in all three long-term bias stress experiments, the 6T pixel circuit demonstrated the correct correlation between T_2 and T_0, which provided the desired compensation behavior regardless of strain situations.

Three additional experiments with random V_{data} were also conducted with flat, tensile strain, and compressive strain conditions on the pixel circuit to verify the compensation capability in the entire data range after bias-stress for 24 hours. Fig. 10 shows the results of the 6T pixel circuit in

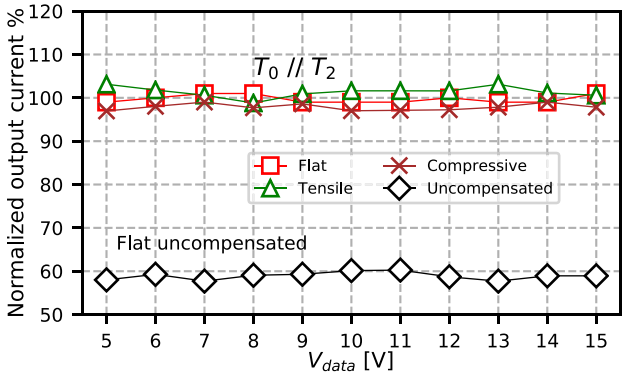

FIGURE 10. The normalized output current of the 6T pixel circuit for the entire V_{data} range after bias-stressed for 24 hours under flat (red), tensile strain (green), and compressive strain (brown) conditions along with the 2T uncompensated pixel circuit under flat condition.

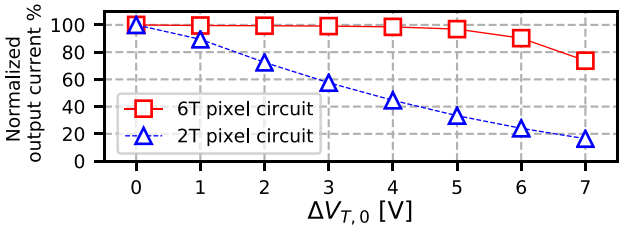

FIGURE 11. The simulation of normalized output current of the 6T pixel circuit and 2T uncompensated pixel circuit with increasing $\Delta V_{T,0}$ under flat condition at maximum $V_{data} = 15\,V$.

comparison with the 2T uncompensated pixel circuit under flat condition. Note that the proposed pixel circuit exhibited less than ±3% of variation for all the situations while the output current of the uncompensated 2T pixel circuit was reduced by ∼ 40%.

D. DISCUSSIONS

The proposed 6T pixel circuit was compared with existing compensation methods in terms of number of TFTs, control signals, and performance. The result is summarized in Table 2. The 6T pixel circuit has the least amount of control signals and average TFT count. Its footprint is also comparable to other charge-transfer pixel circuits and much less than the ones using other compensation methods. The compensation performance under flat and bending situations is superior to the reported solutions, demonstrating the efficacy of the proposed self-compensating pixel circuit for flexible displays.

TABLE 2. Comparison of compensation pixel circuits.

	This Work	Lee [2017]	Yang [2012]	Oh [2012]	Ashtiani [2007]	Lee [2005]
Technology	**a-Si:H**	a-Si:H	a-Si:H	a-Si:H	a-Si:H	a-Si:H
Substrate	**PEN**	PEN	Glass	Glass	Glass	Glass
Compensation Method	**Charge transfer**	Charge transfer	Charge transfer	External sensing	Internal sensing	Reverse anneal
# of TFTs	**6**	4	4	4	5	7
# of signals	**2**	3	3	4	3	3
Footprint (mm^2)	**0.024**	0.021	0.023	0.054	0.036	0.058
Flat	**±1%**	±5%	±3%	±2%	±5%	±6%
Bending	**±3%**	±10%	N/A	N/A	N/A	N/A

To further investigate the limitation of the 6T compensation pixel circuit, higher $\Delta V_{T,2}$ and $\Delta V_{T,0}$ values were applied to the simulation test-bench, while keeping the correlation ratio of 3 : 2. Fig. 11 shows the simulation of normalized output current of the 6T compensated and 2T uncompensated pixel circuits with a $\Delta V_{T,0}$ range from 0 V to 7 V under flat condition. The simulation assumed a maximum $V_{data} = 15\,V$ to mimic the worst-case degradation. It was observed that the compensation started to lose its effectiveness above $\Delta V_{T,0} = 5\,V$. This phenomenon can be explained by the charge model of TFTs. Since the proposed compensation mechanism is to raise $V_{int}^{stressed}$ according to $\Delta V_{T,0}$, $V_{int}^{stressed}$ from Eq. (6) becomes $20\,V$ at $\Delta V_{T,0} = 5\,V$. This has made the difference between gate and drain terminals of T_0 almost zero. As a result, T_0 is no longer in saturation mode when $\Delta V_{T,0}$ is beyond 5 V. Therefore, the correlation of $\Delta V_{T,2} : \Delta V_{T,0}$ becomes less than 3 : 2, decreasing the compensation capability.

In addition to the consideration of the $\Delta V_{T,0}$ limitation, the change of correlation ratio has impact on the design of the 6T pixel circuit. When the correlation ratio is more than 3 : 2, the size of T_2 and T_3 can be reduced because more charge from T_2 is supplied to facilitate the compensation. However, if the correlation ratio is less than 3 : 2, the size of T_2 and T_3 should be increased to reach the desired compensation based on Eq. (15). In this case, the allowed area of the pixel circuit on the display panel dictates the size of T_2 and T_3.

On the other hand, interests in 4K display, augment-reality (AR), and virtual-reality (VR) equipment have been recently growing, which requires faster operating speed and denser pixel displays. Despite the low carrier mobility of the a-Si:H TFTs, if they can be fabricated with design rules of $L_{ovl} = 1\,\mu m$ and a minimum L of $5\,\mu m$, the footprint can be reduced to $\sim 1070\,\mu m^2$, which is less than 5% of the original size. The simulation assumed that the W/L of T_0 remains the same, while other TFTs were sized according to Eq. (15). Moreover, the significant reduction in L_{ovl} can allow the pixel circuit to be operated at a higher frequency. In the proposed 6T pixel circuit, the speed is determined by the RC time constant when T_1 is charging the storage capacitor T_3. If a $1\,\mu m$ overlap design rule is assumed, the simulated worst-case charging time is less than $3\,\mu s$ satisfying the requirement for $200\,Hz$ refresh rate in a 2K display panel. However, if used in a $400\,Hz$ 4K display with more demanding requirements, a-Si:H technology would not be the ideal solution. In this case, high-mobility TFTs made by metal-oxide or LTPS technologies [21] could reduce the size of pixels and increase the operating speed, which satisfy the requirement for high-resolution displays.

V. CONCLUSION

In conclusion, the self-compensating 6T pixel circuit with only two control signals has demonstrated excellent compensation capability on flexible PEN substrate under mechanical strain through a reliable charge-transfer process and careful consideration of the layout. Only ±3% variation from the initial output current was observed after long-term bias stress under various bending conditions. The mechanical manipulation also allows novel approaches to the design, sizing, operation, and control of the circuit, allowing a new degree of freedom that may be utilized through mechanical bending to regulate the circuit performance for flexible display applications.

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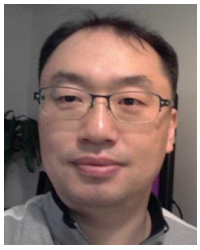

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