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Ultra Low-Loss Si Substrate for On-Chip UWB GHz Antennas

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ABSTRACT In this paper, measurements and simulations of miniature monopole antennas for ultra-wideband (UWB) GHz intra- and inter-chips communication and biomedical applications are presented. Folded designs on four substrates are studied: 1) standard bulk; 2) high-resistivity bulk; 3) ultra low-loss radiofrequency silicon-on-insulator (RF SOI); and 4) quartz. Among the Si-based substrates, RF SOI with its trap-rich sublayer demonstrates the best performances with the lowest RF power losses and centimetric transmission distance between antennas. Transmitted power between two antennas was measured from 0.01 to 20 GHz. Using substrate characterization of resistivity, permittivity, and loss tangent based on measured coplanar waveguide lines on the same substrates, good agreement is obtained between the return losses of simulated antennas on each substrate and numerical solutions, confirming the impact of the substrate properties. An antenna bandwidth of 680 MHz is demonstrated at 6.0 GHz meeting the criterion for UWB radio communications in the 6–10 GHz band.

INDEX TERMS Radiofrequency, semiconductor materials substrate, silicon-on-insulator, device-to-device communication, ultra-wideband antennas.

I. INTRODUCTION

The association of CMOS technologies with radio communications has enabled miniature single-chip tags and the emergence of new possibilities for intra- and inter-chips signal distribution [1], [2] or in-situ biomedical applications [3]. On-chip integrated antennas allow avoiding external communication lines and sophisticated packaging, minimizing the total footprint and losses. In particular, they represent a good solution for short-distance ultra-wideband (UWB) communications, up to 10 cm [4], [5]. However, a trade-off has to be found between size, bandwidth and efficiency, especially when the antenna dimensions become smaller than the wavelength.

The two typical methods to reduce the antenna footprint are to apply a geometrical tuning such as slot, zigzag and meander designs, or to modify materials to increase the substrate permittivity. However, a high permittivity induces an efficiency drop due to the capacitive coupling between the antenna and the ground and limits the matching in a large frequency band [6]. Kulkarni *et al.* [5] present a folded monopole antenna on 1.3 µm-thick SiO_2 with radiation efficiency of −22 dB over the 6–10 GHz band, with ground plane applied through the Si substrate. Indeed, monopole antennas benefit from two advantages: (i) half the size of that of dipole antenna and (ii) no need for a balun. However, their protruding geometry often disqualifies them in practice. A comparison of passive RFID tags with on-chip antenna on Si and quartz substrates, with a 5 GHz working frequency on Si is shown in [7]. Intra-chip radio communications on 5 kΩ·cm Si substrates with 2 µm-thick thermal SiO_2 as an insulating layer has be demonstrated in [8]. State-of-the-art literature [5]–[8] discusses miniaturized antennas performances on different substrates, from bulk Si to high resistivity Si or quartz, but not yet the ultra-low-loss trap-rich (TR) HR-SOI substrate [9] which we introduce here. The on-chip antenna fabrication is presented in Section II, the

substrate characterization in Section III, and the modelling and experimental antenna performance on different substrates in Section IV.

II. FABRICATION

In this paper, three types of Si-based substrates and a quartz lossless reference substrate are compared. We patterned the antennas and coplanar waveguide (CPW) line structures after aluminum e-gun evaporation of 1.25 μm and 1.36 μm-thickness on Si-based and quartz substrates, respectively. The three Si-based substrates under consideration in this work are: standard bulk p-type silicon, high-resistivity (HR) silicon and trap-rich (TR) HR-SOI. Table 1 gives the main characteristics of the four substrates compared in this study.

TABLE 1. Substrates parameters.

Substrate	ε_r	Bulk thickness (μm)	ρ (Ω.cm)	SiO_2 layer
Bulk Si	11.8	380	10-20	400 nm (thermal)
HR Si	11.8	380	>4000	300 nm (PECVD)
TR HR-SOI	11.8	725	>3000	320 nm (thermal)
Fused quartz	3.9	500	$>10^{12}$	-

Standard bulk silicon wafers have typically low resistivity values (in the range of 10 Ω.cm), which make them very lossy and non-ideal for RF applications. Reducing significantly the nominal doping gave rise to the HR-Si substrates. Such substrates are also unsuited to RF applications due to the parasitic surface conduction (PSC) effect that arises when a large amount of free carriers is attracted to the oxide-handle Si substrate interface to counter-balance the fixed charges present within the oxide [10]. This PSC layer renders the HR-Si solution barely any more performant than the standard silicon bulk, as it is responsible for low substrate effective resistivity and high RF substrate losses. Trap-rich substrates overcome this effect with the introduction of a defect layer, rich in traps, composed of polysilicon or amorphous silicon. Deep-level traps provide a mechanism for compensating the fixed oxide charges without strong variations in the surface Fermi level, i.e., without a large amount of free carriers, ensuring a highly resistive state at the oxide interface. Consequently, TR HR-Si or SOI substrates boast highly increased effective resistivity, along with strongly decreased RF losses and substrate crosstalk levels.

The TR HR-SOI substrate used here is composed successively of a Si handle substrate, a trap-rich 1.8 μm-thick polysilicon layer and a 320 nm-thick thermal buried oxide (BOX) layer, while the initial 160 nm-thick conductive Si top layer was completely etched using TMAH.

The substrate backside is metallized with a 1 μm-thick aluminum layer. In Table 1, thermal and PECVD (plasma-enhanced chemical vapor deposition) terms refer to the oxide layer growth or deposition technique on Si.

Figure 1 presents the three folded monopole antennas that were designed with coplanar feed lines. That antenna design was initially proposed in [5] for impulse-response UWB communication. They are labelled as R1, R2 and R3 with lengths equal to 5.325, 9.025 and 12.725 mm, respectively. All aluminum lines are 100 μm-wide. The gap *d* represents the distance between two side-by-side antennas during S_{21} and S_{12} transmission measurements.

The main objective of the article being to demonstrate and model the performance of the new ultra-low loss TR HR-SOI substrate for on-chip antennas, the optimizations of the antenna design and performance have not been considered at this stage. The antenna geometry can be folded around the circuitry in a monolithic design and its footprint further reduced by decreasing the width (10 μm in [5]).

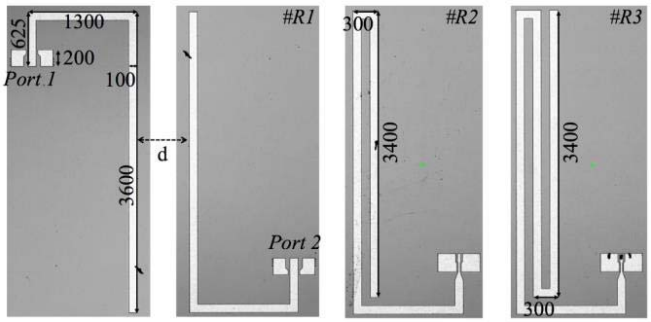

FIGURE 1. R1, R2 and R3 monopole antenna designs (dimensions in μm).

III. SUBSTRATE CHARACTERIZATION TOWARDS ANTENNA DESIGN

The four considered substrates were electrically characterized over a wide frequency band using coplanar waveguide (CPW) transmission lines fabricated alongside the antennas. S-parameter measurements of CPW lines enable the extraction of relevant substrate parameters for on-chip antenna design such as the substrate effective resistivity and RF losses, and substrate effective permittivity, based on the method described in [11]. The dimensions of the measured 50 Ω CPW lines are: a central signal line width of 38 μm, ground line widths of 213 μm, a spacing of 18 μm between the signal line and the ground lines, and an effective line length of 1880 μm.

On-wafer S-parameter measurements were performed using an Agilent N5242A PNA-X vector network analyzer (VNA) in the frequency range between 10 MHz and 20 GHz. A pair of GSG 67 GHz infinity probes from Cascade Microtech with 100 μm-pitch along with a shielded PM8 probe station were used. The reference planes at the probe tips are determined by the short-open-load-thru (SOLT) calibration method. The method developed in [12] is used to extract the equivalent RLGC parameters of the transmission line from the measurements of a 162 μm-long thru and a 2042 μm-long CPW, yielding the effective line length of 1880 μm. Fig. 2 (a), (b), (c), (d) presents the results from the extracted RLGC parameters of the CPW lines on the four considered substrates. The substrate's effective parameters, the effective resistivity (ρ_{eff}), the real part

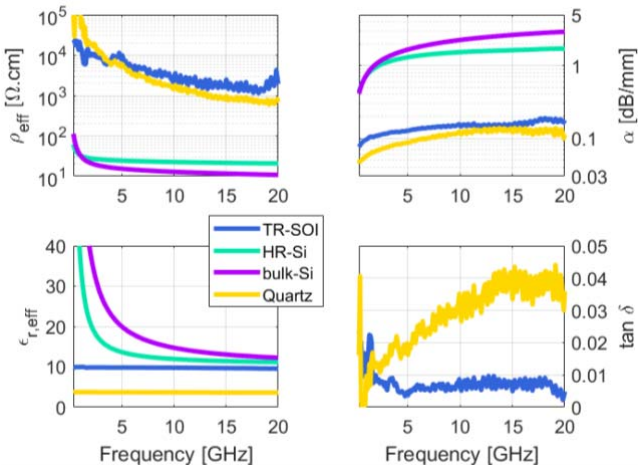

FIGURE 2. RF losses, effective permittivity, resistivity and loss tangent comparison for the different substrates.

of the effective relative permittivity ($\varepsilon'_{r,eff}$) and the loss tangent sensed by the CPW lines over each substrate are plotted at the upper left-hand window, lower left-hand window and lower right-hand window, respectively. The lineic loss of the lines, α, is plotted in the upper right-hand window. Only the loss tangent of the TR HR-SOI and the quartz substrates are presented, as they have the lowest substrate losses.

The extracted effective resistivity sensed by our CPW device on standard bulk Si substrate is in the range of 10 Ω.cm, which leads to high RF losses in the range of 2.6 dB/mm at 15 GHz.

In the HR substrate, without the trap-rich layer, the PSC effect induced by fixed charges at the oxide/Si interface [9] is responsible for still relatively high RF losses. Besides, low effective resistivity (20 Ω.cm) of relatively poor performance, similar to that of the standard bulk Si substrate, is observed.

The TR HR-SOI substrate eliminates the PSC effect with the addition of a high defect density layer beneath the BOX and above a high nominal resistivity silicon bulk. Consequently, the TR HR-SOI provides a ∼100x higher effective resistivity and ∼10x lower RF propagation loss coefficient α than bulk Si, i.e., from 1.37 dB/mm to 0.13 dB/mm at 6 GHz. RF losses on quartz substrate, given as a reference, are the lowest and are due almost purely to series metallic losses of the CPW line. However this substrate is not compatible with monolithic CMOS integration.

The apparent decay in effective resistivity with frequency for the TR HR-SOI and quartz substrates is due to non-negligible dielectric losses compared to conductive losses. In that case, the loss tangent is a more suitable RF figure of merit, as it includes both contributions:

$$\tan\delta = \frac{\rho_{eff}^{-1}}{\omega_0 \epsilon'_{r,eff}} + \frac{\epsilon''_{r,eff}}{\epsilon'_{r,eff}}.$$

Curve fitting of the loss tangent provides an extracted imaginary part of the effective relative permittivity ($\epsilon''_{r,eff}$) of 0.05 and 0.14 for the TR HR-SOI and the quartz substrates, respectively.

The peak in the loss tangent ∼1.3-1.5 GHz and its decrease above 17 GHz are artifacts related to the extraction method and are not further considered here.

IV. ON-CHIP ANTENNA PERFORMANCE

A. MEASUREMENT AND SIMULATION ENVIRONMENTS

S-parameters of the monopole antennas were measured on-wafer using the same equipment and techniques as described in Section III for the CPW lines. Furthermore, all three antennas were simulated on the TR HR-SOI wafer using the method of moments-based software Momentum ADS from Keysight.

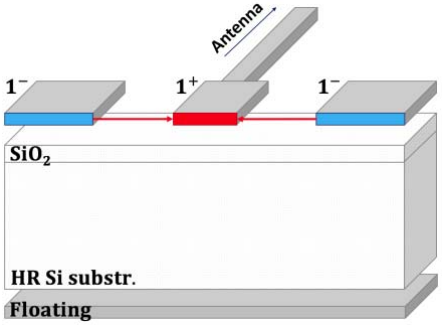

FIGURE 3. 1-port definition of the structure and its boundary conditions.

The substrate was defined as having a 320 nm BOX and an underlying silicon bulk layer defined with a resistivity of 4 kΩ.cm, a relative permittivity of 11.7 and a loss tangent of 0.01. These values were extracted from the CPW line measurements that were discussed in Figure 2, and which enable a calibration of our electromagnetic simulations.

Additionally, a floating RF metallic plane is defined below the substrate in the simulation set-up, as can be seen in Figure 3. This boundary condition represents the die backside and the probe station metallic chuck of the test set-up, which are not connected to the 1^- terminals of the RF measurement port. The excitation to the antenna is fed through a coplanar port, defined between terminals 1^+ and 1^-.

B. TR HR SOI ANTENNA MEASUREMENTS

The RF measurements in Figure 4 reveal good performance of the three monopole antennas integrated on the high-quality TR HR-SOI substrate. R1, R2 and R3 present low S_{11} return loss at their respective resonance frequencies (f_0), which are defined as the frequencies at which the imaginary part of the antenna input impedance crosses zero. The real part is then defined as the antenna radiation impedance (Z_R) at that frequency. The usable bandwidth (BW) around each resonance frequency f_0 is defined as being the frequency range over which the antenna return loss is below −10 dB (in a 50 Ω system). Classically, the fundamental resonance frequency BW is the one of interest for transmission. The S_{11} measurements of R1, R2 and R3 antennas, with increasing

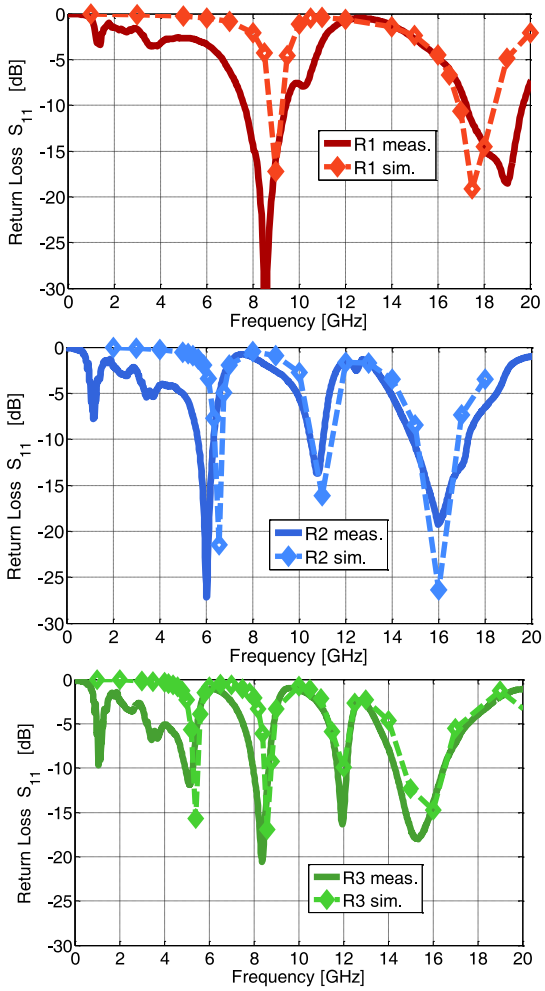

FIGURE 4. Reflection coefficient: RF measurements and simulations of the R1, R2 and R3 on-chip antennas on the TR HR-SOI substrate.

lengths, show the expected resonance frequency reduction. However, increasing the folding also narrows the bandwidth for the fundamental resonance frequency. As can be seen from Figure 4, antennas R1, R2 and R3 present, respectively, 2, 3 and 4 resonance frequencies below 20 GHz.

The Momentum ADS simulations run on the calibrated TR HR-SOI substrate (using results from Section III) are in good agreement with the measurement data, confirming the antenna designs and substrate modeling.

Table 2 lists the resonance frequencies of each antenna on TR HR-SOI and details the observed bandwidth and radiation impedance at each frequency. It is shown that the designed antennas on TR HR-SOI easily achieve large bandwidths from several hundred MHz up to a few GHz, meeting the criterion for UWB radio communications in the 6–10 GHz band (i.e., larger than 500 MHz). This higher band, less explored, presents some advantages such as less interference with other wireless bands, such as WiMAX [5].

C. SUBSTRATE IMPACT ON ANTENNA PERFORMANCE

Figure 5 presents good agreement between measured and simulated return loss S_{11} of antenna R2 implemented on

TABLE 2. Measured antenna on TR HR-SOI at S_{11} minima.

R1	f_0 [GHz]	8.55	19.10	/	/
	Z_R [Ω]	51.7	64.6	/	/
	BW [GHz]	1.80	2.43	/	/
R2	f_0 [GHz]	6.04	10.76	16.4	/
	Z_R [Ω]	54.3	32.9	67.9	/
	BW [GHz]	0.68	0.54	2.38	/
R3	f_0 [GHz]	5.15	8.41	11.88	15.70
	Z_R [Ω]	84.2	61.5	34.5	67.9
	BW [GHz]	0.34	0.71	0.44	2.20

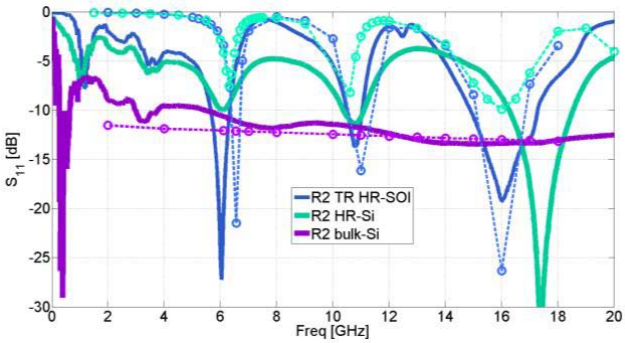

FIGURE 5. Measured (solid lines) and simulated (dashed lines) return loss for R2 on different substrates.

different Si substrates. Low values of S_{11} for our R2 antennas indicate either efficient radiation or high substrate losses. The results on TR HR-SOI show deep minima in the return loss at the antenna resonance frequencies, and reflection coefficients of −0.75 dB to −1.5 dB between these resonance frequencies. These high values indicate that little loss occurs in the TR HR-SOI substrate. The measured values on HR-Si however show reflection coefficients of −4.0 to −5.0 dB between the resonance frequencies, indicating significant substrate loss. The radiation will be less efficient on HR-Si due to these losses, and they are one of the reasons for which the return loss curves at resonance frequencies are not as deep as for the TR HR-SOI. As a result, HR-Si does not meet the requirements for UWB communication. The results from the antenna implemented on standard bulk-Si reveal extremely high substrate loss, with inefficient radiation.

D. 6 GHZ TRANSMISSION WITH TR HR-SOI ANTENNAS

To confirm the high radio-communication performance for the selected R2 antenna design on TR HR-SOI, the S_{21} transmission parameter was measured between two antennas in free-space medium. Figure 6 presents the effect of distance on the S_{21} transmission and demonstrates peak power transmission of −33.2 and −40.8 dB at 6.2 GHz between two R2 TR HR-SOI antennas located at 1 and 2 cm distance, respectively.

This is in the band of interest for UWB communication applications, and corresponds to the fundamental

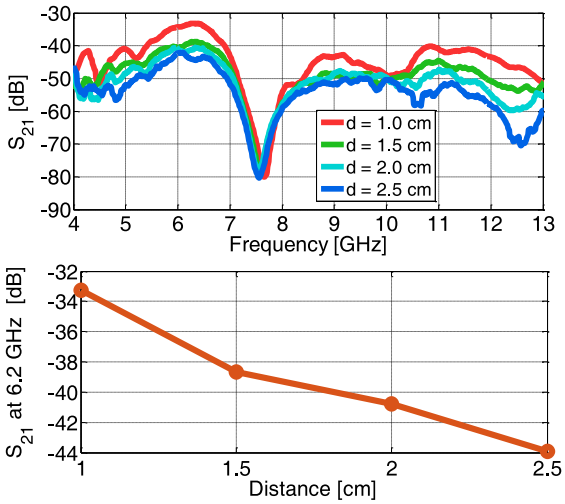

FIGURE 6. S_{21} **measurements between two R2 antennas on TR HR-SOI: versus frequency at various distances (top) or versus distance at 6.2 GHz (bottom).**

resonance frequency of the R2 antenna (see S_{11} in Fig. 3). The R2-to-R2 transmission experiment on TR HR-SOI provides S_{21} performance proving possible centimeter-communications with S_{21} values superior than −50 dB, distance further extendable with insertion of an LNA at the receiver [14], [15]. Moreover, improvements are expected in the case of intra-chip communications with a monolithic design [14]. Besides, low and constant group delay is of high importance for reliable UWB communication. Our measurements demonstrate excellent average and variation results below 0.5 ns and 100 ps respectively.

For transmission measurements, various distances, *d*, between two side-by-side R2 antennas with the same design are used. Millimeter antenna dimensions require proper probing to minimize parasitic wires or lines, only possible in a probe station.

In case of communication with a bio-implant, the second antenna, at the data receiver, does not have to fulfill the footprint constraints imposed on the on-chip emitter antenna. Consequently, a higher transmission efficiency can be achieved to partially compensate for the absorption by biological tissues.

V. CONCLUSION

The monopole antennas on trap-rich high-resistivity SOI substrate presented in this paper take advantage of the excellent substrate insulation against RF losses. This demonstrates for the first time the superior performance of that substrate, as compared to bulk and HR substrates, for antenna applications. Centimetric distance S_{21} transmissions were proven, with suitable S_{11} bandwidth for UWB communications in the 6–10 GHz band. ADS S_{11} simulations are in fair agreement with measurements, confirming the impact of substrate properties on antenna efficiency.

The miniature footprint enables on-chip integration, opening new perspectives for intra and inter-ICs communications and passive bio-implant in confined places such as brain, eye and veins.

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