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A Low-Power Thin-Film Si Heterojunction FET Noise Amplifier for Generation of True Random Numbers

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ABSTRACT A low-power noise amplifier is implemented with thin-film Si heterojunction field-effect transistors (HJFETs) and its suitability for generation of true random numbers is investigated. The HJFETs are operated at near subthreshold to obtain a large output resistance and therefore a high intrinsic gain at a low operation power. It is found that the noise output of a proof-of-concept 4-stage amplifier with a voltage gain of ∼5000, bandwidth of ∼1 KHz, power consumption of ∼100 nW, and a dc-blocking output capacitance of 250 pF is suitable for generation of statistically true random numbers at a rate of 100 bit/s without requiring post-processing. The described technique may find application in emerging technologies, such as large-area, flexible, and/or wearable devices that benefit from enhanced security and low-power computing.

INDEX TERMS 1/f noise, operational amplifiers, random number generation, silicon devices, thin film transistors.

I. INTRODUCTION

Random numbers are widely used for encryption of data and various computation techniques. Similarly, emerging technologies in large-area, flexible and/or wearable electronics can benefit from enhanced security and computing capability [1]–[3]. These technologies often require lightweight, ultrathin and/or flexible components that operate at several orders of magnitude lower frequencies than traditional technologies but require very low operation powers. While it is possible to implement some of these components as application-specific CMOS chips for external mounting, monolithically-integrated implementations with thin-film transistors (TFTs) can greatly reduce system complexity, weight, rigidness and cost. But the relatively low TFT performance, compared to CMOS, limits the feasibility of such implementations.

In contrast to pseudo-random numbers which are generated in software and therefore inherently deterministic, true random numbers are generated in hardware and based on inherently stochastic nature of physical phenomena. However, efficient acquisition and processing of weak random signals can be challenging especially under area, power and/or device performance constraints. The most widely used source of physical randomness is thermal noise, for example of a resistor, either directly by sampling after amplification [4], [5], or indirectly by supplying the thermal noise to an oscillator and sampling the resulting phase noise (jitter) [6], [7]. A fully digital approach based on supplying thermal noise to metastable cross-coupled inverters has also been demonstrated [8]. The direct amplification method is susceptible to substrate signals, coupling noise from digital components and amplifier finite bandwidth, which limit its application in high frequency integrated circuits (ICs). However, the required hardware is sufficiently simple for implementation with TFTs for low-frequency applications. In contrast, oscillator sampling and fully digital methods are more suitable for high-frequency ICs but require more sophisticated hardware. This is in part because improving the statistical randomness of jitter and compensating for mismatch between cross-coupled inverters requires additional processing.

In this paper, a low-power multi-stage noise amplifier is implemented with thin-film Si heterojunction field-effect transistors (HJFETs), and its suitability for generation of true

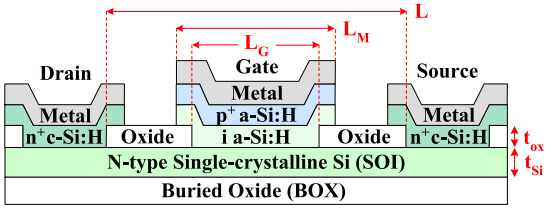

FIGURE 1. Schematic cross-section of the fabricated HJFETs with $t_{Si} = 32$nm, $t_{ox} = 50$nm, and c-Si (SOI) doping of $N_D \approx 10^{18}$ cm^{-3}.

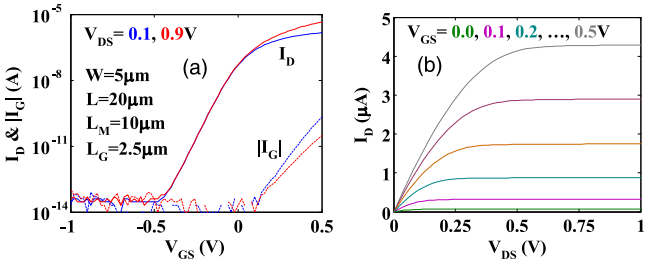

FIGURE 2. Measured (a) transfer and (b) output characteristics of the fabricated HJFETs.

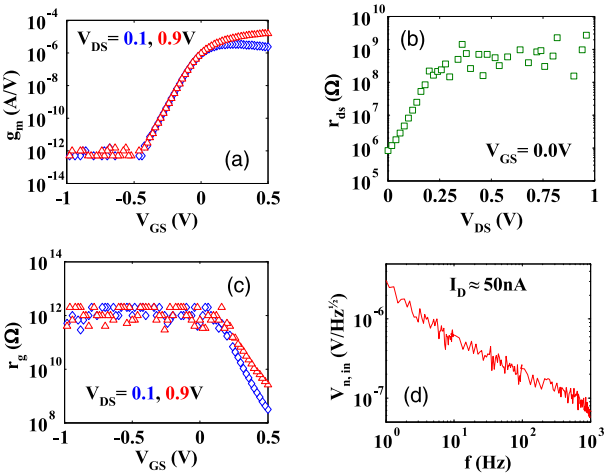

FIGURE 3. Extracted small-signal (a) transconductance, (b) output resistance and (c) gate resistance; and (d) measured low-frequency noise spectrum of the fabricated HJFETs converted to input-referred noise voltage.

random numbers is investigated. The flicker (1/f) noise of the HJFETs is used as the noise source, since it is much stronger than thermal noise at low frequencies. Biasing the HJFETs at near subthreshold allows a large output resistance and therefore a high intrinsic gain of ∼200. The large output resistance allows a sufficiently small DC-blocking capacitor to be used at the amplifier output for suppressing near-DC frequencies. A 4-stage HJFET amplifier with a bandwidth of ∼1 KHz, voltage gain of ∼5000, power consumption of ∼100nW, and a DC-blocking capacitance of 250pF is found to be suitable for generation of true random numbers at a rate of ∼100 bit/sec without requiring post-processing.

II. DEVICE CHARACTERISTICS

The schematic cross-section of an HJFET fabricated on a Si-on-insulator (SOI) substrate is shown in Fig. 1. The fabrication process is the same as that described in [9] and [10] with additional optimizations. The basic structure (and therefore operation principles) of an HJFET is the same as that of a conventional junction FET (JFET) except that the gate of an HJFET is comprised of a hydrogenated amorphous Si (a-Si:H)/crystalline Si (c-Si) heterojunction, whereas the gate of a JFET is comprised of a c-Si/c-Si homojunction. The a-Si:H and hydrogenated crystalline Si (c-Si:H) layers are grown by plasma-enhanced chemical vapor deposition (PECVD) at ∼200°C. Despite the low process temperature, HJFETs have a high electrical stability due to the high quality of the a-Si:H/ c-Si interface. HJFETs may also be fabricated on poly-Si substrates [11]. If poly-Si is prepared by pulsed laser crystallization, HJFETs are expected to be compatible with flexible plastic substrates. Thin layers of c-Si transferred and bonded onto flexible plastic substrates are also expected to be a viable option. In this work, HJFETs fabricated on SOI substrates are used for proof of concept.

The transfer and output characteristics of a fabricated HJFET are plotted in Figs. 2(a) and (b), respectively. The HJFET has a small pinch-off voltage of $V_p \approx 0.0$V and a near-ideal subthreshold slope of $SS \approx 65$ mV/dec. The drain current, I_D is saturated to ∼50nA at $V_{GS} = 0.0$V for $V_{DS} >> 26$mV. The extracted transconductance ($g_m = \partial I_D/\partial V_{GS}$), output resistance ($r_{ds} = [\partial I_D/\partial V_{DS}]^{-1}$) and gate resistance ($r_g = [\partial I_G/\partial V_{GS}]^{-1}$) are plotted in Figs. 3(a), (b) and (c), respectively. At $V_{GS} = 0.0$V and $V_{DS} \geq 0.2$V, $g_m \approx 1\mu$A/V and $r_{ds} \geq\sim 200$MΩ, and therefore the intrinsic gain, $g_m . r_{ds} \approx 200$. The r_g is very large at negative and small positive V_{GS}. The drain current noise spectrum (S_I) was measured using a low-frequency noise analyzer and converted to input-referred noise voltage, $V_{n,in} = S_I^{1/2}/g_m$ (Fig. 3(d)). The integrated noise in the range of 1Hz-1KHz is ∼5μV$_{rms}$. The gate capacitance of HJFET was modelled in [10]. In saturation, $C_{GD} \approx (1/2).W.(L_M - L_G).(C_{ox}||C_D) = 11$fF, and $C_{GS} \approx C_{GD} + (2/3).W.L_G.C_D = 38$fF, where $C_{ox} = \varepsilon_{ox}/t_{ox}$, $C_D = \varepsilon_{Si}/t_{Si}$, and ε_{ox} and ε_{Si} are the dielectric constants of oxide and Si, respectively.

III. AMPLIFIER CIRCUIT

The circuit diagram of the fabricated 4-stage HJFET amplifier is shown in Fig. 4. Each stage includes an amplifying HJFET, and a load HJFET having its gate tied to its source. The HJFETs have the same dimensions. The first stage with its input connected to ground serves as the noise source. The bias supply levels are increased from one stage to the next, such that all amplifying HJFETs are biased at $V_{GS} \approx 0.0$V, and $I_D \approx 50$nA. This biasing method eliminates the need for separate DC bias networks and DC-blocking capacitors between the stages. An amplifying stage is expected to have a maximum (i.e., intrinsic) low-frequency gain of $A_{V,i} \approx -g_m.r_{ds}/2 \approx -1\mu$A/V.100MΩ $= -100$, without

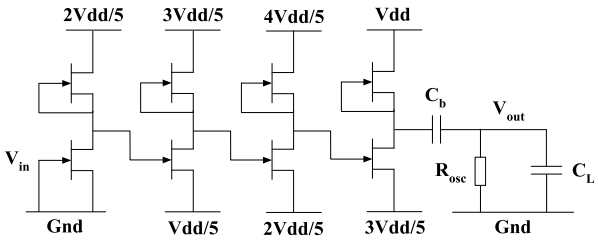

FIGURE 4. Schematic circuit diagram of the 4-stage HJFET amplifier.

a resistive output load, and a corresponding bandwidth of $f_{c,i} \approx 1/[2\pi(C_{out}.r_{ds}/2)]$, where $C_{out} \approx C_{GS} + C_{GD}.(1 - A_{V,i+1})$, and i refers to the stage number ($f_{c,i} \approx 1.4$KHz for $A_{V,i+1} = -100$), where the term $1 - A_{V,i+1}$ is due to Miller effect. The last stage is connected to an oscilloscope for measurement,with $A_{V,4} \approx -g_m.R_{osc} \approx -1$, and $f_{c,4} \approx 1/(2\pi C_L.R_{osc}) = 1.6$KHz, where $R_{osc} = 1$MΩ is the oscilloscope resistance, and $C_L \approx 100$pF represents the combined effect of oscilloscope capacitance (∼8pF), coaxial cables between oscilloscope and probe station, DC probes and other parasitics. The DC-blocking capacitor C_b suppresses output frequencies below $\sim 1/[2\pi C_b(R_{osc} + r_{ds}/2)] \approx 1/\pi C_b r_{ds}$.

IV. RESULTS AND DISCUSSION

The representative output signals of the HJFET amplifier biased at $V_{dd} = 1.25$V, without C_b (referred to as $C_b = 0$) and with $C_b = 250$pF are plotted in Figs. 5(a) and (b), respectively. These signals were acquired over different 3-second time spans and therefore uncorrelated from each other. The frequency spectrums of the signals are plotted in Fig. 5(c). The readout floor (i.e., readout with no input) of the digital oscilloscope is also plotted. When $C_b = 0$, the output signal has a DC level of ∼1V, but $C_b = 250$pF serves as a high-pass filter, setting the DC level to zero and suppressing the near-DC ($< \sim 10$Hz) frequencies. The histograms of the output voltages sampled every 10ms (using the digital oscilloscope) over a span of 12 seconds (therefore a total of 1200 samples) are given in Figs. 5(d) and (e), for $C_b = 0$ and 250pF, respectively (sample values are with respect to the DC level, which is non-zero for $C_b = 0$). Both histograms fit Gaussian distributions which are indicative of random phenomena.

The bit streams generated by replacing the positive samples with 1's, and the negative samples with 0's, are plotted for $C_b = 0$ and 250pF in Figs. 6(a) and (b), respectively. It is clear that the randomness of the bit stream generated with $C_b = 0$ is inferior to $C_b = 250$pF and some degree of predictability (e.g., of probable lengths of 1 and 0 chains, or distribution frequencies) is evident. This is further corroborated by the NIST SP-800-22 tests [12] listed in Table 1. (The criteria for passing a test is P-value ≥ 0.01). The bit stream generated from $C_b = 250$pF passes all the tests, but the bit stream generated from $C_b = 0$ fails the majority of the tests. The presence of low-frequency fluctuations (at frequencies below the sampling frequency), as

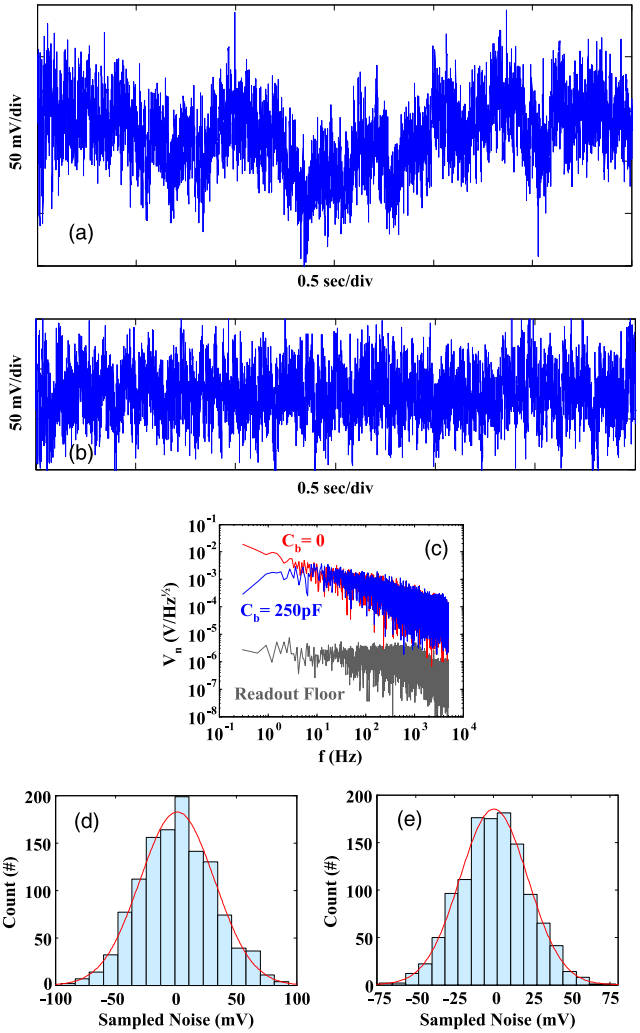

FIGURE 5. Typical measured outputs of the HJFET amplifier: output signals with (a) $C_b = 0$, and (b) $C_b = 250$pF; (c) frequency spectrum of the output signals with $C_b = 250$pF and $C_b = 0$, and the readout floor of the oscilloscope; and histograms of 1200 samples taken at a rate of 100Hz over 12 seconds from the output signals for (d) $C_b = 0$, and (e) $C_b = 250$pF.

is the case in the presence of flicker noise, is known to compromise the statistical randomness of the generated bit streams [13], [14]. To confirm this, frequencies below 10Hz were removed from the Fourier transform of the output signal generated with $C_b = 0$, and the bit stream was generated by sampling from the inverse Fourier transform of the result. The generated bit stream (Fig. 6(c)) indeed passes the NIST tests (Process A in Table 1). In addition, the techniques used for generation of pseudorandom numbers [15], [16] can be used for improving the statistical randomness of the bit stream. For example, the chaotic function $y[i]=x[1+round(1199.t[i+1])]$, $t[i+1]=4.t[i].(1-t[i])$, with $t[1]=0.3$ as the initial condition (x and y are the input and output bit streams, respectively; $1 \leq i \leq 1200$ is an integer, and the *round* function returns the least integer greater than or equal to its input), when applied to the bit stream of Fig. 6(a) results in the bit stream of Fig. 6(d), which

TABLE 1. Results of NIST SP-800-22 tests on generated bit streams.

Test	Bit Size	Block Size	Calculated P-Values			
			$C_b = 0$	$C_b = 250$ pF	$C_b = 0$, Process A	$C_b = 0$, Process B
Frequency (Monobit) Test	N = 1200	–	P = 0.106	P = 0.488	P = 0.729	P = 0.204
Frequency Test within a Block	N = 1200	M = 120	P = 0.000	P = 0.875	P = 0.919	P = 0.626
Runs Test	N = 1200	–	P = 0.000	P = 0.696	P = 0.523	P = 0.636
Longest Run of Ones within a Block	N = 1200	M = 8	P = 0.678	P = 0.783	P = 0.470	P = 0.516
Discrete Fourier Transform Test	N = 1200	–	P = 1.000	P = 0.427	P = 0.596	P = 0.112
Serial Test	N = 1200	M = 5	P1 = 0.000 P2 = 0.000	P1 = 0.549 P2 = 0.785	P1 = 0.018 P2 = 0.408	P1 = 0.591 P2 = 0.841
Approximate Entropy Test	N = 1200	M = 4	P = 0.000	P = 0.864	P = 0.494	P = 0.912
Cumulative Sums (Cusum) Test	N = 1200	–	P = 0.003	P = 0.881	P = 1.000	P = 1.000

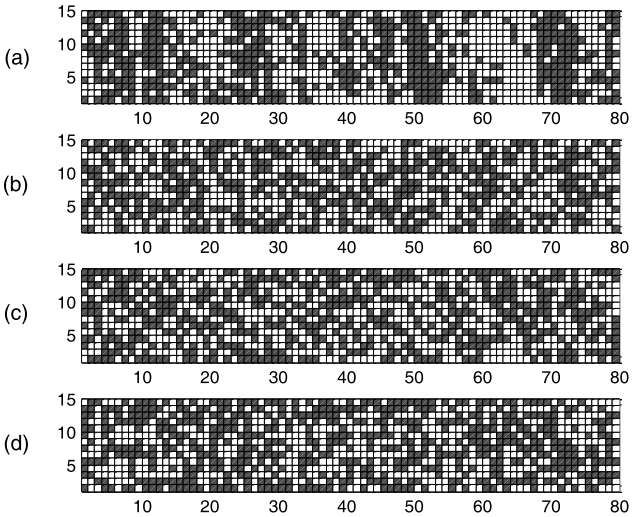

FIGURE 6. Bit streams generated by (a) sampling the output signal with $C_b = 0$ and no processing, (b) sampling the output signal with $C_b = 250$pF and no processing, (c) removing frequency components below 10Hz from the output signal for $C_b = 0$ (Process A) followed by sampling; and (d) applying a chaotic function to the bit stream "(a)" described above (Process B). The sequence representation is column-wise (from bottom to top), and the gray and white pixels represent 0's and 1's, respectively.

passes the NIST tests (Process B in Table 1). Since the input bit stream to the chaotic function is non-deterministic, the output bit stream is also non-deterministic. While it is straightforward to implement such processing techniques with a general-purpose processer, it is unlikely, if practical at all, that they can be implemented with TFTs. In contrast, choosing an appropriate C_b eliminates the need for such processing. For the reported measurements, a discrete capacitor was connected in series between the oscilloscope and the amplifier output, but monolithic implementation of C_b for example as a metal-insulator-metal capacitor is straightforward.

For the bias conditions discussed in Section III, each amplifier stage has a bias current of ∼50nA and a bias voltage of ∼0.5V, thus resulting in a power consumption of ∼25nW per stage. At f = 1Hz, the input-referred noise voltage of $\sim 2\mu V/Hz^{1/2}$ (Fig. 3(d)) is amplified to an output noise voltage of $\sim 10mV/Hz^{1/2}$(Fig. 5(c)), corresponding to a low-frequency amplifier gain of ∼5000, and therefore an average gain of ∼17 for each of the first three amplifier stages (the last stage has a gain of ∼1, due to loading from R_{osc}). This average gain per stage is lower than the predicted maximum of ∼100 derived in Section III. This is due to non-idealities such as device size mismatch and inaccuracy of bias levels created from a monolithic resistive voltage divider (both resulting in some HJFETs having $V_{DS} < 0.25$V and therefore $r_{ds} < 200M\Omega$), as well as unintended leakage paths through the non-optimized interlayer dielectrics and metallization layers, which reduce the effective r_{ds}. The amplifier gain and therefore power consumption are expected to improve with the optimization of the integration process. Given the high stability of the HJFETs [10], [11], the amplifier gain is expected to be sufficiently stable over time. We believe integration of additional circuitry (such as a comparator, or sample and hold) for a monolithic random number generator is also feasible with HJFETs.

While discussed with respect to HJFETs, the described technique is not specific to these devices. However, given that conventional TFTs typically have intrinsic gains smaller than 40 and require power consumptions above 10μW to achieve such intrinsic gains [17]–[23], efficient implementation with conventional TFTs, without any device modification, is unlikely. It has been reported that oxide TFTs with Schottky-barrier source/drain contacts can achieve a very high output resistance, and intrinsic gains exceeding 400 at very low bias currents [24]. This suggests that, with proper device engineering, efficient implementation with other TFT technologies may also be feasible. Other TFT requirements, such as stability, also need to be taken into account.

V. SUMMARY AND CONCLUSION

A low-power noise amplifier was implemented with thin-film Si HJFETs and its suitability for generation of true random numbers was investigated. It was found that the noise output of a proof-of-concept 4-stage amplifier with a voltage gain of ∼5000, bandwidth of ∼1 KHz, operation power of ∼100nW, and a DC-blocking output capacitance of 250pF is suitable for generation of statistically true random numbers at a rate of 100 bit/sec without requiring post-processing. The HJFETs are biased at near subthreshold to obtain a large output resistance and therefore a high intrinsic

gain at a low operation power. The large output resistance also allows the use of a sufficiently small DC-blocking capacitor at the amplifier output. The DC-blocking capacitor eliminates the low-frequency signal fluctuations that would otherwise compromise the statistical randomness of the generated bit stream. Higher amplifier gains and therefore lower power consumptions are expected with optimization of the integration process.

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