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Investigation of a Hybrid Approach for Normally-Off GaN HEMTs Using Fluorine Treatment and Recess Etch Techniques

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ABSTRACT A hybrid approach for obtaining normally off high electron mobility transistors (HEMTs) combining fluorine treatment, recess etch techniques, and AlGaN buffer was studied. The effects of process variations (recess etch depth and fluorine treatment duration) and epitaxial differences (AlGaN and carbon doped GaN buffers) on the DC characteristics of the normally off HEMTs were investigated. Two different epitaxial structures and three different process variations were compared. Epitaxial structures prepared with an AlGaN buffer showed a higher threshold voltage ($V_{\mathrm{th}} = +3.59$ V) than those prepared with a GaN buffer ($V_{\mathrm{th}} = +1.85$ V).

INDEX TERMS AlGaN, GaN, enhancement-mode, fluorine plasma implantation, recess etch, HEMT, normally-off.

I. INTRODUCTION

AlGaN/GaN HEMT devices have become the most widely used devices for high power applications in areas such as defense, space, and telecommunications applications. Since these transistors have a wide band gap, high breakdown field, and high saturation velocity [1], [2], they are almost fully capable of meeting the demands of applications that require high power and high-frequency operations. Several methods have been used to improve the HEMT performance [3]–[5]. Conventional normally-on HEMTs with negative threshold voltages are not suitable for power switching applications because they do not have a fail-safe operation [6] and have high circuit design complexity. Normally-off HEMTs are preferred to prevent fault-turn-on issues and achieve high threshold voltages (V_{th}) for high power switching devices. Many techniques such as gate recess [7], fluorine treatment [8], gate-controlled tunnel junctions [9], and p-type gates [10] have been demonstrated to achieve normally-off operation. Although reliable normally-off operation can be achieved with such methods, gate leakage currents are often increased. Suppression of the gate leakage current is obtained by the conversion of the Schottky gate to a metal-insulator-semiconductor stack, by inserting a dielectric material between the gate metal and barrier layer [11]. Modification of the gate threshold voltage can be performed using ‘gate-recess’ etching, which is etching the barrier layer under the gate metal electrode. Reduction of the AlGaN thickness results in a reduced polarization-induced 2DEG density, which leads to a positive shift in V_{th} [12], [13]. A positive threshold voltage can also be achieved by F^- treatment by means of plasma treatment. Due to the negative charges and strong electronegativity of fluorine ions, the potential of the AlGaN barrier rises, which provides a positive V_{th} [14]. Gate recess and fluorine treatment have been demonstrated in combination to further increase the threshold voltage [15]–[17]. An approach used in conjunction with the abovementioned techniques to obtain normally-off HEMTs is the inclusion of an AlGaN

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Samples A, B, C, D	Sample E
GaN cap	GaN cap
$Al_{0.26}Ga_{0.84}N$ Barrier	$Al_{0.26}Ga_{0.84}N$ Barrier
AlN	AlN
u-GaN	u-GaN
$Al_{0.05}Ga_{0.95}N$ Buffer	GaN:C Buffer
Buffer	Buffer
Nucleation Layer	Nucleation Layer
Si (111)	Si (111)

FIGURE 1. Epitaxial structure illustration of Samples A, B, C, D (left) and, E (right).

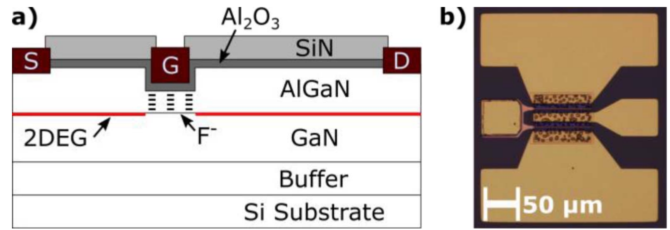

FIGURE 2. a) Schematic cross section and b) micrograph of the fabricated E-mode HEMT.

back-barrier, which has widely been reported to further increase the threshold voltage, in addition to other advantages such as suppressed leakages and improved breakdown voltage [18]–[20].

In this paper, we present the results of an investigative study of the DC characteristics of a normally-off GaN HEMT obtained using a hybrid approach of fluorine treatment, recess etch techniques, and AlGaN buffer. The dependence of the threshold voltages and $I_{d,max}$ values on the gate recess and fluorine treatment process differences were investigated, and compared to characteristics achievable with a GaN:C buffer. A relatively high threshold voltage of +3.59 V is demonstrated for the device obtained with the hybrid approach.

II. DEVICE STRUCTURE AND FABRICATION

Two epitaxial HEMT structures were grown on 100 mm (111) silicon wafers with a resistivity higher than 10 kΩ·cm (Fig. 1). In Samples A, B, C (Group 1), and D (Group 2), the HEMT structure consists of a 300 nm AlN nucleation and AlGaN strain managing layer stack followed by 1150 nm of a low Al content $Al_xGa_{1-x}N$ (x: 0.05) buffer and 110 nm of a high mobility channel GaN. To complete the active layers of the HEMT structure, we grew a 1 nm AlN spacer prior to the 27 nm AlGaN barrier; finally, epitaxial growth was finished with a 3 nm unintentionally doped GaN capping layer. In Sample E (Group 2), the AlGaN buffer was replaced with a 1200 nm carbon doped highly resistive GaN buffer. The rest of the layers and growth conditions were kept the same as those of Group 1. In Table 1, the labeled samples are listed in detail. A two dimensional electron gas (2DEG) density of 6.7×10^{12} cm^{-2} and electron mobility of 1425 cm^2/V·s were measured for Samples A, B, C, and D using the Hall technique. Sample E was found to have an electron mobility of 1313 cm^2/V·s and 2DEG density of 2.0×10^{13} cm^{-2}.

Group 1 of our experiment includes Sample A, Sample B, and Sample C, in which we have compared the results of the recess etch and fluorine treatment variations. Group 2 of our experiment includes Sample D and Sample E, in which we have investigated the impact of the tradeoffs of AlGaN back-barrier compared to the standard GaN buffer.

Device fabrication for both experimental groups began with mesa device isolation performed in the Sentech ICP-RIE dry etching system using a BCl_3 and Cl_2 gas mixture. Ohmic contacts were formed by a Ti/Al/Ni/Au (12/120/35/65 nm) metal stack deposited by electron-beam evaporation. This process was then followed by a 3-step rapid thermal annealing (RTA) process specifically optimized for our HEMTs. The annealing process was carried out in N_2 ambient at 400 °C for 180 s, 700 °C for 40 s, and 830 °C for 30 s (R_c = 0.67 Ω.mm and R_{sh} = 488 Ω/□). The gate regions were defined with optical lithography. Gate recess etching was performed with the Sentech ICP-RIE system using BCl_3/Cl_2 gas chemistry. In Group 1, the gate recess etch depths for the three samples were set at 10 nm, 15 nm, and 15 nm respectively. In Group 2, the recess etch depth of the both samples was set to 10 nm. Immediately after the recess etching a low power F^- treatment was carried out for 10 minutes, 10 minutes and 15 minutes, respectively, for the samples used in Group 1. For Group 2, F^- treatment time was 10 minutes. F^- treatment was carried out with the Samco 140 ip ICP-RIE with SF_6 gas, RF power of 10 W, and no ICP power. A longer low power treatment was preferred in place of conventional shorter and higher power processes in order to minimize surface damage. A 10 nm thick Al_2O_3 dielectric layer was deposited under the gate region on each sample for both experimental groups. The Al_2O_3 dielectric deposition was performed using an Cambridge Nanotech Savannah S100 ALD System. The Al_2O_3 depositions were carried out at 200 °C. Optical lithography was used to redefine the gate regions for the metallization step in order to create the gate electrodes. The gate electrodes were made of Ni/Au (50/300 nm) using e-beam evaporation. A 240 nm SiN_x passivation layer was deposited with Sentech plasma enhanced chemical vapor deposition (PECVD). Subsequently, the contact pad openings were defined with optical lithography and etched using a dry etching process. Interconnect patterns were formed with optical lithography. Finally, a relatively thick Ti/Au interconnect metal stack (200/2000 nm) was deposited by e-beam evaporation. The devices have a source-drain spacing of L_{DS} = 9 µm, source-gate spacing of L_{GS} = 2 µm, two gate fingers with gate length of L_G = 2 µm, and a gate finger width of 100 µm. The schematic cross section and micrograph of a fabricated E-mode HEMT are shown in Fig. 2.

TABLE 1. Summary of epitaxial and process properties, and average measurement results.

Parameter (Mean ± SD)	Group 1			Group 2	
	A	B	C	D	E
n_s (cm^{-2})	6.7×10^{12}	6.7×10^{12}	6.7×10^{12}	6.7×10^{12}	2.0×10^{13}
F^- treatment (min.)	10	10	15	10	10
Recess Etch (nm)	10	15	15	10	10
V_{th} (V)	2.85 ± 0.27	2.60 ± 0.21	3.59 ± 0.12	2.85 ± 0.27	1.85 ± 0.25
$I_{d,max}$ (mA/mm)	421 ± 24	500 ± 6.5	396 ± 16	421 ± 24	741 ± 23
$I_{g,\,leakage}$ (μA/mm)	6.6 ± 2.5	6.7 ± 3.8	11 ± 2.2	6.6 ± 2.5	19 ± 5.3
$I_{d,\,leakage}$ (μA/mm)	0.30 ± 0.26	51 ± 9.5	0.0099 ± 0.0062	0.30 ± 0.26	660 ± 1250
V_{br} (V)	63 ± 1.4	52 ± 1.4	73 ± 1.4	63 ± 1.4	23 ± 1.7
R_{on} (Ohm.mm)	102	84	107	102	73
V_{knee} (V)	5.5	5.2	5.5	5.5	6.6
g_m (mS/mm)	148	150	146	148	190
Buffer	AlGaN	AlGaN	AlGaN	AlGaN	GaN:C

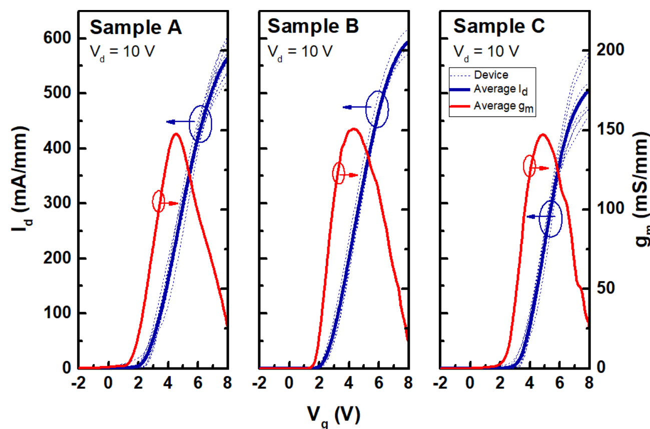

FIGURE 3. Transfer characteristics of Sample A (left), Sample B (middle), and Sample C (right) on the AlGaN buffer wafer.

III. RESULTS AND DISCUSSION

Device characterization was carried out using a Keithley 2612A SourceMeter instrument. Multiple devices were measured from each sample (4-10 devices). In Table 1, the summarized average measurement results and process details of both groups are given; the average and standard deviation are given for the measured results (V_{th}, $I_{d,max}$, $I_{g,leak}$, $I_{d,leak}$, and V_{br}) and the average is given for the calculated results (R_{on}, V_{knee}, and g_m). Fig. 3 and Fig. 4 show the typical transfer characteristics of the measured devices at a drain bias of $V_d = 10$ V. The threshold voltages were extracted using the linear extrapolation method, that is, the gate bias intercept of the linear extrapolation at maximum transconductance has been extracted. The threshold voltages were obtained as +2.85 V for Sample A, +2.60 V for Sample B, +3.59 V for Sample C, +2.85 V for Sample D,

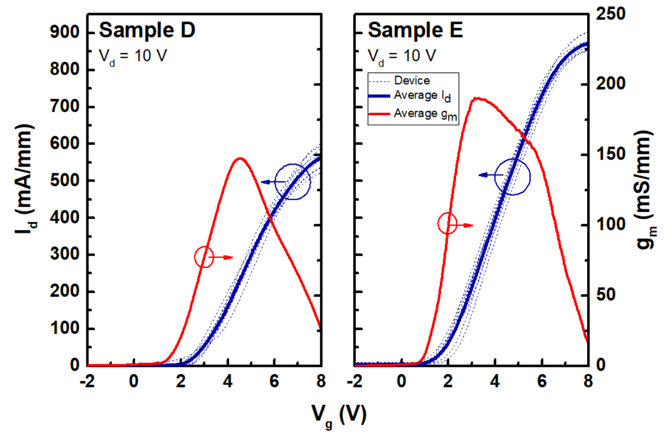

FIGURE 4. Transfer characteristics of Sample D (left) on AlGaN buffer wafer and Sample E (right) on the GaN:C buffer wafer.

and +1.85 V for Sample E. In Group 1, comparing Sample A and Sample B, an increase in threshold voltage is expected due to the decreased sheet carrier density caused by the thinned barrier layer and increased concentration of fluorine ions close to the channel. However, we observe that when the recess depth is increased, a decrease in the threshold voltage by about 0.25 V is observed (Sample A to Sample B), which is attributed to the increasing trap concentration at the Al_2O_3/AlGaN interface due to increased surface damage, which can become positively charged during DC-V_g measurements and lead to a negative shift in V_{th} [21]. It is clearly observed that if we increase the F^- treatment time (Sample B to Sample C) while maintaining the same gate recess etch depth, this degradation is compensated for by the passivation of the traps from increased fluorine ion concentration [21], and the threshold voltage shifts to a more positive value, increasing by nearly 0.9 V. Comparing the samples of Group 2, Sample D exhibits a greater threshold voltage by 1 V. The higher threshold voltage of Sample D is attributed to the AlGaN buffer. The AlGaN buffer acts to raise the conduction band above the Fermi level, leading to a lower sheet carrier density and a higher threshold voltage [22].

Typically, it is known that the gate recess increases the transconductance, as a decrease in the barrier layer thickness causes an increase in the transconductance [23]. Comparing Sample A and Sample B, it is observed that a 5 nm increase of recess depth only leads to a small increase in g_m. Sample C has a decreased transconductance compared to both groups, which indicates that the etching damage from the fluorine plasma treatment affects the electron mobility in the channel. In Group 2, Sample E demonstrates a higher peak transconductance value than Sample D; this increase is also directly related to the higher sheet carrier density of Sample E.

The drain leakage currents were extracted from the transfer characteristic measurements as the drain current density at the gate bias of $V_g = -6$ V. The samples of Group 1

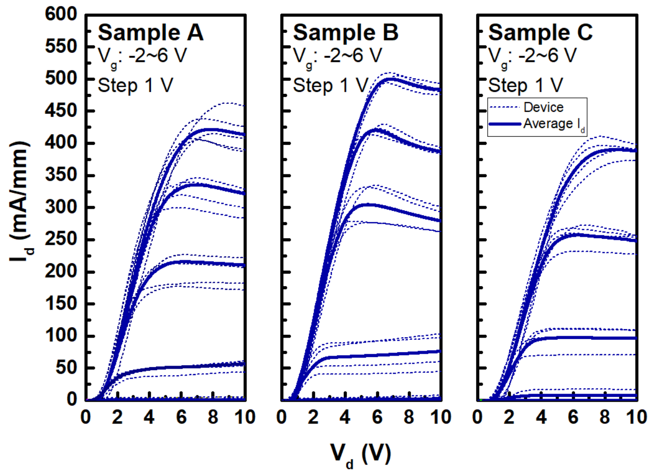

FIGURE 5. Output characteristics of Sample A (left), Sample B (middle), and Sample C (right) on the AlGaN buffer wafer.

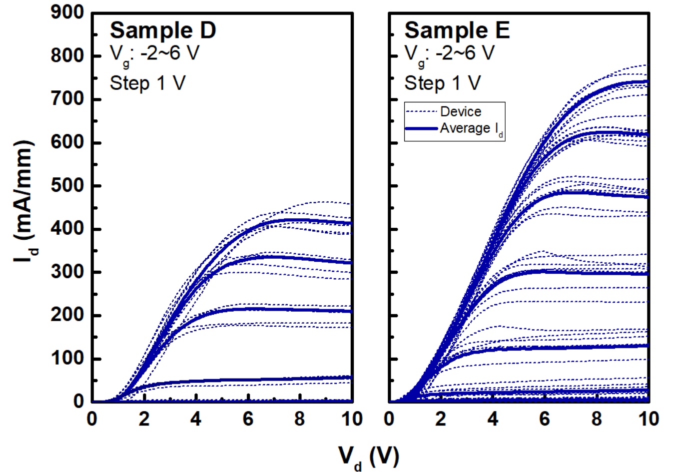

FIGURE 6. Output characteristics of Sample D (left) on AlGaN buffer wafer and Sample E (right) on the GaN:C buffer wafer.

displayed drain leakage magnitudes correlated with the drain current densities. In Group 2, an order of magnitude improvement is seen in the drain leakage characteristic of Sample D compared to Sample E.

The output characteristics are shown in Figure 5 (Group 1) and Figure 6 (Group 2). In Group 1, Sample B demonstrate higher maximum drain current densities than Sample A. It is supposed that the increase in current density in Sample B is related to the lower threshold voltage, indicating that a 5 nm increase in gate recess does not deplete the 2DEG region in a sufficient amount to decrease drain current. Comparing Sample C to Sample B, with the increase of fluorine treatment time, an over 100 mA/mm drop in drain current is observed. This decrease is related to mobility degradation caused by border traps and interface traps generated by an increasing concentration of F^- ions in the channel region [21]. For the three samples in Group 1, similar knee voltages are obtained. In Group 2, Sample E exhibits a higher maximum current density (741 mA/mm at $V_{GS} = 6$ V) than Sample D (421 mA/mm at $V_{GS} = 6$ V), corresponding to a higher drain current of a factor of 1.5, due to the higher sheet carrier density. Sample E also exhibits a 1.1 V higher knee voltage and lower static on-resistance. For both groups, R_{on} values directly correlate with the threshold vales.

The Schottky gate reverse leakage characteristics are shown in Fig. 7. The gate leakage currents were extracted at the gate bias of $V_g = -1$ V. The increase recess depth does not lead to a significant change in gate leakage current. A slight increase is observed in the leakage characteristics with longer fluorine treatment duration. The use of an AlGaN buffer leads to the suppression of the gate leakage current by one order of magnitude compared to a GaN:C buffer.

Off-state breakdown measurements were obtained at gate bias of $V_g = -6$ V (Fig. 8). The breakdown voltage was defined as the drain bias at the drain leakage current of 1mA/mm. For Group 1, Samples A and B display similar breakdown voltages. Sample C displays a slightly higher

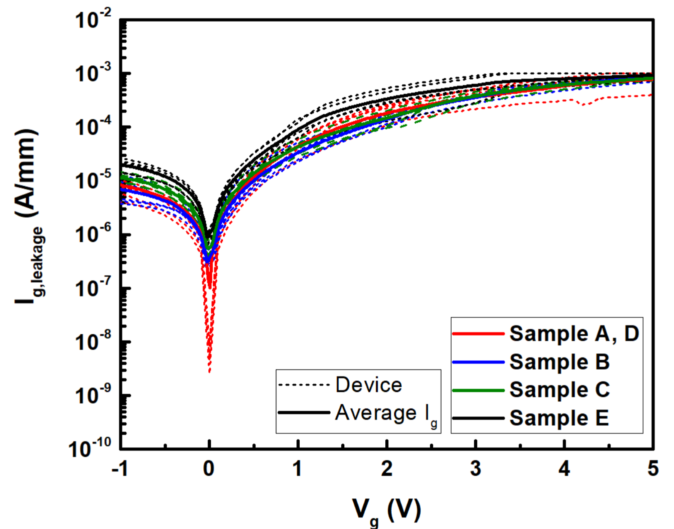

FIGURE 7. Gate leakage characteristics for both experimental groups.

breakdown voltage, owing to the increased energy barrier of the buffer layer under the channel from increased fluorine ion concentration [24]. In Group 2, owing to the reduced sheet carrier density and improved electron confinement resulting from the AlGaN back-barrier, Sample D demonstrates more than double the breakdown voltage of Sample E.

In order to gain insight on the RF characteristics of the fabricated normally-off devices gate lag measurements were carried out for the samples of Group 2 (Fig. 9). The measurements were carried out using an Agilent E3631A power supply, Keysight Technologies 33500B waveform generator, and a Keysight InfiniVision DSOX2004A oscilloscope. The devices were pulsed from Vg of −2 V to 4 V, with a pulse width of 1 μs and period of 20 μs, corresponding to a duty cycle of 5%. Sample D exhibits gate lag of 40%, whereas Sample E exhibits gate lag of 8.8%. We conjecture that the relatively low gate lag of Sample E compared to Sample D

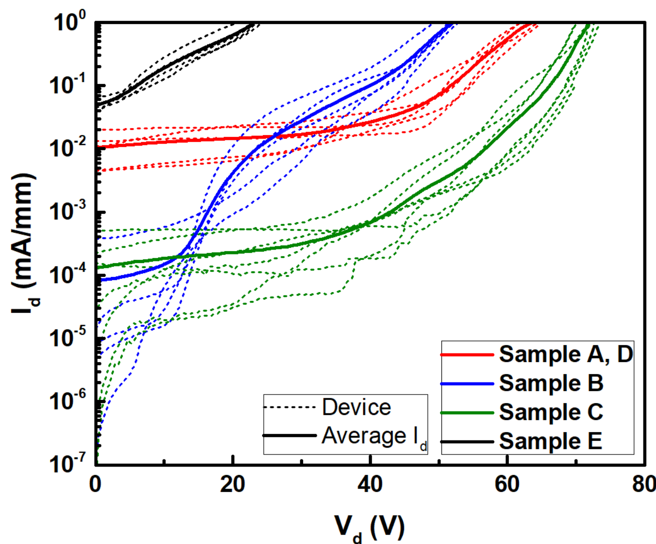

FIGURE 8. Off-state breakdown characteristics for both experimental groups.

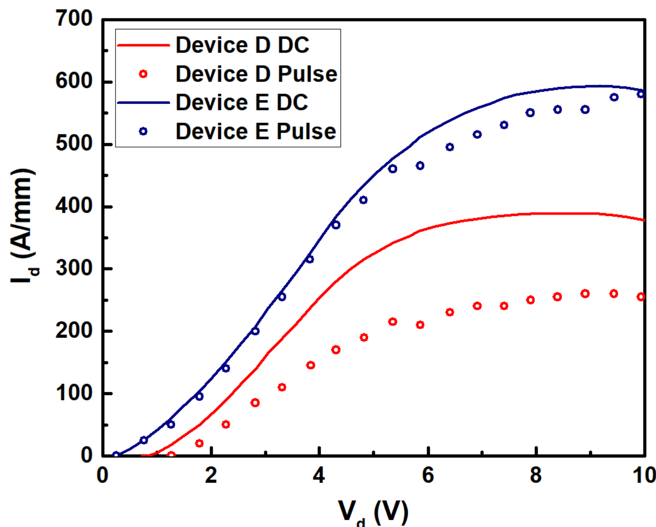

FIGURE 9. Gate lag characteristics for Group 2. In pulsed measurement V_g switches from −2 V to 4 V, with frequency of 50 kHz and duty cycle of 5%.

indicates that the gate lag characteristic is more sensitive to the traps in the AlGaN buffer than surface traps generated by fluorine treatment and recess etch.

IV. CONCLUSION

A study of the DC characteristics of normally-off obtained using a hybrid approach utilizing gate recess, fluorine treatment techniques, and AlGaN buffer was carried out. The fabricated AlGaN buffer normally-off devices were compared to a GaN:C normally-off device in order to assess the impact of the advantages of the AlGaN buffer. Variations of the recess etch depth and fluorine treatment duration are shown to have notable impacts on the threshold voltage, maximum drain current density, and breakdown voltage, whereas the gate and drain leakage currents, knee voltage, and transconductance characteristics are maintained or exhibit minimal variations. In terms of percentage increase or decrease in the V_{th}, $I_{d,max}$, and V_{br} characteristics for the process variations studied, it is observed that the increase in fluorine treatment time has a greater effect than the increase of the gate recess depth. It is observed that for variations in recess etch depth, the characteristics that shows the most sensitivity are $I_{d,max}$, and V_{br}, whereas for variations in fluorine treatment time V_{th} and V_{br} show the most sensitivity. Since the maximum achievable drain current density decreases as the threshold voltage increases, to achieve the optimum tradeoff the fluorine treatment parameters should be optimized. Of the DC characteristics of the AlGaN and GaN:C buffer devices breakdown voltage, maximum drain current density, transconductance, and threshold voltage demonstrate consequential variations, with the breakdown voltage and drain current density varying by over 50%. It is seen that the decrease in threshold voltage for the GaN:C buffer compared to the AlGaN buffer is on the order of those observed for process variations, indicating that the AlGaN buffer is not the most significant factor in achieving normally-off operation in the studied hybrid approach.

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