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Monitoring of FinFET Characteristics Using $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ and $\Delta V_{DIBL}/(I_{on}/I_{off})$

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ABSTRACT In this paper, we present a descriptive analysis of a performance index, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, used for performance monitoring. Scaled n- and p-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) (planar and FinFET devices) are included for comparison of performance trends. Also, the simplified $\Delta V_{DIBL}/(I_{on}/I_{off})$ for monitoring the electrical characteristics of MOSFET devices is proposed due to the "quick measurements" required in the last step of the semiconductor manufacturing process. $\Delta V_{DIBL}/(I_{on}/I_{off})$ only accounts for drain-induced barrier lowering in its numerator and on/off current ratio in its denominator. The calculation process for $\Delta V_{DIBL}/(I_{on}/I_{off})$ is much quicker than for $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, where we need to make an extra measurement of the value of the subthreshold swing. Performance metrics, such as I_{on}/I_{off} and intrinsic gain, $g_m \times r_o$, are reported using $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ and $\Delta V_{DIBL}/(I_{on}/I_{off})$. ΔV_{DIBLSS} of about 100 mV in scaled MOSFETs is required to ensure that the gate control is strong. Since I_{on}/I_{off} is a sensitive function of threshold voltage, the estimates of the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ and $\Delta V_{DIBL}/(I_{on}/I_{off})$ are therefore dependent on the design of threshold voltage. In planar MOSFETs, small values of $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ and $\Delta V_{DIBL}/(I_{on}/I_{off})$ are hard to achieve. However, in FinFETs, it is easy to achieve the performance requirements due to its tri-gate structure.

INDEX TERMS $\Delta V_{DIBL}/(I_{on}/I_{off})$, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, FinFETs, intrinsic gain, performance metrics, scaled MOSFETs.

I. INTRODUCTION

The expression, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, was introduced to evaluate the performance of scaled metal–oxide–semiconductor field–effect transistors (MOSFETs) [1], [2]. Four key parameters extracted from MOSFET subthreshold characteristics are combined into a single parameter reflecting the performance. ΔV_{DIBL} is calculated as the difference between linear threshold voltage, $V_{t,lin}$, and saturation threshold voltage, $V_{t,sat}$. ΔV_{SS} is defined to be approximately the value of the subthreshold swing (SS). ΔV_{DIBLSS} is the sum of ΔV_{DIBL} and ΔV_{SS}. It is interesting to note that the value of the I_{on}/I_{off}, which reflects the "quality" of a transistor, is affected by the value of the ΔV_{DIBLSS}. I_{on} is the drain on–state current and I_{off} is the drain off–state current. As the gate length is reduced, the value of the ΔV_{DIBLSS} needs to be as small as 100 mV. The reason for this requirement is to maintain gate control over the channel potential barrier height [2]–[4]. As a result, the value of the I_{on}/I_{off} should be 10^6. Hence a $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ of about 10^{-4} mV is obtained. These results are described in [2]. If a highly scaled transistor cannot meet the requirements mentioned above, we may say that the poor short–channel performance is expected and acts as a bottleneck for further scaling [5], [6].

We carefully studied the fundamental concepts of $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ in more detail. As discussed earlier, for example, we showed that the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ value should be about (or below) 10^{-4} mV. The FinFET with this requirement is to have a strong control over short–channel effects (SCEs). Note, however, that the focus was on investigating the standard–V_t (SVT) devices. Thus, a descriptive analysis of the figure of merit (FoM), $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, is limited to SVT devices and excludes low–V_t (LVT)

devices. As for the value of the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ in planar MOSFETs and the relationships between the n–channel devices and the p–channel devices in terms of $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, these issues will be discussed in the Results and Discussion section.

In this work, our main goal is to extend the scope of the research findings for both SVT and LVT. The p–channel devices are included for comparison. Additionally, the analog performance metrics such as transconductance, g_m, and output resistance, r_o, are also included. FoM1, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, is used not only for FinFETs, but also for planar MOSFETs. In order to perform a high–throughput measurement required in the last step of the semiconductor manufacturing process, the measurement of ΔV_{SS} can be omitted. FoM2, $\Delta V_{DIBL}/(I_{on}/I_{off})$, provides us a good alternative to FoM1 for this purpose.

II. EXPERIMENT

The fabrication process for FinFET_1 is almost the same as for the FinFETs presented in [2]. For example, fin widths were between 8.2 nm and 9.1 nm, and fin heights were between 40.1 nm and 42.3 nm [2]. Both the thickness uniformity of film stacks and the critical dimension uniformity of patterned photoresist lines are enhanced and controlled because we further optimized the process conditions (for FinFETs) in this work to achieve better performance. Additionally, we present another device called FinFET_2 with lower power supply voltage (V_{dd} = 0.5 V) implemented. The difference between FinFET_1 and FinFET_2 is that FinFET_1 is classified as an SVT device, and FinFET_2 is classified as an LVT device. (Two transistor families are achieved by using metal gate technology.) The planar MOSFETs were fabricated (including for this study). The p–channel devices were also included. It is very hard to make an apple–to–apple comparison of their electrical characteristics, but the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ value has an important role in reflecting the device performance measured by the wafer acceptance testing (WAT). For planar bulk, gate lengths were between 22 nm and 28 nm. For FinFETs, gate lengths were between 16 nm and 20 nm.

The major processes of planar MOSFETs are described. We used bulk silicon (Si) wafers for manufacturing of planar MOSFETs. P–well (B: 1.75×10^{19} cm^{-3} to 3.5×10^{19} cm^{-3}) and n–well (P: 1.5×10^{19} cm^{-3} to 3×10^{19} cm^{-3}) were performed after shallow trench isolation (STI) formation. The gate definition was then carried out. Next, the selective epitaxial growth of silicon–germanium (SiGe) was formed. For n–channel devices, the SiGe structure was absent. Rapid thermal processing (RTP) was applied to activate the implanted source/drain (S/D) dopants (As for n–channel and B for p–channel: 1×10^{21} cm^{-3} to 2×10^{21} cm^{-3}) in Si. Standard replacement metal gate technology took place in subsequent processes. The hafnium oxide (HfO_2) gate dielectric thicknesses (17.9 Å to 19.9 Å) were measured, which is similar to [2].

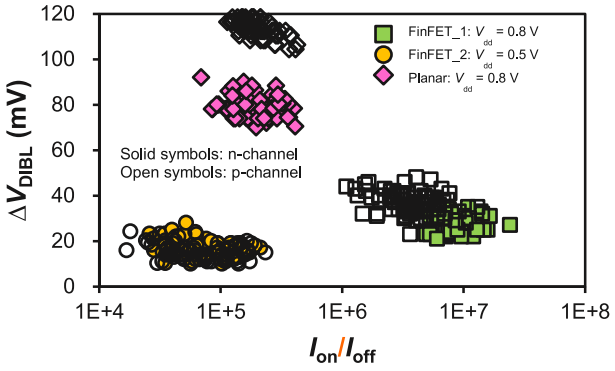
This work focuses on analyzing parameters of scaled MOSFETs, such as drain–induced barrier lowering (DIBL), SS, $V_{t,sat}$, I_{on}, and I_{off}. The transistor's FoMs mentioned above are the five must–have items in the last step of the semiconductor manufacturing process that provides us with the information about the device characteristics. Note that we use the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ value as the key parameter, reflecting the short–channel performance of the devices. We also measured the analog FoMs such as g_m, r_o, and intrinsic gain, $g_m \times r_o$ (in the performance measurement process), in the same devices. In other words, the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ value is used for monitoring not only the logic FoMs, but also the analog FoMs. Furthermore, $\Delta V_{DIBL}/(I_{on}/I_{off})$ is used as a quick feedback of device performance with reduced measuring time. Since it is impossible to make detailed measurements in mass production, the use of $\Delta V_{DIBL}/(I_{on}/I_{off})$ will become highly desirable for minimizing the gap between WAT and wafer packaging. Therefore, the $\Delta V_{DIBL}/(I_{on}/I_{off})$ value becomes even more important in reflecting the short–channel performance of highly scaled MOSFETs within limited measuring time.

III. RESULTS AND DISCUSSION

Fig. 1(a) shows the plot of ΔV_{DIBL} versus log I_{on}/I_{off}. Our goals are: (1) to minimize the value of the ΔV_{DIBL} and (2) to maximize the value of the I_{on}/I_{off}. It is shown that I_{on}/I_{off} is almost independent of ΔV_{DIBL} for FinFETs. Due to the DIBL suppression, the gate of the FinFETs still has more control than the drain over the body of the transistor. It can also be shown that the planar MOSFETs may have reached its limit since its ΔV_{DIBL} value is much higher than that of the FinFETs. As the ΔV_{DIBL} decreases, the I_{on}/I_{off} increases (for planar bulk). We may say that a small ΔV_{DIBL} results in low subthreshold leakage current, thus increasing the I_{on}/I_{off} value [2], [7]. For planar bulk, the value of the ΔV_{DIBL} affects the value of the I_{on}/I_{off}.

The measured ΔV_{SS} versus log I_{on}/I_{off} is plotted in Fig. 1(b). As the SS decreases, the I_{on}/I_{off} of the transistor may be increased [8], [9]. However, due to better control of the gate over the channel of the FinFETs, the I_{on}/I_{off} value is not as strongly affected by decreasing ΔV_{SS}. As discussed earlier (Fig. 1(a)), the value of the ΔV_{DIBL} affects the value of the I_{on}/I_{off} for planar bulk. It is interesting to note that the ΔV_{SS} has a similar effect on the I_{on}/I_{off} as the ΔV_{DIBL}. Since the ΔV_{DIBLSS} shown in Fig. 1(c) is the sum of ΔV_{DIBL} and ΔV_{SS}, the ΔV_{DIBLSS} may have a similar effect on the I_{on}/I_{off} as the ΔV_{DIBL} (and the ΔV_{SS}). Planar bulk's p–channel devices show that the SCEs are quite large. For p–FinFET devices, the multi–gate structure helps to gain adequate control of SCEs. As a result, small DIBL and steep SS may be obtained (for p–FinFET devices). These results are visible in Figs. 1(a), 1(b), and 1(c).

Fig. 2 shows the plot of $V_{t,sat}$ versus log I_{on}/I_{off}. We observe that the value of the I_{on}/I_{off} is strongly affected by the value of the $V_{t,sat}$. FinFET_1, classified as an SVT device, has the advantage of providing a large I_{on}/I_{off}. This



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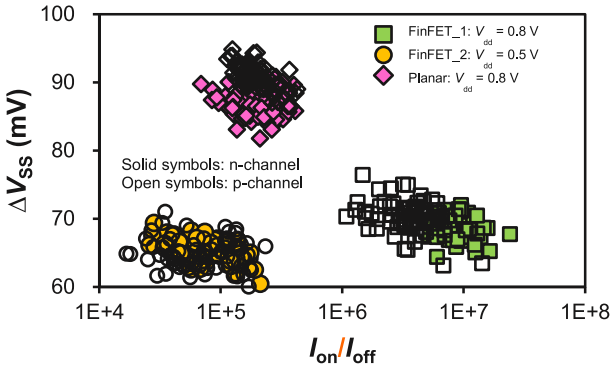

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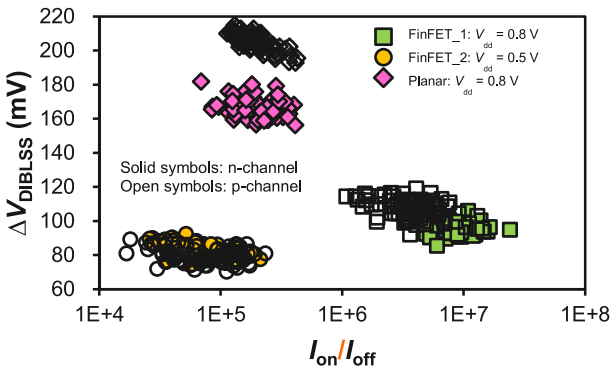


(c)

FIGURE 1. **(a) ΔV_{DIBL} versus log I_{on}/I_{off}. (b) ΔV_{SS} versus log I_{on}/I_{off}. (c) ΔV_{DIBLSS} versus log I_{on}/I_{off}. FinFETs have the ability to gain adequate control of SCEs. Thus, in FinFETs, I_{on}/I_{off} is almost independent of ΔV_{DIBL} (and ΔV_{SS}).**

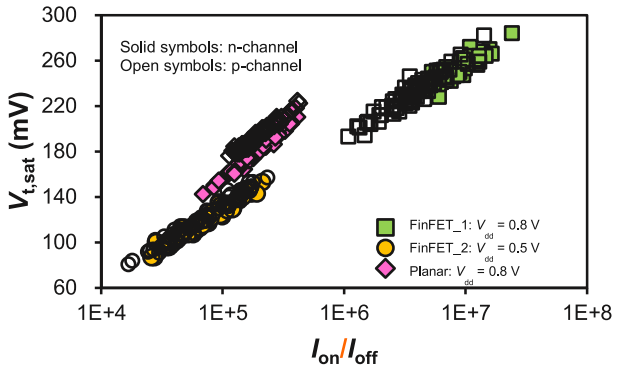
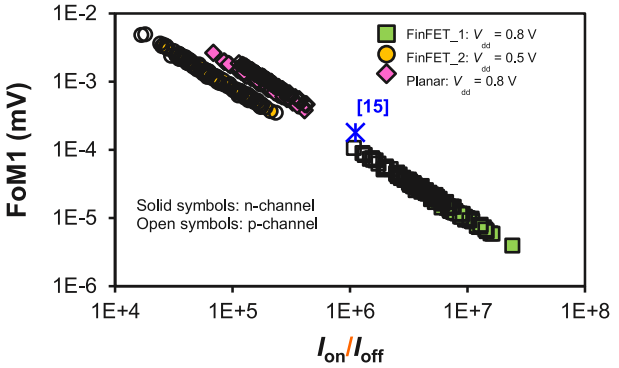


FIGURE 2. **$V_{t,sat}$ versus log I_{on}/I_{off}. The $V_{t,sat}$ value strongly affects the I_{on}/I_{off} value. FinFET_2, due to the design of the LVT scheme, shows a smaller I_{on}/I_{off} value than FinFET_1, which is classified as an SVT device.**

is because of the requirement of low power (logic transistor) applications. I_{on}/I_{off} of about 10^6 is defined as the "threshold" to ensure good gate control over the channel potential barrier height (for SVT devices). FinFET_2, classified as an LVT device, shows a much smaller I_{on}/I_{off} value than FinFET_1. A low $V_{t,sat}$, due to the requirement of high performance (logic transistor) applications, cannot have a large I_{on}/I_{off} [10]. In addition, the planar MOSFET can obtain a larger I_{on}/I_{off} compared to FinFET_2. (For the planar MOSFET, it has become increasingly difficult to ensure that the gate control is strong.) This illustrates again the design of $V_{t,sat}$ decides the value of the I_{on}/I_{off}. In other words, $V_{t,sat}$ becomes the most important factor in reflecting the performance. Interestingly, the I_{on}/I_{off} of the planar MOSFET is also affected by both the ΔV_{DIBL} and the ΔV_{SS} values (Fig. 1). Therefore, the trend of increasing I_{on}/I_{off} for planar MOSFETs is not the same as for FinFETs. In addition, planar bulk's p–channel devices, having higher $V_{t,sat}$ (180 mV to 220 mV), can get a larger I_{on}/I_{off}. (That is why ΔV_{DIBLSS} is larger than for n–channel devices, but the I_{on}/I_{off} value is comparable to n–channel devices.) Similarly, for p–FinFET devices, the value of the I_{on}/I_{off} (of FinFET_1) is actually smaller than for n–FinFET devices due to a smaller $V_{t,sat}$. On the other hand, the short–channel behaviors of n– and p–channel FinFET_2 devices are quite similar.

Fig. 3(a) shows the plot of log FoM1, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, versus log I_{on}/I_{off}. A trend of an increasing I_{on}/I_{off} with a decrease in FoM1 is observed, which is consistent with the finding in previous studies [1], [2]. The FoM1 of FinFET_1 is lower than that of FinFET_2. This is mainly due to the design of $V_{t,sat}$ for FinFET_1, causing it to have a large I_{on}/I_{off}, as discussed earlier (Fig. 2). In other words, $V_{t,sat}$ decides the I_{on}/I_{off} value. This I_{on}/I_{off} in turn affects the FoM1 value. Furthermore, even if $V_{t,sat}$ is low, the FinFET_2 of this work is recognized as having comparable FoM1 to the planar MOSFET. This is attributed to the better control of SCEs, which results in small DIBL and steep SS values. Also, the smaller FoM2 value compared to the FoM1 value is due to the exclusion of ΔV_{SS} (Fig. 3(b)). However, the FoM2 follows similar trend as the FoM1. (As the I_{on}/I_{off} increases, the FoM2 decreases.) This proves that the value of FoM2 can be used to monitor the electrical characteristics of scaled MOSFETs (planar and FinFET devices). Normally, the FoM1 (and the FoM2) of about 10^{-4} mV and about 10^{-2} mV is required for SVT and LVT, respectively. For FinFET_1, the FoM1 (and the FoM2) at the n–channel is smaller than the FoM1 (and the FoM2) at the p–channel. This is mainly because of the influence of I_{on}/I_{off} on the



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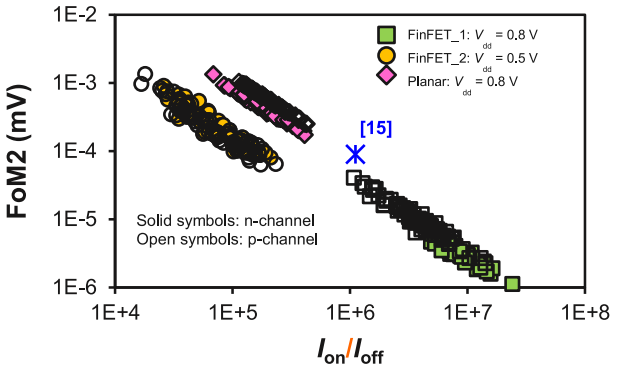
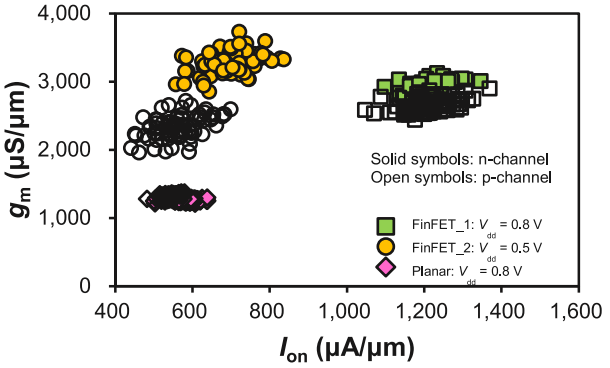


(b)

FIGURE 3. (a) Log FoM1, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, versus log I_{on}/I_{off}. (b) Log FoM2, $\Delta V_{DIBL}/(I_{on}/I_{off})$, versus log I_{on}/I_{off}. An interesting phenomenon happens when FinFET_2 is classified as an LVT device; it is hard to get small FoM1 and FoM2 values. FoMs of about 10^{-4} mV and 10^{-2} mV are necessary (to meet the control requirement of SCEs) for SVT and LVT, respectively.



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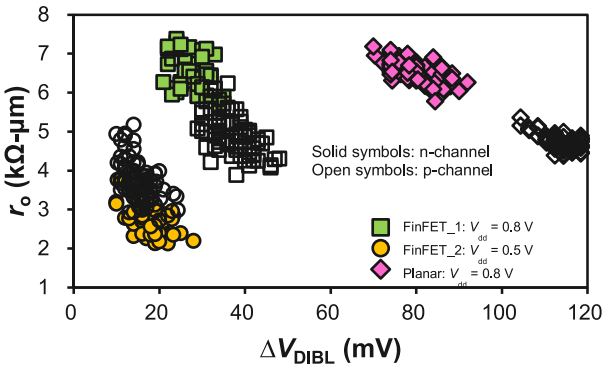


(b)

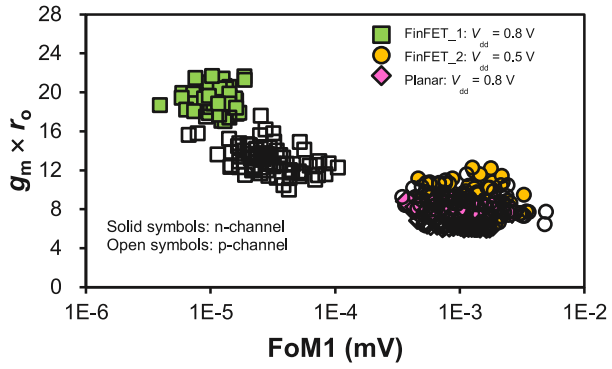
FIGURE 4. (a) g_m versus I_{on}. (b) r_o versus ΔV_{DIBL}. The improved DIBL and SS values help to obtain desirable values of g_m and r_o. The smaller r_o for FinFET_2 is due to its lower V_{dd} (= 0.5 V) value [12].

FoMs. For FinFET_2, values of FoM1 (and FoM2) for both n–channel and p–channel are almost the same. For planar bulk, based on the same FoMs, p–channel gets even higher I_{on}/I_{off} than n–channel by having higher $V_{t,sat}$ (Fig. 2).

Note also that the gap between FoM2 trend lines of FinFET_1 and FinFET_2 observed is due to the exclusion of ΔV_{SS}. Since only ΔV_{DIBL} is presented in the numerator of the FoM2, the smaller ΔV_{DIBL} value (30 mV) compared to the ΔV_{DIBLSS} value (100 mV) results in a smaller FoM2. In addition, Fig. 3(b) is a plot of log FoM2 versus log I_{on}/I_{off}, which is intimately related to log scale behaviors. As a result, the gap between FoM2 trend lines of FinFET_1 and FinFET_2 is expected to be observed. Since highly scaled MOSFETs need to meet the $\Delta V_{DIBLSS} = 100$ mV requirement, the design of $V_{t,sat}$ becomes even more important to the FoM1 (and the FoM2). It will be an important challenge to make these FoMs smaller without using a high $V_{t,sat}$.

Fig. 4(a) illustrates the g_m of scaled n– and p–channel MOSFETs. It can be shown that due to degradation of gate control over the channel potential barrier height, the planar MOSFETs exhibit poorer g_m than the FinFETs. Furthermore, since FinFET_2 has better SS than FinFET_1, it is expected to get a better g_m. We observe that the value of the g_m in n–FinFET_2 is higher than p–FinFET_2. We attribute this to the fact that the hole mobility in the channel is not enhanced by the SiGe structure in comparison to p–FinFET_1. Nevertheless, the desired short–channel behaviors (negligible ΔV_{DIBL}, small ΔV_{SS}, low leakage current) are still observed in p–FinFET_2. A plot of r_o versus ΔV_{DIBL} shows that the r_o tends to increase as the ΔV_{DIBL} is reduced (Fig. 4(b)). We also observe that the influence of ΔV_{DIBL} on r_o is strong [11]. This is more obvious for planar devices. Since FinFETs exhibit better SCEs control, the slope of the r_o versus ΔV_{DIBL} line is steeper than its planar counterpart. This explains the I_{on}/I_{off} independence on ΔV_{DIBL} (and ΔV_{SS}) shown in Fig. 1.

Two observations of r_o versus ΔV_{DIBL} are discussed: (1) Both FinFET_1 and planar bulk show that the p–channel r_o value is smaller than the n–channel due to SCEs. (2) For FinFET_2, the p–channel r_o value being slightly larger than the n–channel indicates that the SCEs are relatively smaller. In other words, different channel geometries may be resulted from the difference of S/D structures: (a) Si S/D for planar bulk's n–channel devices, (b) SiGe S/D for both p–channel planar bulk and FinFET devices, and (c) In–situ phosphorus–doped Si S/D [1], [2] for both



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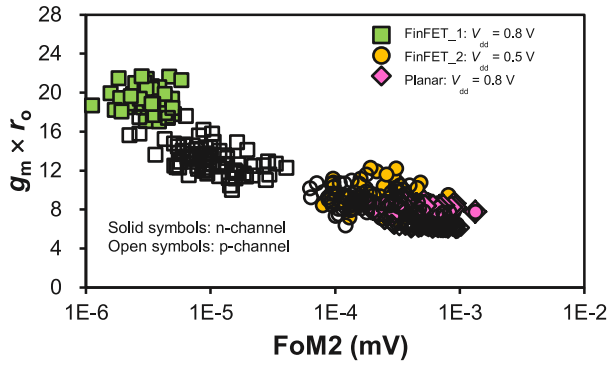
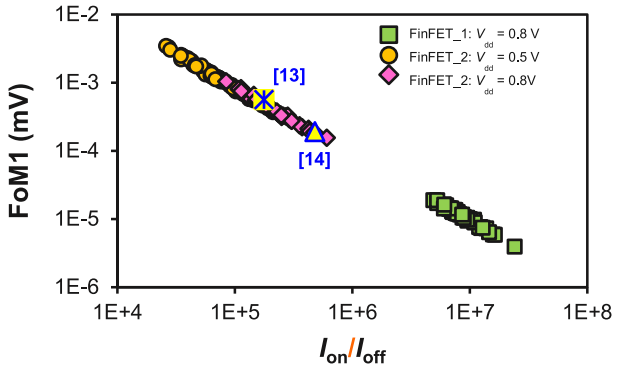


(b)

FIGURE 5. (a) $g_m \times r_o$ versus log FoM1, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$. (b) $g_m \times r_o$ versus log FoM2, $\Delta V_{DIBL}/(I_{on}/I_{off})$. Because of the smaller r_o, the gain of FinFET_2 is smaller than that of FinFET_1.



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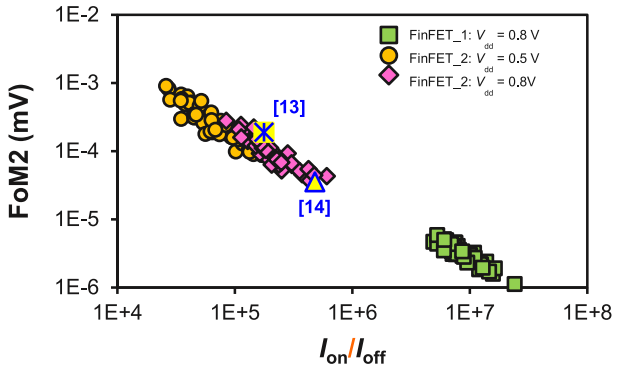

(b)

FIGURE 6. (a) Log FoM1, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, versus log I_{on}/I_{off}. (b) Log FoM2, $\Delta V_{DIBL}/(I_{on}/I_{off})$, versus log I_{on}/I_{off}. Increasing V_{dd} would not increase sharply both FoM1 and FoM2 for FinFET_2, but their values are limited by the design of the LVT scheme. (FoM1 and FoM2 for FinFET_2 can even be slightly decreased at V_{dd} = 0.8 V because of the advantage of DIBL suppression.)

n–channel FinFET_1 and FinFET_2 devices. Since the channel is between the source and the drain, the S/D structure may determine the final channel geometry (and the mobility) and the short–channel behaviors. This explains the transistor behaviors for r_o versus ΔV_{DIBL} that the SCEs are slightly different in n– and p–channel MOSFETs.

The data in Fig. 5 indicate that FinFET_1 shows larger $g_m \times r_o$ than FinFET_2. In other words, the value of the r_o decides the value of the $g_m \times r_o$ since the g_m of FinFET_2 is similar to that of FinFET_1, where the g_m levels are in the same scope. As a result, larger r_o results in larger intrinsic gain. Recall that FinFET_2 has better SS than the planar bulk. This means that the value of the g_m of FinFET_2 is higher. Also, FinFET_2 has a smaller r_o than the planar bulk. Therefore, the $g_m \times r_o$ behaviors of FinFET_2 and planar bulk are quite similar. For both FinFET_2 and planar bulk, evidence is shown that the values of $g_m \times r_o$ for both n–channel and p–channel are almost the same. On the other hand, for FinFET_1, the larger r_o value of the n–channel results in larger $g_m \times r_o$ compared to the p–channel. These data also suggest that if both values of FoM1 and FoM2 are in the same scope, then the $g_m \times r_o$ value would be quite similar. Actually, for these two MOSFETs (FinFET_2 and planar bulk), we may say that their $g_m \times r_o$ values are lumped together.

We further investigate the effect of V_{dd} = 0.8 V on performance characteristics of FinFET_2. Planar bulk as well as the p–channel devices is excluded for simplicity. In Fig. 6, the FoM1 (and the FoM2) dependence on the I_{on}/I_{off} is plotted. Because adequate control of SCEs results in small DIBL and steep SS, FinFET_2 at V_{dd} = 0.8 V shows desirable FoM1 and FoM2 values that are even smaller than at V_{dd} = 0.5 V. Again, we proved that the design of $V_{t,sat}$ decides the values of FoM1 and FoM2. The $g_m \times r_o$ versus log FoM1 characteristics are shown in Fig. 7(a). It is interesting to note that the $g_m \times r_o$ value is significantly increased in FinFET_2 at V_{dd} = 0.8 V. This is attributed to larger r_o [12]. Additionally, trends in $g_m \times r_o$ versus log FoM2 in FinFET_2 are quite similar to $g_m \times r_o$ versus log FoM1 (Fig. 7(b)). We observe that the gate controllability over the channel is strong enough to maintain and improve short–channel performance (for FinFET_2).

In this study, we also include some state–of–the–art scaled devices in [13] and [14] for comparison (Fig. 6). As the improved DIBL and SS values in the short–channel regime are obtained, both FoM1 and FoM2 tend to be decreased. We observe that $V_{t,sat}$ is a key design parameter in assessing

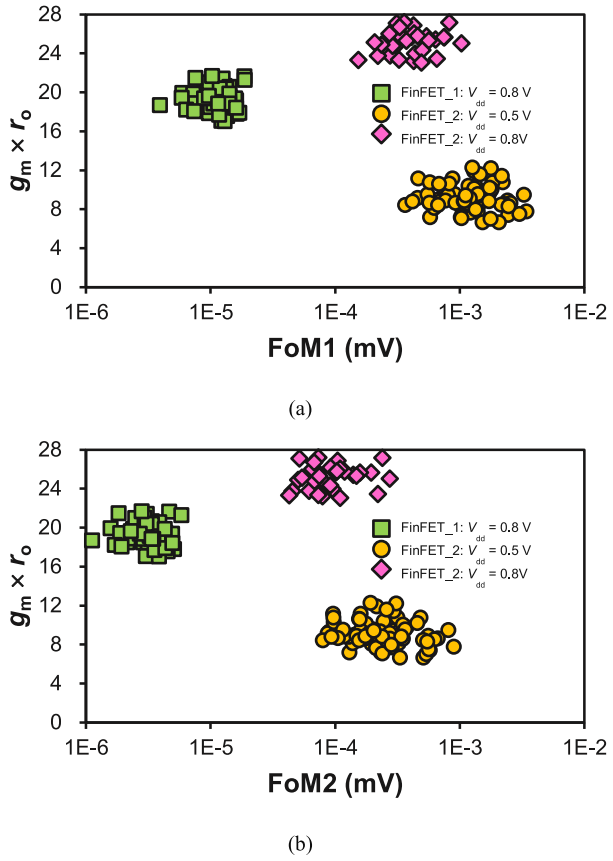

FIGURE 7. **(a) $g_m \times r_o$ versus log FoM1, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$. (b) $g_m \times r_o$ versus log FoM2, $\Delta V_{DIBL}/(I_{on}/I_{off})$. The key finding is that FinFET_2 (at $V_{dd} = 0.8$ V) can get better channel control than FinFET_1 can, leading to a better intrinsic gain.**

the FoMs. (A 32 nm high–κ/metal gate transistor can get even smaller FoM1 and FoM2 values because of the better control of SCEs, as well as higher $V_{t,sat}$ [15] as shown in Fig. 3.) Also, when the measurement of ΔV_{SS} is omitted, the FoM2 of the state–of–the–art scaled devices still follows similar trend as the FoM1.

IV. CONCLUSION

$\Delta V_{DIBLSS}/(I_{on}/I_{off})$ and $\Delta V_{DIBL}/(I_{on}/I_{off})$ used to report the performance of scaled MOSFETs have been demonstrated by experiments. We have shown that the I_{on}/I_{off} of about 10^4 and about 10^6 is required for high performance and low power applications, respectively. ΔV_{DIBLSS} of about 100 mV is necessary to ensure good gate control over the channel of a transistor; therefore, the design of $V_{t,sat}$ decides both $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ and $\Delta V_{DIBL}/(I_{on}/I_{off})$ values. Also, $\Delta V_{DIBL}/(I_{on}/I_{off})$ may be used as a quick feedback of overall device characteristics with reduced measuring time. Performance metrics (e.g., I_{on}/I_{off} and $g_m \times r_o$) can be reflected through $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ and $\Delta V_{DIBL}/(I_{on}/I_{off})$ since SCEs, which introduce severe performance degradation for scaled MOSFETs, are attained through the use of these two figures of merit. Therefore, it is desirable to have small values of $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ and $\Delta V_{DIBL}/(I_{on}/I_{off})$ so that the highly scaled MOSFETs remain functional with further scaling.

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