Received 18 October 2018; revised 31 December 2018; accepted 30 January 2019. Date of publication 4 February 2019; date of current version 1 March 2019. The review of this paper was arranged by Editor M. K. Radhakrishnan.

Digital Object Identifier 10.1109/JEDS.2019.2897286

Impact of Work Function Variation, Line-Edge Roughness, and Ferroelectric Properties Variation on Negative Capacitance FETs

VITA PI-HO HU (Member, IEEE), PIN-CHIEH CHIU (Student Member, IEEE), AND YI-CHUN LU (Student Member, IEEE)

Department of Electrical Engineering, National Central University, Taoyuan 320, Taiwan

CORRESPONDING AUTHOR: V. P.-H. HU (e-mail: vitahu@ee.ncu.edu.tw)

This work was supported by the Young Scholar Fellowship Program by Ministry of Science and Technology (MOST), Taiwan, under Grant MOST107-2636-E-008-001 and Grant MOST108-2636-E-008-001.

ABSTRACT In this paper, the impacts of work function variation (WFV), line-edge roughness (LER), and ferroelectric properties variation on the threshold voltage, subthreshold swing (SS), Ion, and Ioff variations are analyzed comprehensively for negative capacitance ultra-thin body SOI MOSFETs (NC-SOI) compared with SOI MOSFETs (SOI). For LER induced threshold voltage variation (σVt), NC-SOI MOSFETs exhibit smaller σVt (= 3.8 mV) than the SOI MOSFETs (σVt = 17.6 mV). For analyzing WFV of NC-SOI MOSFETs, two scenarios are considered including (I) same WFV patterns, and (II) different WFV patterns between the external and internal metal gates. Compared with SOI, NC-SOI with scenario (I) exhibits comparable WFV induced σVt (= 16.2 mV), and NC-SOI with scenario (II) exhibits larger WFV induced σVt (= 28.5 mV). In scenario (II), different WFV patterns between the internal and external gates result in V_{FE} (voltage drop across the ferroelectric layer) variations, which increases the WFV induced σVt for NC-SOI. LER dominates energy-delay product variations (σEDP), and NC-SOI MOSFETs show smaller σEDP than SOI MOSFETs. Besides, NC-SOI MOSFETs with thicker ferroelectric layer thickness (T_{FE}), larger coercive electric field (E_C), and smaller remnant polarization (P_0) show smaller LER induced σVt and σSS. Ferroelectric properties variations show negligible impact on the WFV induced σVt and σSS.

INDEX TERMS Line-edge roughness, work function variation, negative capacitance FET (NCFET), ferroelectric properties.

I. INTRODUCTION

Ultra-low power integrated circuits are important for Internet-of-Things (IoT) applications and energy harvesting system. Devices with higher Ion/Ioff ratio and steep slope switching are essential to achieve the requirement of ultra-low power systems. Negative capacitance FET (NCFET) [1] is a promising device owing to its better subthreshold swing and scalability [2]. Therefore, NCFET has been actively explored in many aspects. For example, negative capacitance ultra-thin-body SOI MOSFETs (NC-SOI) have been analyzed for performance enhancements through capacitance tuning [3], [4]. Khan *et al.* [3] showed that the relative improvement in device performance due to negative capacitance of ferroelectric layer becomes more significant in short channel devices due to the increased drain-to-channel coupling. Yeung *et al.* [4] showed that NC-SOI MOSFET with ultra-thin body thickness (T_{ch} = 0.5nm) can achieve 10pA/μm I_{OFF}, 200μA/μm I_{on} at supply voltage = 0.3V. NCFETs with sub-10nm ferroelectric layer were fabricated and analyzed [5]–[7]. Lee *et al.* [6] experimentally demonstrated NCFET with 1.5nm HZO ferroelectric layer which paves a promising solution for sub-10nm technology node. The circuit performance of NCFET has also been examined [8]–[11]. Khandelwal *et al.* [8] showed that NC-FinFET improves inverter delay by 11 times compared to 14 nm base FinFET at 0.2V supply voltage. Yuan *et al.* [9]

2168-6734 © 2019 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

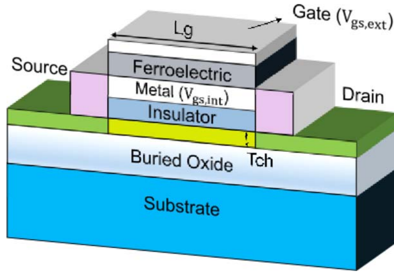

FIGURE 1. The schematic of NC-SOI MOSFET. $V_{gs,ext}$ is the external metal gate voltage, and $V_{gs,int}$ is the internal metal gate voltage which is amplified by ferroelectric layer with negative capacitance. FE layer is the ferroelectric layer.

showed that a low viscosity ($\rho < 0.1\Omega$-m) is required for NCFET to operate at the high gigahertz frequencies. The operation speed of NCFET has been analyzed [12]–[14], and Kobayashi *et al.* [13] showed that NCFET can operate at > MHz, which is suitable for ultralow power IoT application. The leakage from the ferroelectric layer in NCFET results in degradation of the NCFET performance [15], [16]. The line-edge roughness (LER) induced variability [17], [18] for NCFETs have been presented. Lee and Su [17] showed that NC-FinFETs exhibit superior immunity to Fin-LER induced variations. The impact of ferroelectric parameters, such as such as remnant polarization (P_0), coercive electric field (E_c), ferroelectric thickness (T_{fe}) have been discussed [19]–[21]. Lin *et al.* [19] showed that increasing T_{FE} and E_C, and decreasing P_0 can enhance the voltage amplification factor (A_V) for NCFETs. Pahwa *et al.* [20] showed that compared with MFMIS NCFET, MFIS NCFET is more prone to hysteresis and shows hysteresis at a lower ferroelectric layer thickness. However, the analysis of NCFETs considering the combined effects of intrinsic process variations and ferroelectric properties variation has rarely been examined.

In this work, the impact of work function variation (WFV), LER, and ferroelectric properties variation on NCFETs are analyzed comprehensively. This paper is organized as follows. Section II describes the simulation framework and device parameters used in this work. To analyze the WFV of NC-SOI MOSFETs comprehensively, the external and internal metal gates are assumed to have the same (Scenario I) and different (Scenario II) WFV patterns, respectively. In Section III, WFV and LER induced variations are analyzed for NC-SOI MOSEFTs compared with SOI MOSFETs. Impacts of LER and WFV on the power-delay product variability and energy-delay product variability have also been analyzed. In Section IV, the impact of ferroelectric properties variation on the WFV and LER induced threshold voltage and subthreshold swing variations are investigated. The conclusion is drawn in Section V.

II. DEVICE DESIGN AND METHODOLOGY

Fig. 1 shows the schematic of NC-SOI MOSFET used in this work. The device parameters are designed with gate length Lg = 20.2 nm, device width W = 25 nm, channel thickness Tch = 3 nm and EOT (insulator shown in Fig. 1) = 0.65 nm for both NC-SOI and SOI MOSFETs. The coercive electric field E_C = 1 MV/cm, remnant polarization P_0 = 10 μC/cm^2 [22], and the thickness of ferroelectric (FE) layer T_{FE} = 4.5 nm are used for NC-SOI MOSFETs to achieve hysteresis-free design. The hysteresis phenomenon must be avoided for logic applications.

To investigate the LER induced variations, the line edge roughness patterns are generated based on Fourier synthesis approach [23] with the root-mean-square (rms) amplitude Δ = 1.67 nm and correlation length Λ = 20 nm [24], and then atomistic Monte Carlo simulations were performed in TCAD. To assess WFV, an analytical model considering metal material, and possible grain orientations with corresponding probability were considered [25]. The average metal grain size is 4.3nm [26]. For analyzing the WFV induced variations of NC-SOI MOSFETs, two scenarios are considered including (I) the external and internal metal gates have the same WFV patterns, and (II) the external and internal metal gates have different WFV patterns. The drain current versus gate voltage (I_d-V_g) and gate charge versus gate voltage (Q_{MOS}-V_g) of SOI MOSFETs considering LER and WFV were obtained in TCAD simulations. Then, the static Landau equation (dP/dt = 0) is used to derive the voltage of ferroelectric layer (V_{FE}). The electric field in ferroelectric layer (E_{FE}) [27] can be expressed as

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \quad (1)$$

where P is polarization of ferroelectric layer. In this work, γ is assumed to be 0, because the third term P^5 in equation (1) is negligible [28]. The gate charge per unit area of SOI MOSFETs (Q_{MOS}) can be expressed as $Q_{MOS} = P + \epsilon_0 E \approx P$ [27] if electric field is not high (i.e., $E \ll \epsilon_0^{-1}$, where ϵ_0 is the vacuum permittivity). V_{FE} can be expressed as $E_{FE} \times T_{FE} = (2\alpha Q_{MOS} + 4\beta Q_{MOS}{}^3) \times T_{FE}$. In other words, V_{FE} is a function of gate charge Q_{MOS}, and Q_{MOS} equals to the ferroelectric charge Q_{FE}. For NC-SOI MOSFETs, the external gate voltage can be expressed as

$$V_{gs,ext} = V_{gs,int} + V_{FE} \quad (2a)$$

$$V_{gs,ext} = V_{gs,int} + \left(2\alpha Q_{MOS} + 4\beta Q_{MOS}{}^3\right) \times T_{FE} \quad (2b)$$

where $V_{gs,int}$ is the internal gate voltage of NC-SOI MOSFETs. $V_{gs,int}$ is assumed to be equal to the gate voltage V_g of SOI MOSFETs. Then, we can obtain the I_d vs. $V_{gs,ext}$ and Q_{MOS} vs. $V_{gs,ext}$ characteristics of NC-SOI MOSFETs. The I_d vs. $V_{gs,ext}$ characteristics of NC-SOI MOSFETs using the simulation methodology in this work have been calibrated with TCAD simulator in which the Landau-Khalatnikov (L-K) theory self-consistently coupled with the Poisson's and current continuity equations for NCFET analysis. The coefficients α and β are related to the ferroelectric parameters, remnant polarization P_0 and coercive field E_C. Ec is defined as the electric field when $dE_{FE}/dP = 0$, and P_0 is defined as the polarization when $E_{FE} = 0$. According to these two conditions, α and β can be solved to be expressed as [27]

$$\alpha = -\frac{3\sqrt{3}}{4}\frac{E_C}{P_0} \text{ and } \beta = -\frac{3\sqrt{3}}{8}\frac{E_C}{P_0{}^3} \quad (3)$$

The internal gate voltage is amplified by amplification factor A_V which is defined as

$$A_V \equiv \frac{\partial V_{gs,int}}{\partial V_{gs,ext}} = \frac{C_{FE}}{C_{FE} + C_{MOS}} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \quad (4)$$

where C_{MOS} is the capacitance of baseline SOI MOSFETs underneath the FE layer, and C_{FE} is the capacitance of FE layer. The subthreshold swing (SS) of NC-SOI MOSFETs at $V_{gs,ext} = 0V$ can be improved against SOI counterparts, and can be described as [4]

$$SS_{NC-SOI} = \frac{SS_{baseline\ SOI}}{A_V} \quad (5)$$

According to equations (4) and (5), it can be known that higher A_V and larger improvements in SS for NC-SOI MOSFETs can be achieved by better capacitance matching between C_{MOS} and $|C_{FE}|$ (i.e., C_{MOS} should be close to and smaller than $|C_{FE}|$ to achieve higher A_V). In this work, the variability comparisons between SOI and NC-SOI MOSFETs are analyzed comprehensively considering the combined effects of intrinsic process variations and ferroelectric properties variations. The leakage through FE layer [15] is not considered in this work.

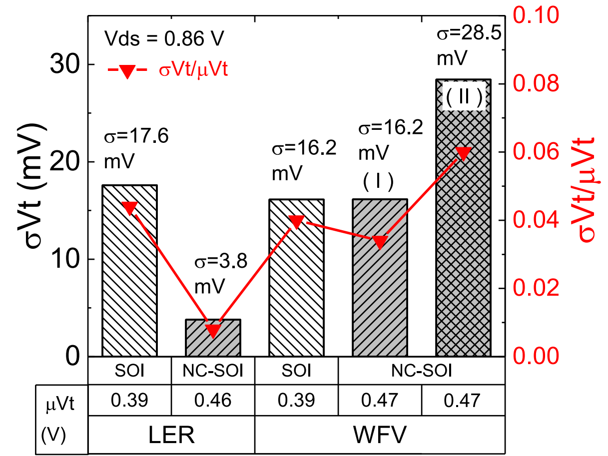

FIGURE 2. Threshold voltage variations (σVt) comparisons between SOI and NC-SOI MOSFETs considering LER and WFV. Compared to SOI MOSFETs, LER induced σVt and the normalized threshold voltage variations (σVt/μVt) can be suppressed by negative capacitance effect in NC-SOI MOSFETs. However, for WFV, NC-SOI MOSFETs show comparable WFV (scenario I) induced σVt and larger WFV(scenario II) induced σVt and σVt/μVt than SOI MOSFETs. Scenario I means the external and internal gate have the same WFV patterns, and scenario II means the external and internal gate have different WFV patterns. The red symbol line shows the normalized threshold voltage variations (σVt/μVt). σVt and μVt are the standard deviation and mean value of Vt variations.

III. IMPACT OF LER AND WFV ON NC-SOI MOSFETS

In this section, line edge roughness (LER) and work function variation (WFV) induced threshold voltage variations (σVt), power-delay product variations (σPDP), and energy-delay product variations (σEDP) for NC-SOI MOSFETs are analyzed comprehensively.

A. LER INDUCED VARIATIONS

Fig. 2 shows the σVt comparisons between SOI and NC-SOI MOSFETs considering LER and WFV, respectively. Compared with SOI MOSFETs, NC-SOI MOSFETs show smaller LER induced σVt (= 3.8 mV) than SOI MOSFETs (σVt = 17.6 mV). Fig. 3(a) and 3(b) show the Vt difference ($Vt_{NC-SOI} - Vt_{SOI}$) between SOI and NC-SOI MOSFETs versus Vt considering LER and WFV, respectively. The threshold voltage of NC-SOI MOSFET (Vt_{NC-SOI}) is equal to certain $V_{gs,ext}$, and threshold voltage of SOI MOSFET (Vt_{SOI}) is equal to certain $V_{gs,int}$ when I_d equals [100nA/μm×(W/Lg)]. Therefore, Vt difference ($Vt_{NC-SOI} - Vt_{SOI}$) is related to V_{FE} and A_V according to Eq. (2a) and Eq. (4). Fig. 3(c) shows SS versus A_V characteristics for NC-SOI MOSFETs considering LER and WFV (shown in inset). The SS of SOI MOSFETs are also plotted in Fig. 3(c) for comparisons although SOI MOSFETs do not have A_V characteristics. For considering LER in Fig. 3(a) and 3(c), SOI MOSFET with the shortest average Lg and the worst short channel effects (SCE) exhibits the smallest Vt and the highest SS. As can be seen, NC-SOI MOSFET shows the largest ($Vt_{NC-SOI} - Vt_{SOI}$) and highest A_V when its baseline SOI device underneath the FE layer exhibits the worst SCE. This is because as Lg decreases, the drain-to-channel field coupling is increased which increases C_{MOS}, thus showing better capacitance matching and higher A_V. However, NC-SOI MOSFET shows smaller ($Vt_{NC-SOI} - Vt_{SOI}$) and lower A_V when its baseline SOI device exhibits larger Vt, lower SS, and better SCE control. Therefore, NC-SOI MOSFETs exhibit smaller LER induced σVt and σSS than the SOI MOSFETs, and LER induced σVt and σSS can be suppressed by negative capacitance effect.

B. WFV INDUCED VARIATIONS

In contrast to LER induced σVt in NC-SOI MOSFETs, NC-SOI MOSFETs show comparable WFV (scenario I) induced σVt (= 16.2 mV) and larger WFV (scenario II) induced σVt (= 28.5 mV) compared with SOI counterparts as shown in Fig. 2. Fig. 3(b) shows that for SOI MOSFETs, WFV only induces Vt variations, and shows negligible impact on σSS as shown in the inset of Fig. 3(c). For NC-SOI MOSFET with WFV (scenario I), Vt difference ($Vt_{NC-SOI} - Vt_{SOI}$) is a constant, thus showing comparable WFV(I) induced σVt compared with SOI counterparts as shown in Fig. 3(b). Besides, WFV shows negligible impact on A_V as shown in the inset of Fig. 3(c), because WFV only shifts C_{MOS} horizontally. Therefore, NC-SOI MOSFETs with WFV (scenario I) exhibit negligible σSS.

For NC-SOI MOSFETs with different WFV patterns between the external and internal gates (scenario II), there is a work function difference between the external and internal metal gates (across the FE layer), which results in V_{FE} variations as shown in Fig. 4. Therefore, WFV (scenario II) shows

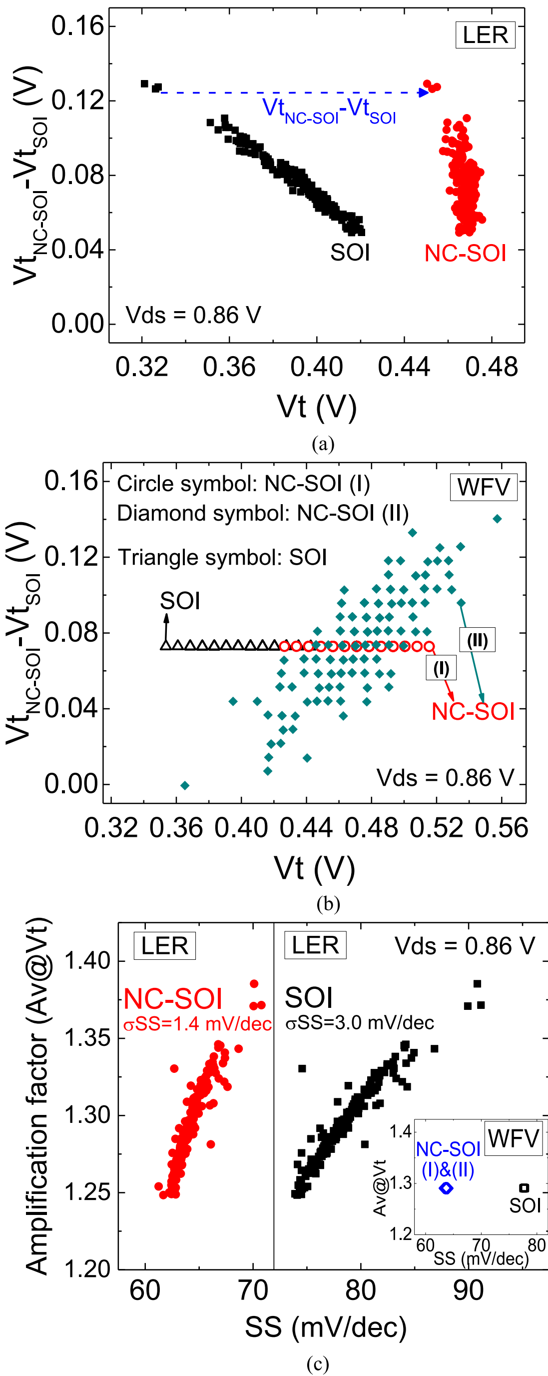

FIGURE 3. The Vt difference (= $Vt_{NC-SOI} - Vt_{SOI}$) between SOI and NC-SOI MOSFETs versus Vt when considering (a) LER and (b) WFV. According to equation (2), Vt difference (= $Vt_{NC-SOI} - Vt_{SOI}$) is related to V_{FE}. The blue arrow in (a) indicates the Vt difference between SOI and NC-SOI. (c) The amplification factor (A_V@Vt) versus subthreshold swing (SS) characteristics considering LER and WFV (shown in the inset). For LER, NC-SOI with larger SS exhibits higher Av. However, WFV introduces flat-band variations and Vt variations; while WFV shows negligible impact on the subthreshold swing variations. The SS characteristics of SOI MOSFETs are plotted in Fig. 3(c) for comparisons although SOI MOSFETs do not have A_V characteristics.

larger ($Vt_{NC-SOI} - Vt_{SOI}$) variations (Fig. 3(b)) and larger σVt (= 28.5 mV) than WFV (scenario I) (σVt = 16.2 mV) for NC-SOI MOSFETs.

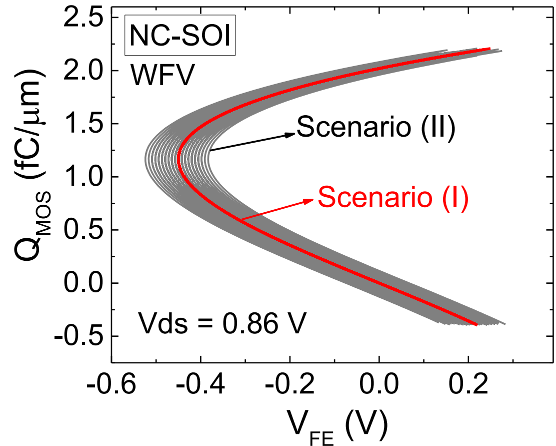

FIGURE 4. The gate charge (Q_{MOS}) versus V_{FE} characteristics of NC-SOI MOSFETs considering WFV(I) and WFV(II). For WFV(I), the external and internal gates have the same WFV patterns, and thus no V_{FE} variation. For WFV(II), the external and internal gates have different WFV patterns, which means there is a work function difference between external and internal metal gates. Therefore, WFV(II) shows V_{FE} variations. In this figure, Q_{MOS} increases as $V_{gs,ext}$ increases.

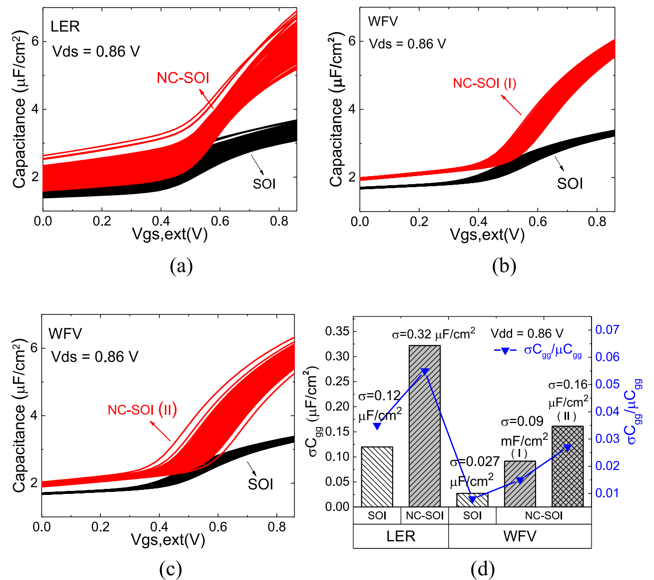

FIGURE 5. Gate capacitance dispersions for NC-SOI MOSFETs considering (a) LER, (b) WFV(I), and (c) WFV(II), respectively, compared with SOI counterparts. (d) The comparisons of gate capacitance variations (σC_{gg}) for NC-SOI and SOI MOSFETs at V_{dd} = 0.86V. NC-SOI MOSFETs show larger σC_{gg} than SOI MOSFETs due to A_v variations. For both NC-SOI and SOI MOSFETs, LER exhibits larger σC_{gg} than WFV due to its larger A_v variations. (σ is the standard deviation, and μ is the mean value).

C. POWER-DELAY PRODUCT AND ENERGY-DELAY PRODUCT

Power-delay product (PDP) is a measure of energy consumed per switching event and is defined by the product of power and gate delay. PDP is proportional to ($C_{gg} \cdot V_{dd}^2$), and therfore the PDP variability is determined by the C_{gg} variations. Fig. 5(a), Fig. 5(b), and Fig. 5(c) show the capacitance dispersions of NC-SOI MOSFETs considering

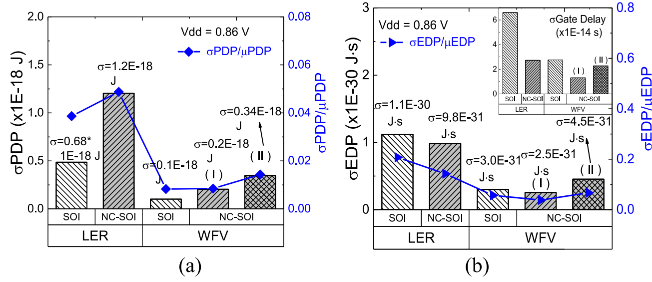

FIGURE 6. (a) Power-delay product variations (σPDP) and (b) energy-delay product variations (σEDP) comparisons for SOI and NC-SOI MOSFETs considering LER and WFV. For fair comparisons, NC-SOI and SOI MOSFETs are analyzed at the same μIoff. For both NC-SOI and SOI MOSFETs, LER dominates σPDP and σEDP compared with WFV. Compared to PDP, EDP is a more preferable metric which is used to balance power and performance. NC-SOI MOSFETs exhibit smaller LER induced σEDP than SOI MOSFETs due to its smaller gate delay variations. (σ is the standard deviation, and μ is the mean value).

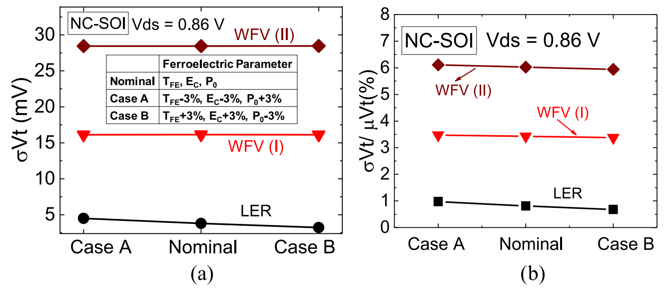

FIGURE 7. Impact of ferroelectric properties variations on (a) Vt variations (σVt) and (b) normalized Vt variations (σVt/μVt) of NC-SOI MOSFETs. Ferroelectric properties variations show negligible impact on WFV induced σVt. However, LER induced σVt can be slightly suppressed in case B compared to case A and nominal case. From case A to case B, σVt/μVt of NC-SOI MOSFET slightly decreases for considering LER, WFV(I), and WFV(II).

LER, WFV(I), and WFV(II), respectively, compared with SOI MOSFETs. Gate capacitance of NC-SOI MOSFET ($C_{gg,NC-SOI}$) is defined as

$$\left(\frac{1}{C_{FE}}+\frac{1}{C_{MOS}}\right)^{-1}=\frac{|C_{FE}|\cdot C_{MOS}}{|C_{FE}|-C_{MOS}}=A_v\cdot C_{MOS}$$

where C_{MOS} is the capacitance of baseline SOI MOSFET. Fig. 5(d) compares the gate capacitance variations (σC_{gg}) at $V_{dd} = 0.86$V. NC-SOI MOSFETs show larger σC_{gg} than SOI counterparts due to A_v variations at $V_{dd} = 0.86$V. For NC-SOI MOSFETs, LER induced σC_{gg} is larger than WFV(I) and WFV(II) induced σC_{gg} because LER exhibits larger A_v variations than WFV(I) and WFV(II).

Fig. 6(a) shows that PDP variations (σPDP) and σC_{gg} (Fig. 5(d)) exhibit similar trend because σC_{gg} dominates σPDP. Besides PDP variability, Fig. 6(b) shows the energy-delay product variations (σEDP) for NC-SOI and SOI MOSFETs. EDP is defined by the product of PDP and gate delay, and EDP is a more preferable metric used to balance the power consumption and delay performance. As can be seen, LER induced σEDP is larger than WFV induced σEDP for both NC-SOI and SOI MOSFETs because LER exhibits larger σPDP and gate delay variations (inset of Fig. 6(b)) than WFV. Although NC-SOI MOSFETs show larger LER induced σPDP than SOI counterparts, NC-SOI MOSFETs show smaller LER induced σEDP than SOI MOSFETs because gate delay variations dominate σEDP. NC-SOI MOSFET exhibits smaller gate delay variations than SOI MOSFET due to its larger effective drive current and smaller gate delay [18].

IV. IMPACT OF FERROELECTRIC PROPERTIES VARIATION

In this section, the impact of ferroelectric properties variation on the LER and WFV induced variations for NC-SOI MOSFETs are analyzed. Three cases are used to evaluate the impact of ferroelectric properties variation include (1) nominal case with $T_{FE} = 4.5$ nm, $E_C = 1$ MV/cm, and $P_0 = 10$ μC/cm^2 [22], (2) case A with $T_{FE} - 3\%$, $E_C - 3\%$, and $P_0 + 3\%$, and (3) case B with $T_{FE} + 3\%$, $E_C + 3\%$, and $P_0 - 3\%$.

A. THRESHOLD VOLTAGE

Fig. 7 shows the impact of ferroelectric properties variation on WFV and LER induced σVt for NC-SOI MOSFETs. As can be seen, LER induced σVt of NC-SOI MOSFETs can be slightly suppressed in case B compared to case A and nominal case. As T_{FE} increases, E_C increases, and P_0 decreases (i.e., from case A to case B), ($Vt_{NC-SOI} - Vt_{SOI}$) and A_V of NC-SOI MOSFET increases [19]. Fig. 8(a) and 8(b) show that for considering LER, as ferroelectric properties change from case A to case B, NC-SOI MOSFET with smaller Vt and larger subthreshold swing (i.e., worse short channel effect) shows larger increases in ($Vt_{NC-SOI} - Vt_{SOI}$) and A_V than the NC-SOI MOSFET with larger Vt and smaller subthreshold swing. In other words, NC-SOI MOSFET with worse short channel effect (i.e., shorter Lg, lower Vt, and higher SS) exhibits larger Vt shift as ferroelectric properties change from case A to case B; while NC-SOI MOSFET with better short channel effect (i.e., longer Lg, larger Vt, and lower SS) exhibits smaller Vt shift as ferroelectric properties change from case A to case B. Therefore, NC-SOI MOSFETs with case B show smaller Vt dispersion and smaller σVt.

Fig. 8(c) shows that for considering WFV, as ferroelectric properties change from case A to case B, NC-SOI MOSFETs with different work function (i.e., Vt) show the same increases in ($Vt_{NC-SOI} - Vt_{SOI}$) and A_V. In other words, as ferroelectric properties change from case A to case B, NC-SOI MOSFETs with different work function exhibit the same amount of Vt shift. Therefore, WFV induced σVt keeps the same for NC-SOI MOSFETs as ferroelectric properties change from case A to case B as shown in Fig. 7.

B. SUBTHRESHOLD SWING

As ferroelectric properties change from case A to case B (i.e., T_{FE} and E_C increasing, and P_0 decreasing), NC-SOI MOSFETs show increase in A_V. According to eq. (5), SS

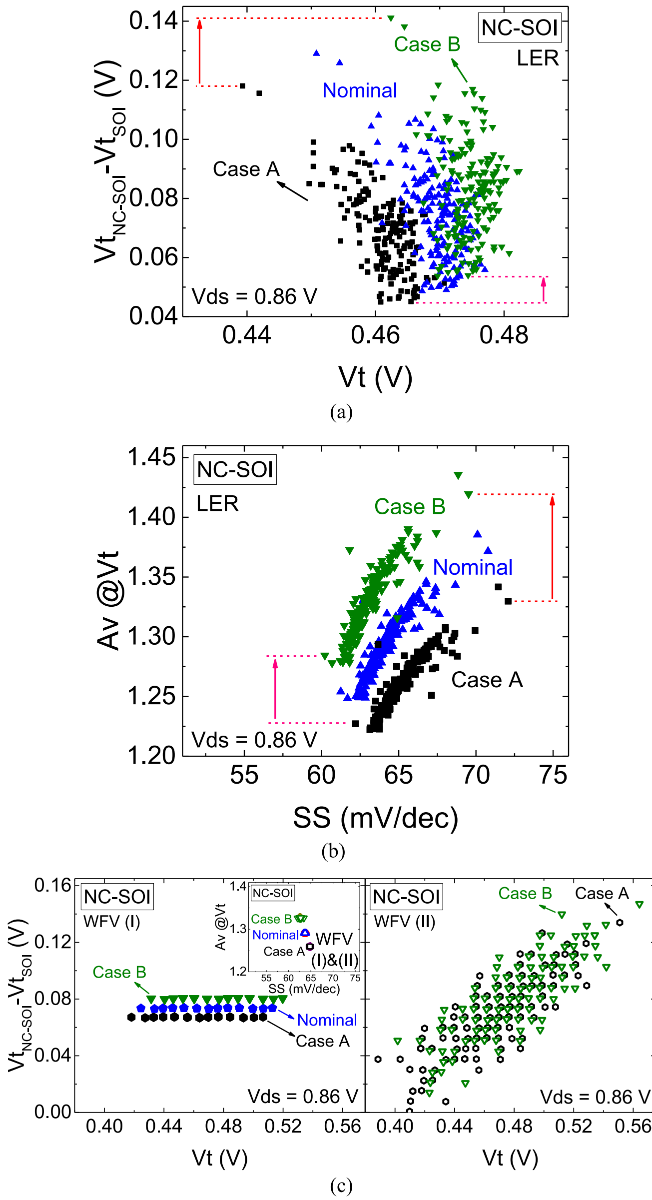

FIGURE 8. (a) Impact of ferroelectric properties variation on ($Vt_{NC-SOI} - Vt_{SOI}$) and Vt dispersion for NC-SOI MOSFETs considering LER. (b) Impact of ferroelectric properties variation on A_V versus SS characteristics for NC-SOI MOSFETs considering LER. (c) Impact of ferroelectric properties variations on ($Vt_{NC-SOI} - Vt_{SOI}$) versus Vt for NC-SOI MOSFETs considering WFV(I) and WFV(II). Fig. 8(a) and 8(c) show that µVt increases from case A to case B.

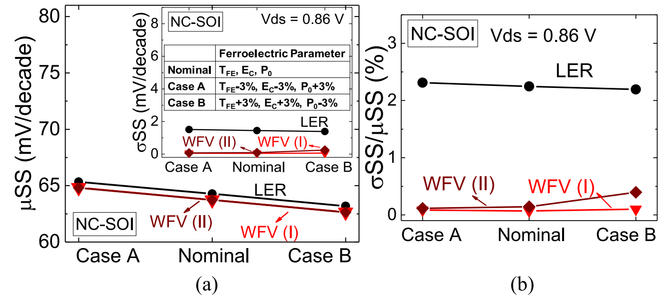

FIGURE 9. (a) Impact of ferroelectric properties variation on the mean of SS (µSS) for NC-SOI MOSFETs. The inset shows the impact of ferroelectric properties variation on SS variation (σSS) for NC-SOI MOSFETs. (b) Impact of ferroelectric properties variation on the normalized subthreshold swing variations (σSS/µSS) of NC-SOI MOSFET. For considering LER, σSS and σSS/µSS can be slightly improved as the ferroelectric parameters changes from case A to case B. For considering WFV(I) and WFV(II), σSS (< 0.5mV/dec) and σSS/µSS (< 0.5%) are quite small, and therefore ferroelectric properties variation shows negligible impact on WFV induced σSS and σSS/µSS.

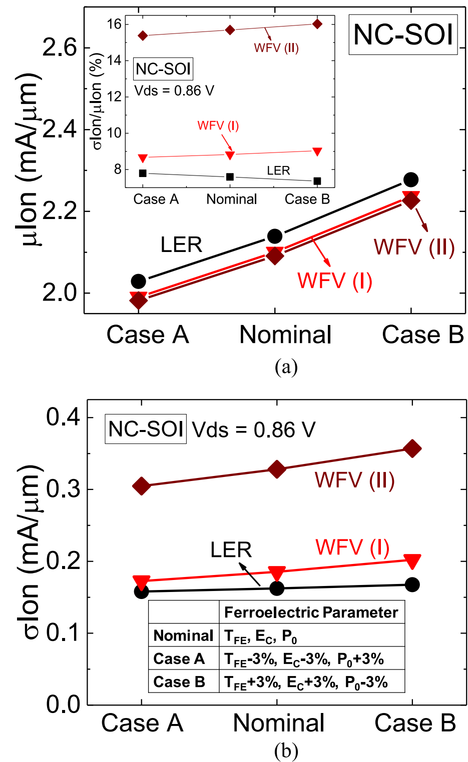

FIGURE 10. Impact of ferroelectric properties variation on (a) mean of Ion (µIon) and (b) Ion variation (σIon) of NC-SOI MOSFETs. As T_{FE} increases, E_C increases, and P_0 decreases (i.e., from case A to case B), µIon increases. Normalized Ion variations (σIon/µIon) is shown in the inset of Fig. 10(a). From case A to case B, WFV(I) and WFV(II) induced σIon and σIon/µIon increases slightly; while LER induced σIon/µIon decreases slightly for NC-SOI MOSFETs.

of NC-SOI (SS_{NC-SOI}) reduces as A_V increases. Therefore, the mean of SS (µSS) of NC-SOI MOSFET decreases from case A to case B as shown in Fig. 9(a). NC-SOI MOSFETs considering LER show worse short channel effect and larger µSS than NC-SOI MOSFETs considering WFV. The inset of Fig. 9(a) and Fig. 8(b) show that for NC-SOI MOSFETs considering LER, subthreshold swing variation (σSS) can be slightly improved from case A to case B. Fig. 9(a) inset shows that NC-SOI MOSFETs considering WFV show negligible σSS (< 0.5 mV/dec).

C. ON AND OFF CURRENTS

Fig. 10(a) shows that µIon of NC-SOI MOSFET increases as ferroelectric properties change from case A to case B, although µVt of NC-SOI MOSFET increases from case A to case B as shown in Fig. 8(a) and 8(c). This is because as T_{FE}

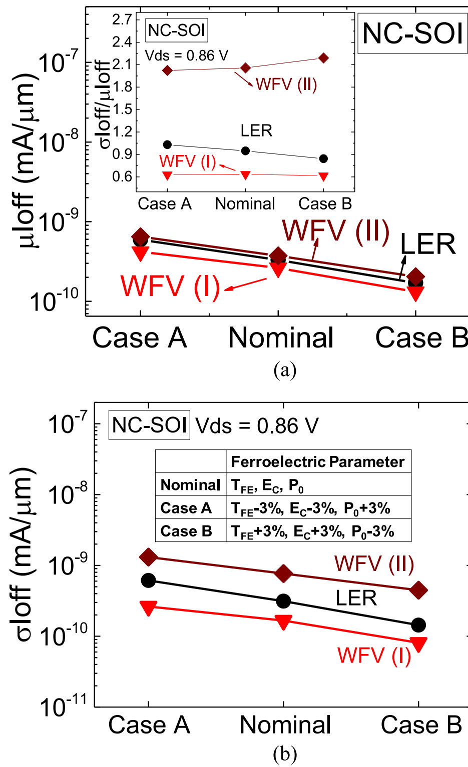

FIGURE 11. **Impact of ferroelectric properties variation on (a) mean of Ioff (μIoff) and (b) Ioff variation (σIoff) of NC-SOI MOSFETs. The inset of Fig. 11(a) shows normalized Ioff variations (σIoff/μIoff). For NC-SOI MOSFETs considering WFV(II), as T_{FE} increases, E_C increases, and P_0 decreases (from case A to case B), μIoff of NC-SOI MOSFETs decreases while WFV(II) induced σIoff/μIoff slightly increases.**

increases, E_C increases, and P_0 decreases (from case A to case B), A_V increases (Fig. 8(b)) thus enhancing transconductance and Ion of NC-SOI MOSFET. σIon of NC-SOI MOSFETs slightly increases from case A to case B due to its increased μIon. Besides, NC-SOI MOSFETs considering WFV(II) exhibit larger σIon than considering LER and WFV(I) due to its higher σVt as shown in Fig. 10(b).

The off state leakage current of MOSEFT is related to Vt and SS (i.e., $I_{off} \propto 10^{-Vt/SS}$). Fig. 11(a) shows that μIoff of NC-SOI MOSFET decreases as ferroelectric properties change from case A to case B due to its enhanced A_V and decreased μSS. NC-SOI MOSFETs considering WFV(II) exhibit higher σIoff than LER and WFV(I) because of its higher σVt, and NC-SOI MOSFETs considering LER show higher σIoff than WFV(I) due to its higher σSS. Fig. 12 shows that compared to SOI MOSFETs, NC-SOI MOSFETs considering LER, WFV(I), and WFV(II) show larger Ion variation (σIon = 0.162 mA/μm, 0.185 mA/μm, and 0.328 mA/μm) and smaller Ioff variation (σIoff = 3.13e-10 mA/μm, 1.67e-10 mA/μm, 7.68e-10 mA/μm), because NC-SOI MOSFETs show larger μIon and smaller μIoff than SOI MOSFETs as shown in Fig. 12. For NC-SOI MOSFETs, WFV(II) with highest σVt dominates the Ioff and Ion variations, and shows largest

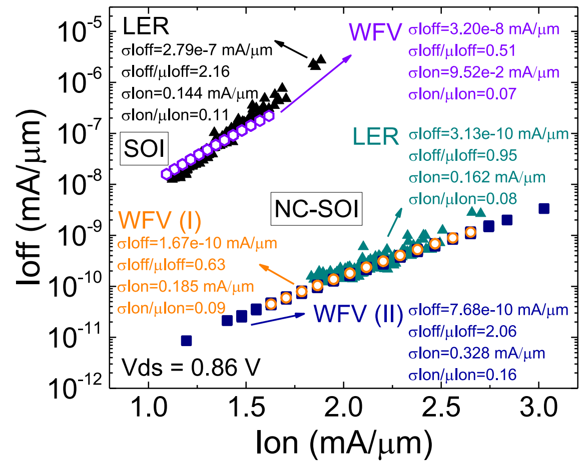

FIGURE 12. **Ioff versus Ion characteristics of SOI and NC-SOI MOSFETs considering LER and WFV. LER dominates the Ion and Ioff variations of SOI MOSFETs, while WFV(II) dominates the Ion and Ioff variations of NC-SOI MOSFETs.**

σIoff/μIoff and σIon/μIon than LER and WFV(I). For SOI MOSFETs, LER dominates the Ion and Ioff variations compared to WFV. NC-SOI MOSFETs with WFV(II) still exhibit smaller σIoff/μIoff than SOI MOSFETs with LER.

V. CONCLUSION

We analyze the threshold voltage, subthreshold swing, Ion, and Ioff variations for NC-SOI MOSFETs considering LER, two scenarios of WFV, and ferroelectric properties variation. For NC-SOI MOSFETs, due to V_{FE} variation, WFV with scenario (II) dominates σVt, σIon, and σIoff compared to LER and WFV(I). Besides, NC-SOI MOSFETs exhibit smaller LER induced σVt and comparable/larger WFV(I)/WFV(II) induced σVt than SOI counterparts. Although NC-SOI MOSFETs show larger WFV(II) induced σVt than SOI MOSFETs, NC-SOI MOSFETs with WFV(II) exhibit smaller σIoff and σIoff/μIoff than SOI MOSFETs with LER. NC-SOI MOSFETs without internal metal gate design may suppress the WFV induced variability.

ACKNOWLEDGMENT

The authors are grateful to the National Center for High-Performance Computing in Taiwan for computational facilities and software.

REFERENCES

[1] S. Salahuddin and S. Dattat, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices,” *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008.

[2] V. P.-H. Hu, P.-C. Chiu, A. B. Sachid, and C. Hu, “Negative capacitance enables FinFET and FDSOI scaling to 2 nm node,” in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2017, pp. 23.1.1–23.1.4.

[3] A. I. Khan, C. W. Yeung, C. Hu, and S. Salahuddin, “Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation,” in *Proc. Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2011, pp. 11.3.1–11.3.4.

[4] C. W. Yeung, A. I. Khan, A. Sarker, S. Salahuddin, and C. Hu, "Low power negative capacitance FETs for future quantum-well body technology," in *Proc. Int. Symp. VLSI Technol. Syst. Appl. (VLSI-TSA)*, Hsinchu, Taiwan, 2013, pp. 1–2.

[5] P. Sharma *et al.*, "Impact of total and partial dipole switching on the switching slope of gate-last negative capacitance FETs with ferroelectric hafnium zirconium oxide gate stack," in *Proc. Symp. VLSI Technol.*, Kyoto, Japan, 2017, pp. T154–T155.

[6] M. H. Lee *et al.*, "Physical thickness 1.x nm ferroelectric HfZrOx negative capacitance FETs," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2016, pp. 12.1.1–12.1.4.

[7] Z. Krivokapic *et al.*, "14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2017, pp. 15.1.1–15.1.4.

[8] S. Khandelwal *et al.*, "Circuit performance analysis of negative capacitance FinFETs," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, 2016, pp. 1–2.

[9] Z. C. Yuan *et al.*, "Switching-speed limitations of ferroelectric negative-capacitance FETs," *IEEE Trans. Electron Devices*, vol. 63, no. 10, pp. 4046–4052, Oct. 2016.

[10] X. Li *et al.*, "Enabling energy-efficient nonvolatile computing with negative capacitance FET," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3452–3458, Aug. 2017.

[11] T. Dutta *et al.*, "Performance evaluation of 7-nm node negative capacitance FinFET-based SRAM," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1161–1164, Aug. 2017.

[12] Y. Li, K. Yao, and G. S. Samudra, "Delay and power evaluation of negative capacitance ferroelectric MOSFET based on SPICE model," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2403–2408, May 2017.

[13] M. Kobayashi, N. Ueyama, K. Jang, and T. Hiramoto, "Experimental study on polarization-limited operation speed of negative capacitance FET with ferroelectric HfO2," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2016, pp. 12.3.1–12.3.4.

[14] M. Kobayashi and T. Hiramoto, "Device design guideline for steep slope ferroelectric FET using negative capacitance in sub-0.2V operation: Operation speed, material requirement and energy efficiency," in *Proc. Symp. VLSI Technol. (VLSI Technol.)*, Kyoto, Japan, 2015, pp. T212–T213.

[15] A. I. Khan, U. Radhakrishna, S. Salahuddin, and D. Antoniadis, "Work function engineering for performance improvement in leaky negative capacitance FETs," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1335–1338, Sep. 2017.

[16] A. I. Khan, U. Radhakrishna, K. Chatterjee, S. Salahuddin, and D. A. Antoniadis, "Negative capacitance behavior in a leaky ferroelectric," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4416–4422, Nov. 2016.

[17] H.-P. Lee and P. Su, "Suppressed Fin-LER induced variability in negative capacitance FinFETs," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1492–1495, Oct. 2017.

[18] P.-C. Chiu and V. P.-H. Hu, "Analysis of negative capacitance UTB SOI MOSFETs considering line-edge roughness and work function variation," in *Proc. IEEE Electron Devices Technol. Manuf. (EDTM)*, Kobe, Japan, Feb. 2018, pp. 13–15.

[19] C.-I. Lin, A. I. Khan, S. Salahuddin, and C. Hu, "Effects of the variation of ferroelectric properties on negative capacitance FET characteristics," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 2197–2199, May 2016.

[20] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical insights on negative capacitance transistors in nonhysteresis and hysteresis regimes: MFMIS versus MFIS structures," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 867–873, Mar. 2018.

[21] T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process variations on negative capacitance FinFET devices and circuits," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 147–150, Jan. 2018.

[22] G. Karbasian *et al.*, "Ferroelectricity in HfO_2 thin films as a function of Zr doping," in *Proc. Int. Symp. VLSI Technol. Syst. Appl. (VLSI-TSA)*, Hsinchu, Taiwan, 2017, pp. 1–2.

[23] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254–1260, May 2003.

[24] N. Agrawal, Y. Kimura, R. Arghavani, and S. Datta, "Impact of transistor architecture (bulk planar, trigate on bulk, ultrathin-body planar SOI) and material (silicon or III–V semiconductor) on variation for logic and SRAM applications," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3298–3304, Oct. 2013.

[25] H. F. Dadgour, K. Endo, V. K. De, and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors—Part II: Implications for process, device, and circuit design," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2515–2525, Oct. 2010.

[26] K. Ohmori *et al.*, "Impact of additional factors in threshold voltage variability of metal/high-k gate stacks and its reduction by controlling crystalline structure and grain size in the metal gates," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2008, pp. 1–4.

[27] H.-P. Chen, V. C. Lee, A. Ohoka, J. Xiang, and Y. Taur, "Modeling and design of ferroelectric MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2401–2405, Aug. 2011.

[28] S. Khandelwal, J. P. Duarte, A. I. Khan, S. Salahuddin, and C. Hu, "Impact of parasitic capacitance and ferroelectric parameters on negative capacitance FinFET characteristics," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 142–144, Jan. 2017.

VITA PI-HO HU (S'09–M'13) received the B.S. degree in materials science and engineering and the Ph.D. degree in electronics engineering from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, in 2004 and 2011, respectively.

From 2011 to 2015, she was an Assistant Research Fellow with National Chiao Tung University. She is currently an Assistant Professor with the Department of Electrical Engineering, National Central University, Taoyuan, Taiwan. Her research interests include ferroelectric FET and memory, silicon and IIIV-based nano-electronics, ultra-low power SRAM and logic circuits, and circuit/device interaction.

PIN-CHIEH CHIU (S'16) received the B.S. degree in physics and the M.S. degree in electrical engineering from National Central University, Taoyuan, Taiwan, in 2016 and 2018, respectively. His research interests include advanced CMOS device designs and ferroelectric transistors.

YI-CHUN LU (S'18) is currently pursuing the M.S. degree with the Department of Electrical Engineering, National Central University, Taoyuan, Taiwan. Her research interests include analog performance of ferroelectric FETs and circuits.