Received 17 July 2018; revised 5 October 2018 and 23 November 2018; accepted 22 January 2019. Date of publication 31 January 2019; date of current version 1 March 2019. The review of this paper was arranged by Editor M. K. Radhakrishnan.

Digital Object Identifier 10.1109/JEDS.2019.2895367

Ferroelectric Field Effect Transistors Based on PZT and IGZO

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This work was supported in part by the Romanian Ministry of Research and Innovation and in part by the Executive Unit for Financing Higher Education and Innovation, National Council of Scientific Research (CNCS-UEFISCDI) under Grant PN-II-RU-TE-2014-4-1122 and Grant PN-III-P1-1.1-PD-2016-1546.

ABSTRACT Ferroelectric field effect transistors (FeFETs) based on lead zirconate titanate (PZT) ferroelectric material and amorphous-indium-gallium-zinc oxide (a-IGZO) were developed and characterized. The PZT material was processed by a sol-gel method and then used as ferroelectric gate. The a-IGZO thin films, having the role of channel semiconductor, were deposited by radio-frequency magnetron sputtering, at a temperature of ~50°C. Characteristics of a typical field effect transistor with SiO_2 gate insulator, grown on highly doped silicon, and of the PZT-based FeFET were compared. It was proven that the FeFETs had promising performances in terms of I_{on}/I_{off} ratio (i.e., 10^6) and I_{DS} retention behavior.

INDEX TERMS Ferroelectric transistor, PZT, IGZO.

I. INTRODUCTION

Ferroelectric field effect transistors (FeFET) are highly attractive as non-volatile memories due to characteristics like non-destructive read-out, high-density integration possibility, high speed of reading and writing and low power consumption [1], [2]. CMOS compatible FeFET employing silicon (Si) transistors and Al doped HfO_2 as ferroelectric material were recently reported [3]–[5]. Ferroelectric gate thin film transistors (FeTFT) were developed using different ferroelectrics such as PZT [6]–[10], poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] [11]–[14], $(Bi,La)_4Ti_3O_{12}$ (BLT) [15] or HfO_2-based materials (e.g., Si-doped or Zr-doped HfO_2) [16]–[19]. In terms of architecture, the [P(VDF-TrFE)] based FeTFT devices are generally top-gate, whilst the fully inorganic structures are bottom-gate.

Among the above mentioned ferroelectrics, HfO_2-based materials recently attracted significant attention. Since the breakthrough of Böscke *et al.* [20], which reported in 2011 the ferroelectricity of Si-doped HfO_2, incremental focused researches have been performed in order to asses if HfO_2 based-materials can overcome some of the limitations of conventional ferroelectrics (such as PZT), markedly their (*i*) reduced compatibility with metal-oxide-semiconductor (CMOS) technologies or (*ii*) limited scalability. The ferroelectricity of HfO_2 films manifests when the layer thickness is reduced to few nm (e.g., 10 nm) [16], [21]. However, this could generate an important technological hindrance, since a non-uniformity of only 1 nm will correspond to a thickness variation of 10%, with a negative impact on the overall performance reproducibility. One the other hand, PZT presents ferroelectricity even at film thicknesses of tens or hundreds of nm, and thereby a similar thickness non-uniformity will not induce a deleterious effect of the same magnitude.

A disadvantage shared by all polycrystalline ferroelectrics (HfO_2, PZT included) is the random orientation of the crystalline grains, which will determine a random behavior of the correlation between the polarization and direction of the electric field along the crystalline grains. Moreover, in PZT the binding of cations to oxygen is relatively weak (thus, the oxygen vacancies formed relatively easy) and this can cause reliability concerns. However, PZT, as gate in FETs, is appealing due to its high remnant polarization and low coercive voltages. Moreover, this material can be obtained via solution methods, offering high scalability, while maintaining the good ferroelectric response [22]. Still, a drawback of PZT is the difficulty of integration in the mature Si technology because of the poor quality of

the PZT/Si interface [23]. Nevertheless, this issue can be overcome by combining the ferroelectric PZT with an oxide semiconductor, such as indium-gallium-zinc oxide (IGZO). First suggested by Nomura *et al.* [24], amorphous IGZO (a-IGZO) is already acknowledged as a suitable material for application in transparent transistors, acting as the semiconductor channel. The notoriety of a-IGZO was gained in the last decade due to its relatively large carrier mobility, high transparency and good uniformity on large areas. Consequently, IGZO has been used so far in FeFETs as channel semiconductor in combination with [P(VDF-TrFE)] [11], [12], BLT [15], and bilayer gates, e.g., [P(VDF-TrFE)]/Al_2O_3 [25]–[27].

At an energy band gap of ∼3 eV and a work function of 4.5 eV, IGZO has an unsuitable band alignment with Si- [28] and Zr-doped HfO_2 [29] for FET-type applications. In the case of PZT and un-doped HfO_2, the band alignment is presumed to be favorable (type I-straddled), but with low valence band offset (∼0.4 eV) and low conduction band offset (∼0.2 eV) for PZT. Nevertheless, the band offset may vary as both the band gap and the work function of polycrystalline films are greatly influenced by the synthesis method variables. For example, the IGZO band gap was found to vary in the range 2.5 – 3.5 eV [30], [31].

For the design of FeFETs, PZT has been combined with MoS_2 [6], [7], graphene [8], [32], ITO [9] or ZnO [10]. Graphene, ITO and ZnO are transparent in visible range, whilst MoS_2 has a band gap of ∼1.2 eV. The use of graphene in PZT- FeFETs (memory window of 4.1 – 4.3 eV, ∼ 72% of I_{high}/I_{low} can be retained after 10 years) devices produces good performances, but it cannot substitute IGZO, as it has a p-type conduction. In ZnO the free carriers are generated as consequence of oxygen vacancies (VO), and therefore, the electron concentration and its reproducibility is difficult to be managed. In the case of IGZO, the free carriers density is governed by indium concentration, while the VOs, which are the predominant defects also in type of material, have the highest formation energy in the vicinity of gallium atoms. Thereby, the modification of gallium concentration in IGZO can be used to control the formation of VOs, and consequently, to tune the free carriers density [33]. Although ITO/PZT based FeFETs were considered promising, they are affected by large leakage currents, which can be associated with the unfavorable band alignment (valence offset of −1.1 eV) [34].

To the best of our knowledge, no reports on the fabrication and performance of FeFETs using HfO_2 – doped or un-doped – or PZT (as ferroelectric gate) and a-IGZO (as channel semiconductor), have been published yet. In this article we advance the use of one of these combinations (i.e., PZT and IGZO) for the development of a new ferroelectric transistors.

II. DEVICE FABRICATION AND EXPERIMENTAL METHODS

Two types of bottom-gate field effect transistors (FET) were fabricated: (*i*) with 50 nm thick SiO_2 gate insulator grown on highly doped Si ("SiMat") and (*ii*) with 230 nm thick PZT ($PbZr_{0.2}Ti_{0.8}O_3$) deposited by sol-gel method onto temperature resistant glass substrate. The fabrication steps of the PZT layers are described elsewhere [35]. The 40 nm thick IGZO channel semiconductor was deposited by radio-frequency magnetron sputtering (RF-MS) (using a customized AJA Phase II J system) on both SiO_2 and PZT, at room-temperature (i.e., without intentional heating; the substrate temperature reaching a temperature of ∼50 °C under the deposition conditions, due to plasma bombardment processes only), in the same deposition session. The sputtering of In:Ga:Zn (1:1:2) oxide target was performed in inert atmosphere, using an Ar flow of 20 sccm, and a substrate-to-target separation distance of 80 mm. To ensure good uniformity the substrates were rotated at a speed of 30 rpm. The Ti/Au layers for the gate (only on PZT based transistors) and source-drain electrodes were deposited by RF-MS, subsequently to the patterning of the substrates by photolithography. In both SiO_2 and PZT-based transistor cases, the channel width – length ratio was W/L = 20 μm/20 μm. The as-fabricated transistors and metal-ferroelectric-metal structures – MFM (the schematics given in Figd. 1 (d – f) were thermal-treated in air at 250 °C, on a hot plate in two consecutive sessions of 2 h, under dark conditions. Subsequently, the devices were analyzed.

The structure of the PZT layers was analyzed by X-ray diffraction (XRD) in symmetric geometry, using a Bruker D8 Advance machine (CuK_α radiation). The morphology of the PZT/IGZO based FET was investigated by scanning electron microscopy (SEM), with a Zeiss Merlin Compact field emission scanning electron microscope. The transfer and output characteristics of the FETs were evaluated with a Keithley 4200 semiconductor parameter analyzer, in dark conditions, using 0.5 s per one step of 0.2 V in sweeping V_{GS} and 0.1 V in sweeping V_{DS}. The electrical measurements were performed in normal atmospheric conditions at room-temperature, and in vacuum (at 2×10^{-6} mbar) at various temperatures. Furthermore, the capacitance-voltage (C-V) characteristics of SiO_2/IGZO/Ti/Au and PZT/IGZO/Ti/Au structures were carried out directly on FETs; the C-V curves were recorded at 100 kHz frequency of the a.c. small signal of 100 mV amplitude using a Hioki LCR meter, by sweeping the voltage from negative to positive values and back. The polarization–voltage (P–V) measurements were performed at 100 Hz by employing a TF2000 ferritester system equipped with a FE-Module (aixACCT).

III. RESULTS AND DISCUSSION

The polycrystalline nature of PZT layers structure can be depicted based on Fig. 1 (c). The identified diffraction maxima are ascribed to crystallized PZT [35]. Crystalline coherence length (D_{h00}) and mean square strain values of 73 nm and 0.02, respectively, were determined by the Williamson-Hall method. In addition, the top-view and cross-view SEM analyses revealed that the PZT layer is dense and elicits a clear separation interface with the IGZO thin film (see Fig. 1 (a) and (b)). MFM structures, having areas of

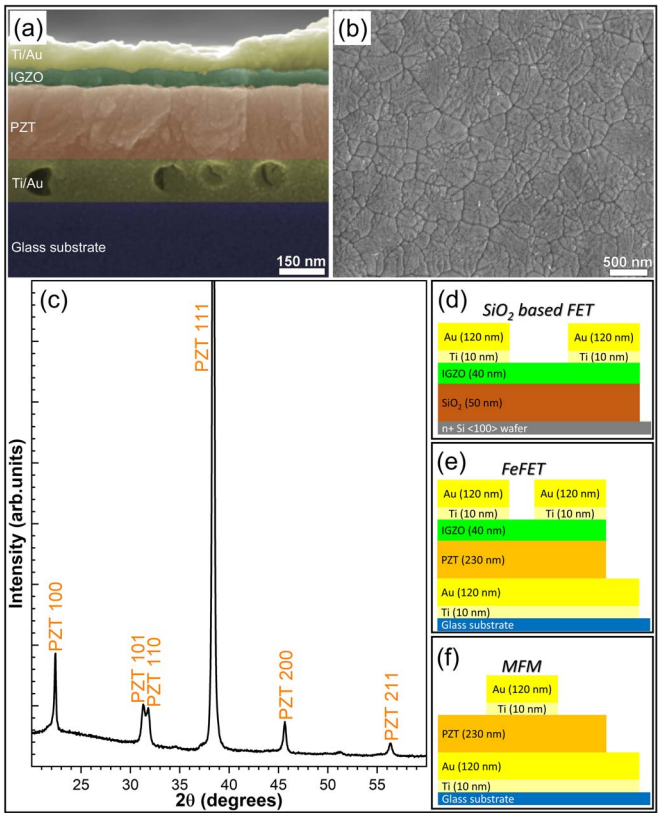

FIGURE 1. **(a) Cross-sectional SEM image of PZT/IGZO based FET; (b) Top-view SEM image of the PZT layer's surface; (c) XRD pattern of the sol-gel synthesized PZT thin film; Schematics of the (d) SiO_2 based FET, (e) PZT based FeFET; and (f) metal-ferroelectric-metal (MFM) structures.**

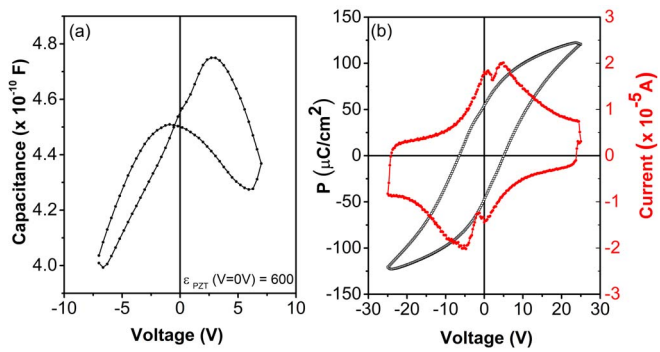

FIGURE 2. **(a) Capacitance-voltage (C-V) characteristics of the PZT based MFM; (b) Hysteresis loop recorded for the PZT film.**

0.0196 mm^2, were fabricated on the same glass wafer as the FET structures, to enable performing the C-V and hysteresis loop measurements.

The C-V characteristics (Fig. 2 (a)) are asymmetric in terms of capacitance values, and moreover, show a small shift towards negative voltages. The asymmetry of the C-V curves can be caused by the different PZT interface formed with the bottom (Ti/Au/PZT) and top (PZT/Ti/Au) electrodes, respectively. Moreover, the bottom electrode was subjected to an annealing temperature of 650 °C after the deposition of the PZT film, and this caused its degradation. The significant impact of the thermal annealing on the bottom electrodes is revealed by the cross-section SEM image (Fig. 1 (a)), which evidenced the presence of voids with diameters up to 100 nm in the Au layer.

TABLE 1. **Performance parameters of FeFETs. This work: electrical properties of SiO_2 and PZT based FETs. In the case of PZT-based FET, the threshold voltage (consequently, μ_{fe}) has two values, corresponding to forward and reverse sweeps. I_{on}(SiO_2 base FET) = 2.6×10^{-6} A, I_{off} (PZT based FET) = 2.1×10^{-6} A; Other works: [P(VDF-TrFE] [25], [36], [37], BLT [15], PZT [9], [32] and HfZrO [18], [19].**

Gate	Channel	I_{on}/I_{off}	V_{th} (V)	SS (V/dec)	μ_{fe} (cm^2/Vsec) (V_{DS} = 0.1 V)
This work					
SiO_2	IGZO	7.6 x 10^2	-2.7	1.35	29
PZT	IGZO	1.5 x 10^6	-1.2/2.6	1.25	1.5/ 3
Other works					
[P(VDF-TrFE]	IGZO	10^5 [36] 10^7 [37]	0.5 [37]	0.4 [37]	1 [37]
[P(VDF-TrFE]/Al_2O_3	IGZO	10^8 [25]	3.1 [25]	0.34 [25]	49.2 [25]
BLT	IGZO	10^4 [15]	-	0.1 [15]	-
PZT	ITO	10^5 [9]	1.5 [9]	-	0.092 [9]
PZT	SLG	6 [32]	-	-	1500 [32]
HfZrO/Al_2O_3	IZO	-	-0.4 [19]	0.82 [19]	5.5 [19]
HfN/HfZrO/SiO_2	p-Si	10^4 [18]	-6/5 [18]	-	-

The hysteresis loops (Fig. 2 (b)) were recorded using a triangular voltage wave with a frequency of 100 Hz. The current hysteresis shows the presence of the characteristic peaks associated to polarization reversal. The value for remnant polarization (Pr) is around 53 $\mu C/cm^2$, while the coercive voltages of −6.5 V and +5.2 V lead to a coercive field of 240 kV/cm. It should be mentioned that the hysteresis loops have a small shift towards negative voltages.

The typical pinch-off of n-type semiconductor FETs was shown by the output characteristics of SiO_2 or PZT based FETs (Fig. 3 (a) and (d)). Both devices showed a good saturation tendency, while the linear regime was recorded for V_{DS} biases lower than 1 V for both devices.

Table 1 summarizes the essential parameters for FET devices ($I_{on} - I_{DS}$ at maximum V_{GS} bias; the I_{on}/I_{off} ratio, where I_{off} and I_{on} are the I_{DS} at minimum and maximum V_{GS} bias, respectively; the threshold voltage – V_{th}; the subthreshold slope – SS; field effect mobility – μ_{fe}). The leakage current, I_{GS}, in the case of SiO_2 based FET was 10^{-10}A, thus, with two orders of magnitude higher with respect to the one of FeFET, degrading the I_{off} level and consequently the I_{on}/I_{off} ratio.

The field effect mobility values were calculated using the equation 1, where oxide capacitance values are

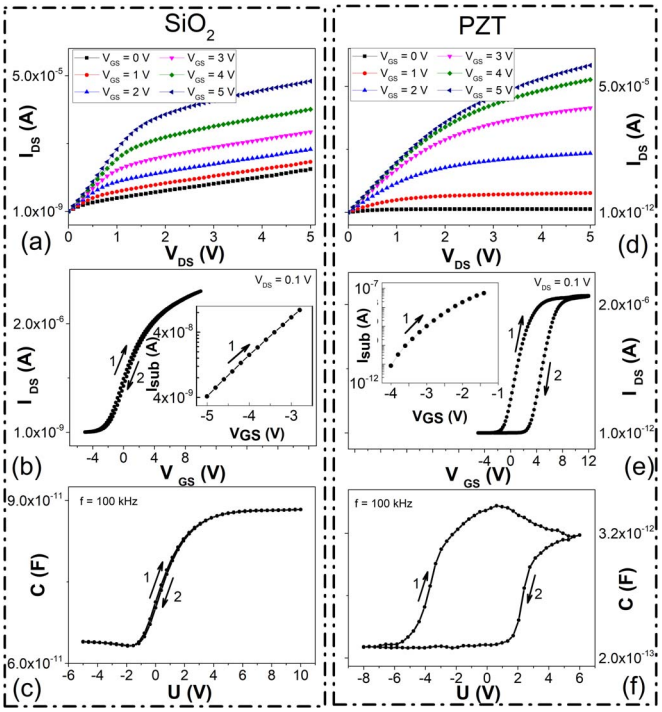

FIGURE 3. **SiO_2/IGZO/Ti/Au structure: (a) Output characteristics; (b) Linear transfer characteristics with inset of sub-threshold region, and (c) C-V curve; PZT/IGZO/Ti/Au structure: (d) Output characteristics; (e) Linear transfer characteristics with inset of sub-threshold region; and (f) C-V curve.**

$C_{ox}(SiO_2) = 6.9 \times 10^{-8}$F/cm and $C_{ox}(PZT) = 2 \times 10^{-6}$F/cm. The obtained μ_{fe} values are underestimated with ~24%, due to the contact resistance effect, $R_c = 29k\Omega$ (extracted using Transmission Line Method [38]).

$$\mu = \frac{L}{W} \frac{I_{DS}}{C_{ox}(V_{GS} - V_{th})V_{DS}} \tag{1}$$

The transfer characteristics (I_{DS} *vs.* V_{GS}) with a double sweep of the V_{GS}, under $V_{DS} = 0.1$V, are presented in Fig. 3 (b) and (e). For SiO_2 based FET, the hysteresis width – defined as the ΔV_{GS} at $(I_{on} - I_{off})/2$ – has a negligible value of 0.2 V. The insignificance of the hysteresis width for this device is confirmed by the C-V measurements (Fig. 3 (c)). However, in the case of PZT based FET, ΔV_{GS} is 3.2 V and the hysteresis width in capacitance – defined as Δ V at $(C_{max} - C_{min})/2$ – is 6.2 V. (Fig. 3 (f)). Both I-V and C-V hysteresis loops show a clock-wise behavior, which is intriguing since, in a proper FeFET, the hysteresis loops have to be counter clock-wise when the ferroelectric is grown on a n-type semiconductor.

Equation (2) [39], [40] was used to estimate (considering the product of the deep bulk states density and the IGZO thickness as much lower-than the interface states density) the maximum the interface states densities, D_{it}, of 1×10^{12} cm^{-2} eV^{-1} for SiO_2/IGZO and 1.3×10^{13} cm^{-2} eV^{-1} for PZT/IGZO structures. This interface quality difference is reflected also in the sub-threshold performance of the TFTs (inset – Fig. 3 (b) and (e)), i.e., the higher sub-threshold current for SiO_2-TFT.

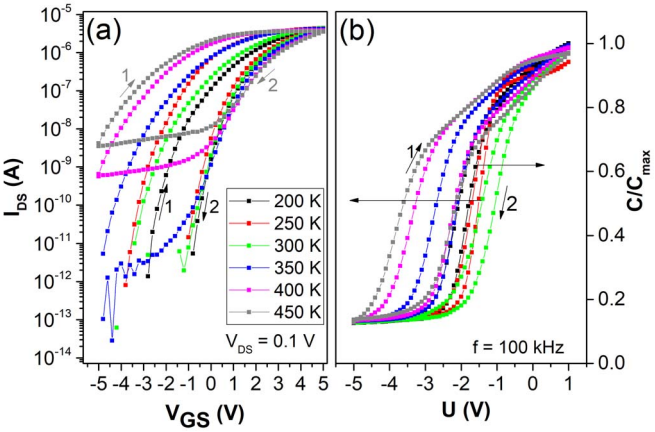

FIGURE 4. **PZT FeFET structure: (a) Linear transfer characteristics; (b) (C-V) characteristics measured at different temperatures.**

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{qSS}{kT\ ln10} - 1 - \frac{C_D}{C_{ox}}\right) \tag{2}$$

where $C_D \sim 10^{-7}$ F/cm is depletion capacitance.

Considering the IGZO thickness of 40 nm and its electron concentration of 6×10^{17} cm^{-3} (extracted from Hall measurements, data not shown here), it results that the free carriers from the channel can compensate a polarization of maximum 0.4 μC/cm^2. This is a much smaller value than the one extracted from the hysteresis loop presented in Fig. 2 (b). On the other hand, the D_{it} extracted for the PZT/IGZO interface corresponds to about 6 μC/cm^2.

The result is that the hysteresis loops at room-temperature are dominated by the interface traps. PZT-based FeFETs with clock-wise loops are not unprecedented [6], [7]. The observed hysteresis loops were described by the dynamic charge trapping and de-trapping which take places when V_{GS} is swept from negative to positive, and back. Nevertheless, even in the case of a clock-wise hysteresis, the field effect can be modulated by changing the polarization value in the ferroelectric gate, as shown in Sun *et al.* [6].

We have also performed temperature-dependent hysteresis measurements on the PZT/IGZO FeFET (Fig. 4). One can see that, up to 420 K, the counter clock-wise hysteresis could not be recovered. A possible explanation for this is that the capacitance measurement was performed between the gate and source/drain electrodes, thus the results are affected by some parasitic capacitances (e.g., overlap capacitance between the gate electrode and the source/drain electrodes with only PZT in between).

It is shown that the hysteresis width (memory window) increases with temperature. This effect can be attributed to the presence of ferroelectric polarization in the gate layer. As the temperature increases the trapping on the interface states is no longer active, and thus the effect of ferroelectric polarization is more visible in the device characteristics. Moreover, a peculiar behavior was revealed by the C-V *vs.*

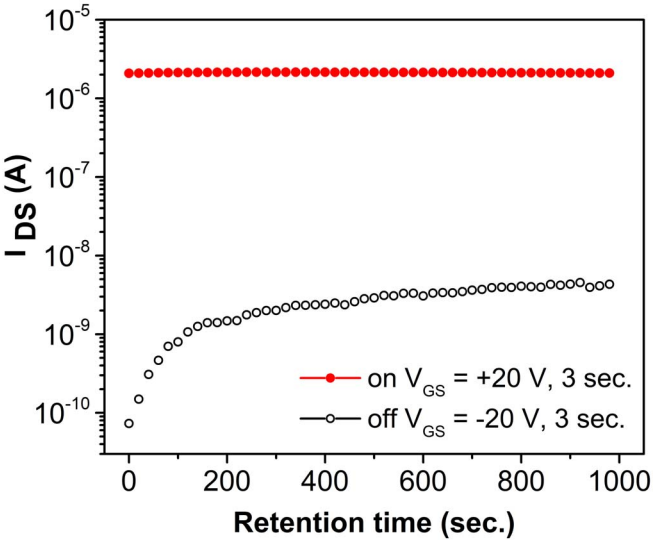

FIGURE 5. Retention behavior of the PZT-IGZO based FeFET; Variation of the "On" and "Off" states with a time lapse of 1000 seconds.

temperature measurements: from 200 K to 250 K, the C-V curve has a positive shift, while, from 250 K to 420 K, the C-V curves show a shift towards negative voltage. Up to 250 K, the positive shift could be caused by the trapping of electrons by the existing defects at the given top electrode (with activation energy larger than 21.4 meV), which partially screens the applied gate bias and makes the effective gate voltage smaller. As the temperature is further increased, the curves are shifted toward negative V_{GS} values due to the carriers thermal activation (electron detrapping) from trapping states.

The memory function (as non-volatile memory) was tested by applying a voltage pulse of +20 V or − 20 V for 3 seconds on the gate electrode, orienting in this way the polarization upward (towards the IGZO channel) or downward (towards the gate electrode), and then measuring the drain current at regular time intervals with no potential applied on the gate (floating gate).

Two I_{DS} values were obtained, for On and Off states (Fig. 5), corresponding to the two orientations of the polarization. Thus, the memory function is present although the ferroelectric hysteresis is masked by the parasitic effect of the interface states. The memory property can be explained by the fact that, after removing the external poling field applied on the gate, the polarization value and orientation stabilizes to the value allowed by the available charges for compensating the depolarization field. The values/orientations appear to be different leading to different values of the drain current. We can speculate that the upward value (for positive gate voltage) is very stable (induces accumulation in the channel), leading to an almost constant value of the drain current up to 1000 seconds. The opposite orientation of polarization seems to stabilize after about 100 seconds, as suggested by the fact that the drain current value increases from few tens of picoamps to few nanoamps. This is owned to the fact that during the poling period and immediately after removing the poling field, the polarization value is close to the one extracted from the hysteresis loop (about 50 $\mu C/cm^2$). After removing the poling field, the polarization value decreases, probably around 0.4 $\mu C/cm^2$ or less, leading to an increase drain current value. One can observe that the increase in the value of the drain current is about the same order of magnitude with the assumed decrease in polarization value after removing the poling field.

There is an apparent inconsistency between the clockwise hysteresis (Fig. 3e) and the presence of I_{DS} retention (Fig. 5). The question of how both behaviors can characterize the same FeFET can arise. We believe that this may be a result of the measurement procedure. The current-voltage characteristic in Fig. 3e is a dynamic one (V_{GS} sweeping); in this case, both voltages are applied on the structure, V_{GS} and V_{DS}.

The retention measurement results, presented in Fig. 5, were obtained after the gate probe was mechanically lifted (open gate); in this case only V_{DS} is applied on the structure. The fact that there is a certain superposition between the gate electrode on one hand and the source/drain electrodes on the other hand, may lead to different behavior of charges in the structure when both V_{GS} and V_{DS} are applied, compared to the situation when only V_{DS} is applied and the gate is not grounded.

When a positive voltage is applied on the gate, then polarization will be oriented towards the IGZO channel, attracting electrons to the interface for compensating the positive polarization charges. Some of these electrons are trapped on the interface states. When the applied V_{GS} is higher than +9 V (Fig. 3e), the device is not completely trapped. Therefore, applying a V_{GS} bias of +20 V before measuring the I_{DS} retention time is enough for obtaining the maximum accumulation current, ~2 microamps, the same as the one measured in Fig. 3e. Moreover, because the gate contact is open, there are no parasitic conduction channels for the charges in the structure and the drain current remains at the value set after poling the ferroelectric with positive V_{GS}.

The functionality of here presented FeFET device is inferior to those based on [P(VDF-TrFE)] and IGZO, which show field effect mobility higher than 40 cm^2/Vs, I_{on}/I_{off} of 10^8 and retention time of days [25]. However, contrary to PZT, P(VDF-TrFE) suffers of permanent degradation of its ferroelectric properties when is exposed to temperatures higher that 65 °C, being unsuitable for high temperature applications.

IV. CONCLUSION

Thin PZT layers were obtained by sol-gel, a low-cost fabrication method, and successfully integrated into FeFETs. The device provided good performances in terms of both I_{on}/I_{off} ratio and threshold voltage. However, the interface states between PZT and IGZO acted as traps and affected the ferroelectric memory window. In spite of this, good retention

behavior was shown due to the polarization switching in the gate ferroelectric.

Therefore, PZT/IGZO based FeFETs could become interesting alternatives, even for transparent electronics, if the contribution of interface states acting as traps will be reduced (ideally, completely removed). This could be the solution to recover the ferroelectric memory window and to manufacture an accurate FeFET that may compete with the existing non-volatile memories based on trap charges or floating gate. One possible route to optimize the interface quality is to use a textured or even epitaxial ferroelectric layer instead of a polycrystalline one. However, such an approach, based on ferroelectric layers of higher structural quality would imply the use expensive deposition technologies (i.e., PVD or CVD) and would introduce certain restrictions in what concerns the substrate choices.

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