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# Investigation of Nitrous Oxide Nitridation Temperatures on P-Type Pi-Gate Poly-Si Junctionless Accumulation Mode TFTs

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**ABSTRACT** In this paper, the influence of nitrous oxide ($N_2O$) nitridation temperatures on p-type Pi-gate (PG) poly-Si junctionless accumulation mode (JAM) TFTs is experimentally investigated. The tetraethoxysilane (TEOS) gate oxide quality for PG JAM TFTs can be significantly improved by increasing $N_2O$ nitridation temperatures ($T_N$) from 700 °C to 800 °C in $N_2O$ ambient, resulting in the improvement of average subthreshold swing (A.S.S.), increase of on current ($I_{ON}$), and enhancement of TEOS gate oxide breakdown $E$-field ($E_{OBD}$). PG JAM TFTs by means of a proper channel doping concentration ($N_{ch} = 5 \times 10^{18}$ cm$^{-3}$) and a suitable $T_N$ (800 °C) exhibit a steep A.S.S. ~96 mV/dec. and a large $E_{OBD}$~12.1 MV/cm.

**INDEX TERMS** 3-D integrated circuits (ICs), reverse boron penetration, nitrous oxide ($N_2O$), Pi-gate (PG), poly-Si, junctionless accumulation mode (JAM).

## I. INTRODUCTION

Polycrystalline silicon thin-film transistor (poly-Si TFT) is one kind of field-effect transistors. Poly-Si TFTs have been widely investigated and used in large-area flat panel displays with integrated peripheral circuits as the pixel array, such as active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light-emitting displays (AMOLEDs) [1]–[4]. Moreover, poly-Si TFTs are very suitable for three-dimensional integrated circuit (3-D IC) applications and 3-D NAND flash memory applications owing to those advantages associated with low cost, low thermal budget, simple fabrication, high sequential stacked ability, and CMOS-compatible process [5]–[7].

Before the 0.25 $\mu$m technology node, both n-MOSFETs and p-MOSFETs with the same *in situ* $n^+$ doped poly-Si gates require p-type channel doping regions to acquire a suitable threshold voltage ($V_{TH}$) for very large scale integration (VLSI) applications [8]. Based on the use of $n^+$ poly-Si gates, p-MOSFETs are more susceptible to short-channel effects (SCEs) due to the use of p-type channel doping regions for $V_{TH}$ adjustment [8]–[10]. Such devices are designated as buried-channel MOSFETs (BC-MOSFETs). To enhance SCE immunity as well as attain low and symmetric $V_{TH}$, $n^+$ poly-Si gates and p-type channel doping regions for n-MOSFETs as well as $p^+$ poly-Si gates and n-type channel doping regions for p-MOSFETs in the 0.25 $\mu$m technology node are utilized to form surface-channel MOSFETs (SC-MOSFETs) in submicron CMOS devices [11]–[13]. However, boron atoms used to dope the undoped poly-Si gates can rapidly diffuse through the thin gate oxide from the $p^+$ poly-Si gate into the underlying n-type channel region during a high thermal-budget process, namely, boron penetration. This causes a positive shift in flat-band voltage ($V_{FB}$), a positive shift in $V_{TH}$, a degraded subthreshold swing (S.S.), and a degraded $Si/SiO_2$ interface [11]–[18].

In literature, numerous approaches have been proposed and demonstrated to relieve boron penetration. There are two common methods. The first method is to establish diffusion barrier layers at interfaces of poly-Si gates/gate oxides and/or of gate oxides/n-type channel doping regions. This can be accomplished by nitrogen (N) ion implantations

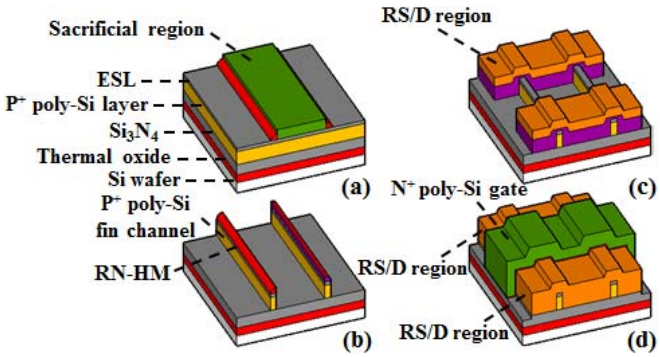


**FIGURE 1.** (a)–(d) Schematic 3-D configurations of a PG JAM TFT for the key fabrication steps.

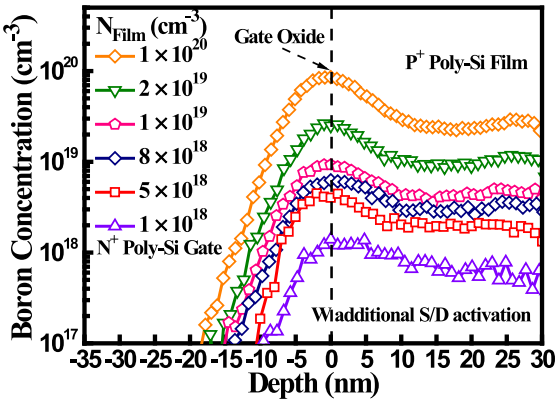


**FIGURE 2.** SIMS depth profiles of the un-patterned $p^+$ poly-Si films with different film doping concentrations after the gate stack formation.

into poly-Si gates and nitridations for poly-Si gates and/or gate oxides by using nitrous oxide ($N_2O$), nitric oxide (NO), or ammonia ($NH_3$). Alternatively, inductive-coupling-nitrogen plasma (ICNP) treatments can be used to incorporate nitrogen-rich layers at interfaces of poly-Si gates/gate oxides and/or of gate oxides/n-type channel doping regions [18]–[23]. The second method is to retard vertical diffusion of boron atoms in gate stack structures. This can be realized by using as-deposited $\alpha$-Si gates instead of poly-Si gates and stacked (or modified) gate structures with $\alpha$-Si and poly-Si layers [16], [24]–[26].

Current p-type junctionless (JL) and junctionless accumulation mode (JAM) transistors need ultra-shallow channel doping regions by using boron difluoride ($BF_2$) ion implantations in order to effectively deplete the conducted carriers in the OFF-state. However, boron diffusion can further aggravate as a result of the presence of fluorine (F) atoms from $BF_2$ ion implantations with F atoms [11]–[13]. This indicates that reverse boron penetration will become more severe in p-type JL and JAM transistors. As a result, in this study, we will explore the influence of channel doping concentrations ($N_{ch}$) and $N_2O$ nitridation temperatures ($T_N$) on p-type PG JAM TFTs to further evaluate the optimum $N_{ch}$ and $T_N$. Furthermore, we will clarify the major impact factors that affect the threshold voltage, the average subthreshold swing (A.S.S.), the on current ($I_{ON}$), the S/D series resistance ($R_{SD}$), and the tetraethoxysilane (TEOS) gate oxide breakdown *E*-field ($E_{OBD}$).

## II. DEVICE FABRICATION

The schematic 3-D configurations of a PG JAM TFT for the key fabrication steps are shown in Fig. 1(a)–(d). The detailed fabrication steps for the PG JAM TFTs were reported in our previous work [27]. First of all, the 150-nm-thick silicon nitride ($Si_3N_4$) layer was deposited on the thermal oxide with a film thickness of 500 nm grown on a Si wafer. Subsequently, the 40-nm-thick undoped amorphous-Si (a-Si) layer was deposited and then crystallized during the solid-phase crystallization (SPC) process. Next, the undoped poly-Si layer was implanted with 18-keV boron difluoride ions ($BF_2^+$) to a dose of $2 \times 10^{13}$ $cm^{-2}$. After the dopant activation, an etching stopping layer (ESL) with a film thickness of 11 nm and a sacrificial layer with a film thickness of 50 nm were sequentially deposited. Following the patterning of the sacrificial regions, the TEOS oxide with a film thickness of 50 nm was deposited and then etched to form the oxide-spacer hard masks (O-SPHMs) [Fig. 1(a)]. After the removal of the sacrificial regions, the O-SPHMs as the first hard masks were utilized to define the rectangular silicon nitride-hard masks (RN-HMs). A 100-nm-thick undoped a-Si layer was deposited and then implanted with the boron ions ($B^+$) to a dose of $2 \times 10^{15}$ $cm^{-2}$ after the $p^+$ poly-Si fin channel formation [Fig. 1(b)]. Using the RN-HMs as the second hard masks, the twin $p^+$ poly-Si fin channels and the raised source/drain (RS/D) regions were simultaneously patterned by means of an anisotropic dry etching process [Fig. 1(c)]. After the RN-HM strip, the gate stack formation consists of the TEOS oxide with a film thickness of 5 nm and the $n^+$ poly-Si gate with a film thickness of 200 nm. During the gate stack formations, the TEOS gate oxides were nitridized at different $N_2O$ nitridation temperatures ($T_N$ = 700 °C, 750 °C, 800 °C, and 850 °C) in $N_2O$ ambient. The gate formation was accomplished to complete the p-type PG JAM TFTs [Fig. 1(d)]. The channel thickness ($T_{ch}$) × the channel width ($W_{ch}$) for the $p^+$ poly-Si fin channel is 36.0 nm × 26.7 nm for p-type PG JAM TFTs [27].

## III. RESULTS AND DISCUSSION

Fig. 2 illustrates the secondary ion mass spectroscopy (SIMS) depth profiles of the un-patterned $p^+$ poly-Si films with different film doping concentrations after the gate stack formation. The film doping concentration ($N_{film}$) values for the un-patterned $p^+$ poly-Si films are, respectively, $1 \times 10^{20}$ $cm^{-3}$, $2 \times 10^{19}$ $cm^{-3}$, $1 \times 10^{19}$ $cm^{-3}$, $8 \times 10^{18}$ $cm^{-3}$, $5 \times 10^{18}$ $cm^{-3}$, and $1 \times 10^{18}$ $cm^{-3}$. It is noteworthy that more boron atoms can penetrate through the TEOS gate oxide from the $p^+$ poly-Si film toward the *in situ* $n^+$ doped poly-Si gate with an increase in $N_{film}$, namely, channel doping concentration-induced reverse boron penetration. This implies that more

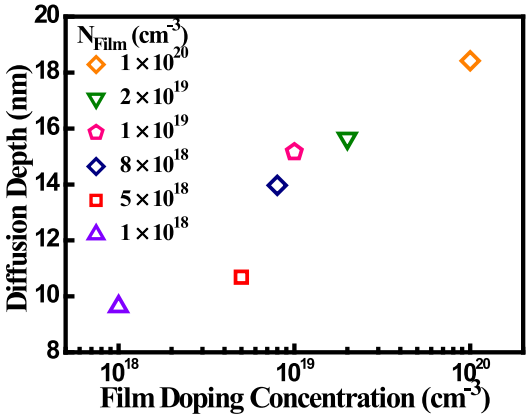


**FIGURE 3.** Diffusion depth of boron atoms versus $N_{film}$ in the *in situ* $n^+$ doped poly-Si gate.

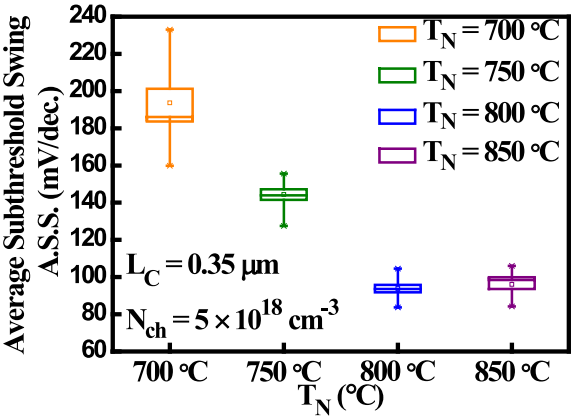


**FIGURE 5.** Statistical distributions of A.S.S. for the PG JAM TFTs with different $T_N$ values.

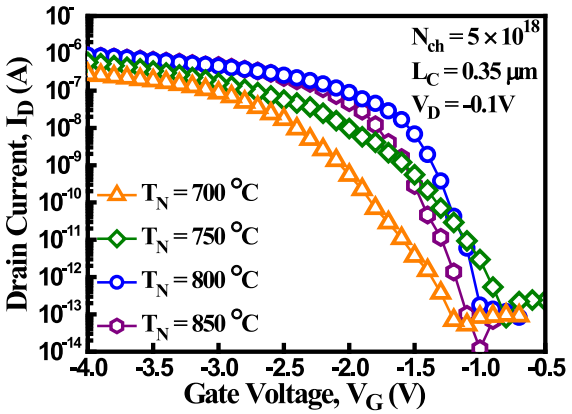


**FIGURE 4.** Comparison of the transfer characteristics of PG JAM TFTs with different $T_N$ values.

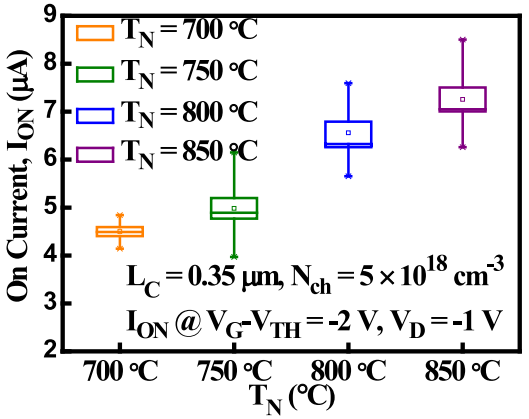


**FIGURE 6.** Statistical distributions of $I_{ON}$ for the PG JAM TFTs with different $T_N$ values.

boron atoms can stay at the TEOS gate oxide with the increase of $N_{film}$. In addition, the diffusion depth of boron atoms in the *in situ* $n^+$ doped poly-Si gate becomes long with an increase in $N_{film}$, as shown in Fig. 3. According to the above-mentioned SIMS depth profiles, the PG JAM TFTs with a higher $N_{ch}$ will undergo more severe channel doping concentration-induced reverse boron penetration. Based on an evaluation between device performance and channel doping concentration-induced reverse boron penetration, an $N_{ch}$ of $5 \times 10^{18}$ $cm^{-3}$ is suitable for PG JAM TFTs [27].

Fig. 4 displays the transfer characteristics of PG JAM TFTs with different $T_N$ values. $V_{TH}$ values are defined by a constant current of $5 \times 10^{-9}$ A. With increasing $T_N$ from 700 °C to 800 °C in $N_2O$ ambient, the positive shift in $V_{TH}$ for PG JAM TFTs might be largely attributed to two causes. One is the enhancement of gate oxide interface quality since the deposition temperature for the TEOS gate oxides was 700 °C. The other is the effective suppression of reverse boron penetration by $N_2O$ treatments [20], [22]. In PG JAM TFTs, the negative shift in $V_{TH}$ could result from the further generation of positive fixed oxide charge with an increase in $T_N$ from 800 °C to 850 °C in $N_2O$ ambient [28]–[33].

Fig. 5 shows the statistical distributions of A.S.S. for PG JAM TFTs with different $T_N$ values. Degradation of A.S.S. for PG JAM TFTs can be attributed to the reduction of gate oxide interface quality and the aggravation of reverse boron penetration [11]–[13], [27]. With increasing $T_N$ from 700 °C to 800 °C in $N_2O$ ambient, the obvious improvement in A.S.S. suggests that the enhancement of gate oxide interface quality is the major impact factor, which is consistent with the above-mentioned analyses and explanations for $V_{TH}$. Furthermore, PG JAM TFTs have a similar A.S.S. as the TEOS gate oxides are nitridized at a $T_N$ of 800 °C and a $T_N$ of 850 °C in $N_2O$ ambient. This indicates that both PG JAM TFTs have a similar interface state density.

Fig. 6 exhibits the statistical distributions of $I_{ON}$ for PG JAM TFTs with different $T_N$ values. PG JAM TFTs utilizing a $T_N$ of 850 °C in $N_2O$ ambient show the highest $I_{ON}$. There are two causes that are associated with the increase of $I_{ON}$ for PG JAM TFTs. One is the decrease in coulomb scattering due to the enhancement of gate oxide interface quality. This can be proved through the obvious improvement for A.S.S., as presented in Fig. 5. The other is the decrease in $R_{SD}$ with an increase in $T_N$. So as to further understand and analyze

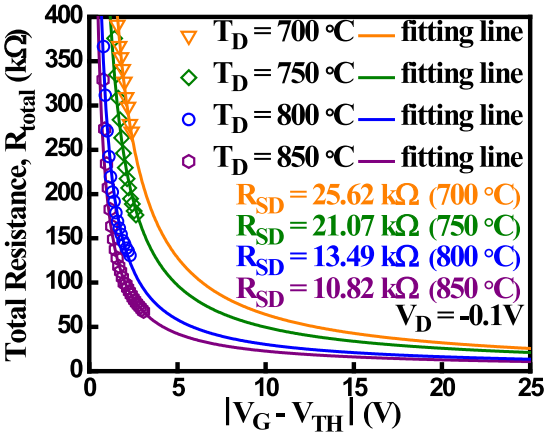


**FIGURE 7.** Extracted $R_{total}$ as a function of $V_G$ for the PG JAM TFTs with different $T_N$ values.

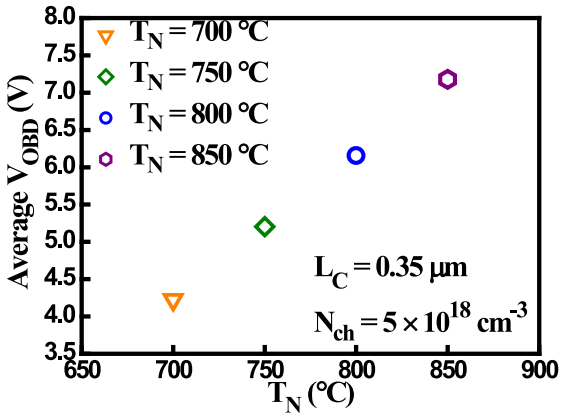


**FIGURE 8.** Extracted average $V_{OBD}$ versus $T_N$ for the PG JAM TFTs with different $T_N$ values.

the impact of $R_{SD}$ on $I_{ON}$ for PG JAM TFTs with different $T_N$ values, $R_{SD}$ is derived from $R_{total} = R_{SD} + (L_G)/[W_{eff} \times \mu_{eff} \times C_{ox} \times (V_G - V_{TH})]$ at $V_{DS} = -0.1$ V [34], where $R_{total}$ is the total resistance, $W_{eff}$ is the effective channel width, $\mu_{eff}$ is the effective mobility, and $C_{ox}$ is the gate oxide capacitance. The second term on the right-hand side of the equation can be ignored as $V_G - V_{TH}$ is close to infinity, i.e., $R_{total}$ is equal to $R_{SD}$. Fig. 7 compares the extracted $R_{total}$ as a function of $V_G$ for PG JAM TFTs with different $T_N$ values. The extrapolated $R_{SD}$ for PG JAM TFTs are, respectively, 25.62 kΩ, 21.07 kΩ, 13.49 kΩ, and 10.82 kΩ at $V_G - V_{TH} = -25$ V with the increase of $T_N$ from 700 °C to 850 °C in $N_2O$ ambient. Using a $T_N$ of 850 °C in $N_2O$ ambient, PG JAM TFTs exhibit the lowest extrapolated $R_{SD}$, which is consistent with the previous result shown in Fig. 6.

Fig. 8 displays the extracted average TEOS gate oxide breakdown voltage ($V_{OBD}$) versus $T_N$ for PG JAM TFTs with different $T_N$ values. It is worth noting that the extracted average $V_{OBD}$ increase with an increase in $T_N$. To further check the TEOS gate oxide quality for the TEOS gate oxides with different $T_N$ values, $E_{OBD}$ is extracted by $(V_{OBD} - V_{TH})/T_{ox}$. Here, $T_{ox}$ is the TEOS gate oxide thickness. The

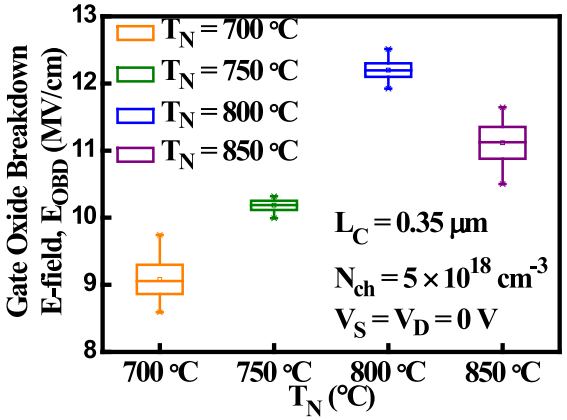


**FIGURE 9.** Statistical distributions of $E_{OBD}$ for the PG JAM TFTs with different $T_N$ values.

statistical distributions of $E_{OBD}$ for PG JAM TFTs with different $T_N$ values are presented in Fig. 9. Utilizing a $T_N$ of 800 °C in $N_2O$ ambient, PG JAM TFTs can achieve the largest $E_{OBD}$ owing to these devices with the best TEOS gate oxide quality [17], [18]. This is consistent with the previous result shown in Fig. 8.

## IV. CONCLUSION

In this paper, the influence of $N_2O$ nitridation temperatures on the electrical characteristics of p-type PG JAM TFTs was experimentally investigated by $N_2O$ treatments. For the first time, it was found that more boron atoms can penetrate through the gate oxide from the $p^+$ fin channel toward the $n^+$ poly-Si gate with an increase in $N_{ch}$. By increasing $T_N$ from 700 °C to 800 °C in $N_2O$ ambient, the TEOS gate oxide quality can be obviously improved, leading to an improvement of A.S.S., an increase of $I_{ON}$, and an enhancement of $E_{OBD}$. By means of a proper $N_{ch}$ ($5 \times 10^{18}$ $cm^{-3}$) and a suitable $T_N$ (800 °C), PG JAM TFTs can exhibit the steepest A.S.S. and the largest $E_{OBD}$.

## REFERENCES

[1] T.-J. King, "Trends in polycrystalline-silicon thin-film transistor technologies for AMLCDs," in *Proc. 2nd Int. Workshop Active Matrix Liq. Cryst. Displays*, 1995, pp. 80–86.
[2] S. Zhang, C. Zhu, J. K. O. Sin, J. N. Li, and P. K. T. Mok, "Ultrathin elevated channel poly-Si TFT technology for fully-integrated AMLCD system on glass," *IEEE Electron Device Lett.*, vol. 47, no. 3, pp. 569–575, Mar. 2000.
[3] R. M. A. Dawson *et al.*, "The impact of the transient response of organic light emitting diodes on the design of active matrix OLED displays," in *IEEE IEDM Tech. Dig.*, Dec. 1998, pp. 875–878.
[4] J.-C. Goh, H.-J. Chung, J. Jang, and C.-H. Han, "A new pixel circuit for active matrix organic light emitting diodes," *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 544–546, Sep. 2002.
[5] Y.-H. Lu, P.-Y. Kuo, Y.-H. Wu, Y.-H. Chen, and T.-S. Chao, "Novel GAA raised source/drain sub-10-nm poly-Si NW channel TFTs with self-aligned corked gate structure for 3-D IC applications," in *VLSI Symp. Tech. Dig.*, Jun. 2011, pp. 142–143.
[6] Y.-H. Lu *et al.*, "High-performance poly-Si thin-film transistors with L-Fin channels," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 215–217, Feb. 2012.
[7] E.-K. Lai *et al.*, "A highly stackable thin-film transistor (TFT) NAND-type flash memory," in *VLSI Symp. Tech. Dig.*, Jun. 2006, pp. 46–47.

[8] G. J. Hu and R. H. Bruce, "Design tradeoffs between surface and buried-channel FET's," *IEEE Trans. Electron Devices*, vol. ED-32, no. 3, pp. 584–588, Mar. 1985.
[9] M. R. Wordeman, "Characterization of depletion mode MOSFET's," in *IEEE IEDM Tech. Dig.*, Dec. 1979, pp. 26–29.
[10] K. Tanaka and M. Fukuma, "Design methodology for deep submicron CMOS," in *IEEE IEDM Tech. Dig.*, Dec. 1987, pp. 628–631.
[11] F. K. Baker *et al.*, "The influence of fluorine on threshold voltage instabilities in $p^+$ polysilicon gated p-channel MOSFETs," in *IEEE IEDM Tech. Dig.*, Dec. 1989, pp. 443–446.
[12] J. M. Sung *et al.*, "Fluorine effect on boron diffusion of $p^+$ gate devices," in *IEEE IEDM Tech. Dig.*, Dec. 1989, pp. 447–450.
[13] H.-H. Tseng *et al.*, "The effect of silicon gate microstructure and gate oxide process on threshold voltage instabilities in $BF_2$ implanted $p^+$ gate p-channel MOSFETs" in *VLSI Symp. Tech. Dig.*, Jun. 1990, pp. 111–112.
[14] G. Q. Lo, D. L. Kwong, and S. Lee, "Anomalous capacitance-voltage characteristics of $BF_2$-implanted and rapid thermal annealed $p^+$-polycrystalline silicon gate metal-oxide-semiconductor structures," *Appl. Phys. Lett.*, vol. 57, no. 24, pp. 2573–2575, Dec. 1990.
[15] A. B. Joshi, J. Ahn, and D. L. Kwong, "Oxynitride gate dielectrics for $p^+$-polysilicon gate MOS devices," *IEEE Electron Device Lett.*, vol. 14, no. 12, pp. 560–562, Dec. 1993.
[16] S.-L. Wu, C.-L. Lee, T.-F. Lei, J.-F. Chen, and L.-J. Chen, "Suppression of the boron penetration induced $Si/SiO_2$ interface degradation by using a stacked-amorphous-silicon film as the gate structure for pMOSFET," *IEEE Electron Device Lett.*, vol. 15, no. 5, pp. 160–162, May 1994.
[17] Y.-H. Lin, C.-L. Lee, T.-F. Lei, and T.-S. Chao, "Thin polyoxide on the top of poly-Si gate to suppress boron penetration for PMOS," *IEEE Electron Device Lett.*, vol. 16, no. 5, pp. 164–165, May 1995.
[18] Y.-H. Lin, C.-S. Lai, C.-L. Lee, T.-F. Lei, and T.-S. Chao, "Nitridization of the stacked poly-Si gate to suppress the boron penetration in PMOS," *IEEE Trans. Electron Devices*, vol. 43, no. 7, pp. 1161–1165, Jul. 1996.
[19] T. Kuroi *et al.*, "The effects of nitrogen implantation into $p^+$ polysilicon gate on gate oxide properties," in *VLSI Symp. Tech. Dig.*, Jun. 1994, pp. 107–108.
[20] A. Uchiyama, H. Fukuda, T. Hayashi, T. Iwabuchi, and S. Ohno, "High performance dual-gate sub-halfmicron CMOSFETs with 6 nm-thick nitride $SiO_2$ films in an $N_2O$ ambient," in *IEEE IEDM Tech. Dig.*, Dec. 1990, pp. 443–446.
[21] L. K. Han, D. Wristers, J. Yan, M. Bhat, and D. L. Kwong, "Highly suppressed boron penetration in NO-nitrided $SiO_2$ for $p^+$-polysilicon gated MOS device application," *IEEE Electron Device Lett.*, vol. 16, no. 7, pp. 319–321, Jul. 1995.
[22] K. S. Krisch *et al.*, "Impact of boron diffusion through $O_2$ and $N_2O$ gate dielectrics on the process margin of dual-poly low power CMOS," in *IEEE IEDM Tech. Dig.*, Dec. 1994, pp. 325–328.
[23] H.-C. Cheng *et al.*, "Suppression of boron penetration for $p^+$ stacked poly-Si gates by using inductively coupled $N_2$ plasma treatment," *IEEE Electron Device Lett.*, vol. 20, no. 10, pp. 535–537, Oct. 1999.
[24] C.-Y. Lin *et al.*, "A comprehensive study of suppression of boron penetration by amorphous-Si gate in $p^+$-gate PMOS devices," *IEEE Trans. Electron Devices*, vol. 42, no. 12, pp. 2080–2088, Dec. 1995.
[25] S.-L. Wu, C.-L. Lee, and T.-F. Lei, "Suppression of boron penetration into an ultra-thin gate oxide ($\leq$ 7 nm) by using a stacked-amorphous-silicon (SAS) film," in *IEEE IEDM Tech. Dig.*, Dec. 1993, pp. 329–332.
[26] C.-Y. Lin, C.-Y. Chang, and C. C.-H. Hsu, "Suppression of boron penetration in $BF_2$-implanted p-type gate MOSFET by trapping of fluorines in amorphous gate," *IEEE Trans. Electron Devices*, vol. 42, no. 8, pp. 1503–1509, Aug. 1995.
[27] D.-R. Hsieh, Y.-D. Chan, P.-Y. Kuo, and T.-S. Chao, "Investigation of channel doping concentration and reverse boron penetration on p-type Pi-gate poly-Si junctionless accumulation mode FETs," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 314–319, Mar. 2018.
[28] B. Yu, D.-H. Ju, N. Kepler, and C. Hu, "Impact of nitrogen ($N_{14}$) implantation into polysilicon gate on high-performance dual-gate CMOS transistors," *IEEE Electron Device Lett.*, vol. 18, no. 7, pp. 312–314, Jul. 1997.
[29] W. Yang, R. Jayaraman, and C. G. Sodini, "Optimization of low-pressure nitridation/reoxidation of $SiO_2$ for scaled MOS devices," *IEEE Trans. Electron Devices*, vol. 35, no. 7, pp. 935–944, Jul. 1988.
[30] H. C. Cheng, J. K. Her, and C. Y. Wu, "Influences of atmospheric-pressure reoxidation on the ultrathin oxide films nitrided in atmospheric $NH_3$ ambient," *J. Electrochem. Soc.*, vol. 137, no. 9, pp. 2816–2819, Sep. 1990.
[31] L. V. Munukutla, B. Morady, J. N. Fordemwalt, and M. R. Moore, "Correlation between interface nitrogen and the fixed charge in thermally nitrided silicon dioxide on silicon," *J. Appl. Phys.*, vol. 68, no. 9, pp. 4662–4666, Nov. 1990.
[32] A. Philipossian and D. B. Jackson, "Determining the charge properties of reoxidized, lightly nitrided oxides using surface charge analysis," *J. Electrochem. Soc.*, vol. 140, no. 4, pp. L68–L71, Apr. 1993.
[33] Y. Suizu, "Reexamination of the role of nitrogen in oxynitrides-fixed charge reduction in the $p^+$-polysilicon gate MOS," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2777–2784, Dec. 2001.
[34] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006, p. 208.

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