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Hybrid Systems-in-Foil—Combining the Merits of Thin Chips and of Large-Area Electronics

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ABSTRACT This paper reports on the status of a comprehensive ten-year research and development effort toward hybrid system-in-foil (HySiF). In HySiF, the merits of high-performance integrated circuits on ultra-thin chips and of large-area and discrete electronic component implementation are combined in a complementary fashion in and on a flexible carrier substrate. HySiF paves the way to entirely new applications of electronic products where form factor, form adaptivity and form flexibility are key enablers. In this review paper the various aspects of thin-chip fabrication and embedding, device and circuit design under impact of unknown or variable mechanical stress, and the on- and off-chip implementation of sensor, actuator, microwave, and energy supply components are addressed.

INDEX TERMS Hybrid integrated circuits, thin film circuits, flexible electronics, micro assembly, multichip modules, chip scale packaging.

I. INTRODUCTION

Printed circuit board (PCB) and integrated circuit (IC) are well established technologies for achieving both utmost integration density and performance in nanoelectronics and, at the same time, electronic interfacing to the macroscopic user environment. During the past ten years several approaches have come up for merging those technologies, either by shifting PCB related aspects to the IC package, i.e., system-in-package (SiP) [1], or by shifting packaging related concepts and metal passive elements to the PCB or chip periphery (bare die in or on PCB [2], chip-in-mold eWLB technology [3]). All those efforts are directed towards watering down the interconnect and performance bottleneck at the chip edges where submicrometer interconnects on chip meet 10-100 micrometer dimensions on PCB. Also, due to that fact, a substantial part of the chip area is devoted to bond pads, thus increasing the total chip area and cost, which is particularly of concern for small chips.

Those mentioned approaches relate to rigid PCB carriers and thick chips. Obviously, with migrating such concepts to ultra-thin and bendable chips and to foil carriers instead of PCB, one would arrive at a large-area Hybrid System-in-Foil (HySiF) which paves the way to entirely new applications of electronic components in which form factor, form adaptivity and form flexibility play a decisive role [4]–[7], (Fig. 1).

This paper provides an overview of a comprehensive 10-year research program on HySiF technology and applications, involving thin-chip fabrication (Section II) and embedding (Section III), large-area electronic components (Section IV), design considerations (Section V) and application demonstrators (Section VI). Section VII provides the conclusions.

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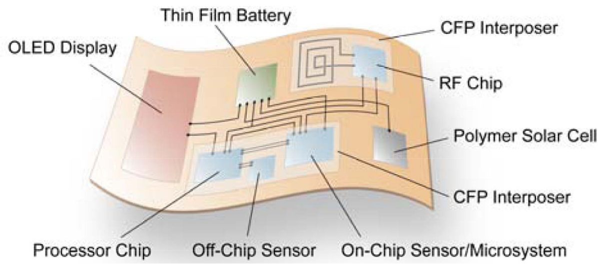

FIGURE 1. Concept of a Hybrid System-in-Foil (HySiF).

II. ULTRA-THIN CHIP FABRICATION

A. GENERIC APPROACHES

Thin chips feature a paradigm shift in microelectronics [8]. Conceptually, thin chips can be derived by thinning wafers after CMOS integration, followed by separation of the thin dies (Fig. 2a). A more precise control of the final chip thickness is possible when using silicon-on-insulator (SOI) instead of bulk silicon wafers, which, however, considerably increases cost. Those technologies represent the subtractive kind of approach to thin chip fabrication since the major part of the original wafer is sacrificed. There are also technologies, such as IBM's spalling [9], which allow for separating the top part of the wafer while conserving and reusing the bulk substrate. This is particularly important for costly wafer substrates such as GaAs, GaN and SiC but of lesser significance for silicon. All such subtractive technologies suffer from the difficulty in handling the resulting ultra-thin wafer and in separating the thin dies. The dicing before grinding (DBG) technique provides the technological advantage by avoiding separation of the thin chips by means of sawing (see Section II-B; Fig. 2b) [10].

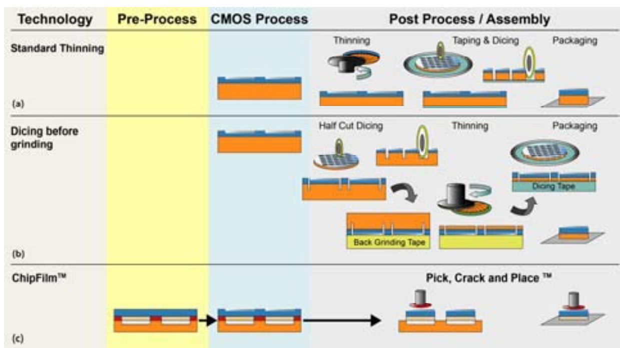

FIGURE 2. Illustration of candidate technologies for fabricating thin and ultra-thin chips, i.e., standard thinning of wafers followed by thin-chip singulation, ultra-thin chips through dicing before grinding, and ChipFilm technology.

In contrast, an additive approach to thin chip fabrication would consider preparing the thin chip on the silicon substrate and detaching it from the wafer. However, an additive approach can also provide the advantage of a far better chip thickness control and surface quality, which are beneficial aspects for dealing with stress management (see Section V-B). It can also be designed for thin-chip rather than thin-wafer fabrication, hence allowing for far easier thin-die singulation. The ChipFilm technology described in Section II-C provides all of those benefits (see also Fig. 2c) [11], [12].

B. CHIP DICING BEFORE GRINDING – A SUBTRACTIVE APPROACH

Chips are typically separated from wafers by sawing along dicing channels between the chips after the wafer has been attached to a dicing tape for supporting the chips temporarily. When wafers are thinned down to thickness below ~50 μm the sawing process may cause mechanical damage of the chip edges (edge chipping), which may lead to chip fracture. A half-cut dicing process prior to the back-grinding avoids chipping and enables thinning down to thicknesses well below 50 μm. This dicing-Before-grinding (DBG) approach [13], [14] has the advantage that it is a true post process following the CMOS integration and benefits from the tremendous progress with grinding processes in recent years, now enabling wafer thinning down to 20 μm with decent thickness uniformity [10]. As a further improvement, sawing can be avoided when applying deep reactive ion etching (RIE) to a depth equal the intended chip thickness prior to wafer thinning. Caveats are that thickness control and reproducibility remain difficult and that grinding introduces considerable stress which leads to warpage (see Section III-B) and reduced mechanical reliability (see Section III-C).

C. CHIPFILM TECHNOLOGY – AN ADDITIVE APPROACH

ChipFilm technology (Fig. 2c; Fig. 3) exploits precise chip thickness definition by epitaxial layer growth on a silicon wafer having a dual porous silicon (PorSi) layer at its surface, which results in buried cavity formation underneath the chip areas (Fig. 3a).

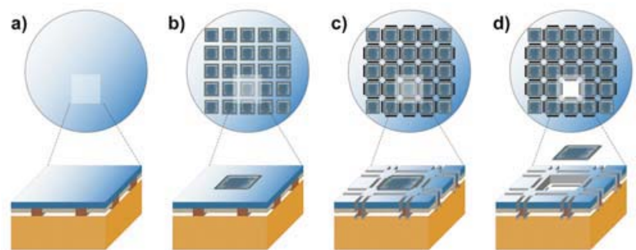

FIGURE 3. Schematic illustration of ChipFilm technology: (a) starting wafer substrate with buried cavities, (b) after integration of CMOS circuitry over buried cavities, (c) after trenching along chip edges, and (d) after chip detachment.

The thus predefined thin chips are anchored laterally [11] or vertically [12] for strong mechanical attachment to the wafer during the succeeding CMOS processing (Fig. 3b). Lateral anchors have the advantage that the mechanical action of anchor breakage is spaced away from the electrically active parts of the chips. However, the fact that the cavity underneath the chip area becomes evacuated as

a result of the epitaxial overgrowth process in hydrogen atmosphere, the silicon membrane settles downwards resulting in a non-planar wafer surface which is unsuitable for deep sub-micrometer CMOS device integration [11]. This issue is removed when using vertical anchors underneath the mentioned chip membrane, though anchors need to be designed to ensure breakage exclusively within the anchors without any micro cracks propagating to the electrically active device region [12]. Through etching of trenches along the chip edges reaching down into that buried cavity the process induced stress on the vertical anchors increases by about two orders of magnitude, resulting in a weak but still firm attachment of the chip to the substrate (Fig. 3c; Fig. 4a).

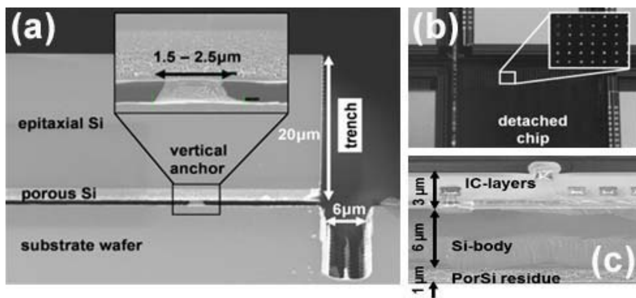

FIGURE 4. Images of (a) a cross section of a ChipFilm die in weak attachment after trenching (see Fig. 2c), (b) a plan view of a wafer section from which a ChipFilm die was detached (see Fig. 2d), and (c) a cross section of a detached 10-µm ChipFilm die.

By means of additional externally applied stress through well-defined wafer bending, a defined part of the vertical anchors become broken, so that the chips are weakly attached to the substrate carrier, i.e., still strong enough to remain on the substrate though weak enough for detaching the chips (Fig. 3d, Fig. 4b) by using a Pick,Crack&Place method [11], [12]. That weak attachment can be tailored by using either uniform (Fig. 5a) or non-uniform (Fig. 5b) anchor arrays underneath the chips.

ChipFilm technology allows for fabrication of chips having thickness of 10 µm (Fig. 4c) with the advantage of accurate chip thickness control which eases stress management in foil substrate assembly (see Section III-B). ChipFilm wafer substrates can be built with individual buried cavities underneath each chip area (Fig. 3a) or with a global buried cavity that extends over the entire wafer area, except for a solid silicon ring at the wafer edge (not shown). ChipFilm wafers with individual cavities have the advantage that chips are separated by solid silicon chip dividers (analogous to dicing channels), thus proving strong chip membrane attachment during the CMOS integration process (Fig. 3b). Trenching along the die edges then removes the lateral attachment to those silicon chip dividers, thus distinctly transforming from a strong to a weak chip attachment (Fig. 3c, Fig. 4b). This provides a wide process window between strong and weak chip attachment. The disadvantage, however, is that the starting substrate has to be prepared with the chip sizes and locations in mind, i.e., with a pre-process (Fig. 2a), which is not the case if the global buried cavity is implemented, thus providing a generic ChipFilm wafer substrate. In that case, however, a sufficiently wide process window has to be derived from more sophisticated anchor architectures, using different sizes or different densities of anchors.

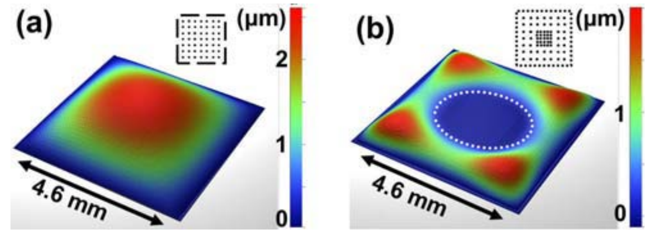

FIGURE 5. Topographic profile images of ultra-thin ChipFilm dies after externally applied stress by which well-defined parts of the vertical anchors underneath the chips became broken while other parts remain intact, thus providing a weak attachment to the substrate carrier: (a) uniform anchor array; (b) non-uniform anchor array.

III. ULTRA-THIN CHIP EMBEDDING

Direct embedding of chips in flexible PCB [15] or of thin chips in foil [16], [17] appears as the most straightforward way to realize HySiF (Fig. 6a). However, this requires that laser drilled and electroplated vias be landed directly on the contact pads of the embedded chip, which adds to the chip area and, thus, cost. Also, the metallization schemes of PCB and chip technologies are incompatible unless contact pads on chip receive a suitable noble metal capping [15]. Chips can either be embedded face-up [16] or face-down by means of solder-bump flip-chip assembly [17]. In all cases contact pads are needed, which may limit the input/output (I/O) count or increase the chip area. This can be avoided by applying a fine-pitch metal layer that connects the chip with high I/O count to the foil peripheral area, thus omitting large contact pads and only requiring small test pads on the chip area [17]. However, the face-up implementation of the chips and the use of coarse-pitch assembly technology prevents from matching the metal pitch of the global interconnects on chip and, thus, from reaching the maximum I/O count and the minimum chip die area. This can be achieved by using Chip-Film Patch (CFP) technology in which the same lithographic patterning technology is applied to both the chip and foil peripheral areas [19], [20]. CFP thus features a foil interposer patch which is structured by means of microelectronic chip fabrication processing, thus allowing for a more favorable interconnect transition from chip to foil or between embedded chips (Fig. 6b).

A. CHIP-FILM PATCH (CFP) EMBEDDING TECHNOLOGY

Chip-Film Patch (CFP) has been derived from ChipFilm technology but is applicable to any kind of thin-chip fabrication. The basic idea behind CFP is not to embed the thin chip directly into the foil substrate (Fig. 6a) but instead into a foil interposer (Fig. 6b) featuring a foil patch with the chip having an overall micro-structured global metallization

FIGURE 6. Examples of chips (4.6×4.6 mm², 20 µm thick) directly embedded into (a) a flexible LCP [18] (20×20 mm², thickness 70 µm) or (b) by using CFP interposer technology (15×15 mm², thickness 60 µm).

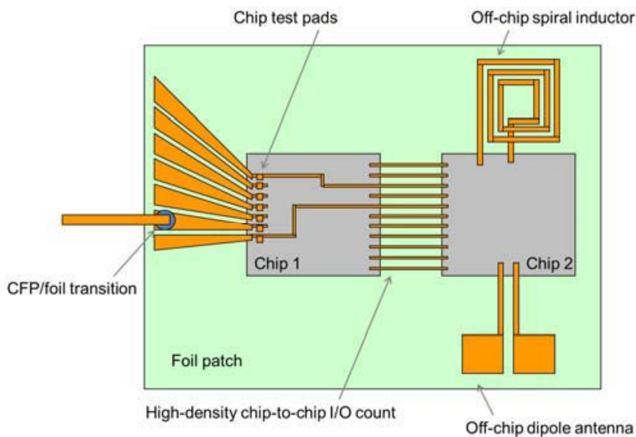

FIGURE 7. Illustrative plan view sketch of a CFP sample with indication of its benefits *versus* direct embedding of thin dies: (1) omittance of peripheral contact pads, thus decreasing chip area and cost; (2) feasibility of high-density chip-to-chip interconnects; (3) off-chip passive metal components, leading to higher quality and lower cost.

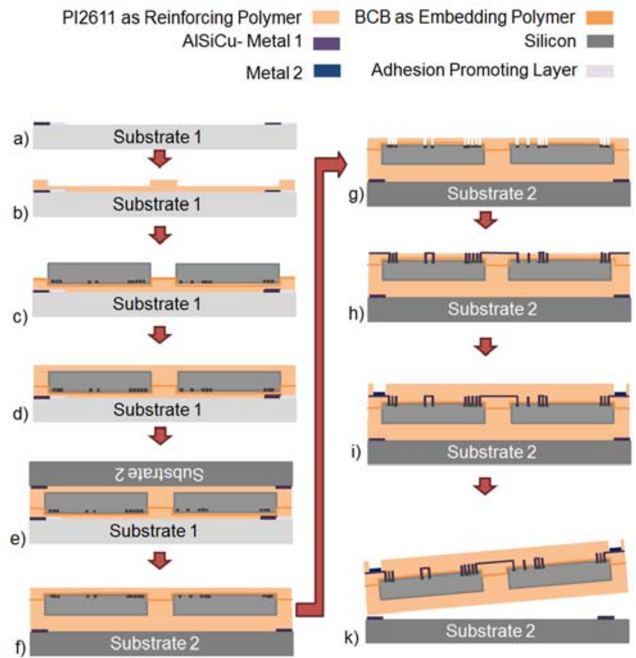

FIGURE 8. Process sequence of a CFP including two thin chips.

for foil and chip regions using photolithographic patterning (Fig. 6b; Fig. 7).

The CFP is then embedded into, and interconnected to, the foil substrate of the HySiF in place of the standalone thin chip. This allows for omitting any bond pads at the chip edges, thus achieving smaller silicon die area for reducing cost as well as realizing a far higher I/O count (Fig. 7). The CFP also allows for implementing spacy passive metal structures, such as inductors, transformers and antenna's into the foil peripheral area, hence reducing chip real estate and cost even more (Fig. 7). The CFPs are fabricated as a composite of Benzocyclobutene (BCB), which can be patterned like a photoresist, and of polyimide on a silicon wafer carrier using silicon processing [19], [20].

Chips can be embedded face-up [19] and face-down (Fig. 8). The face-up option has the advantage that the CFP can be built on the processing wafer carrier from which the CFP is released at the end, thus only one release process is required. As a disadvantage, differences in chip thickness result in excessive surface topography, thus requiring thicker polymer layers for the global interconnects which limits the interconnect metal pitch to about 10 µm. Better conditions enabling micrometer-pitch global interconnects result from the face-down option (Fig. 8). There, the chips are first assembled face-down temporarily on a first carrier wafer substrate (Substrate 1 in Fig. 8), so that the device layers of the chips are levelled (Fig. 8a-d). After attaching a second carrier wafer substrate (Substrate 2; Fig. 8e) that first substrate is removed and the mentioned global interconnect layer (or multiple layers) can be added (Fig. 8f-i). Finally, the CFP is detached from the second carrier and becomes available for assembly into the HySiF (Fig. 8k).

A key issue is the alignment of the embedded chips to the global interconnects, because the chips can become slightly shifted and rotated during transfer to the foil carrier and curing of the polymer materials. As a result, the interconnect layout either needs to be relaxed in order to accommodate those alignment errors, which, however, contradicts the CFP basic concept, or the layout needs to be adjusted.

An adaptive layout can be realized by using a maskless laser direct writer (Heidelberg Instruments VPG400) in which first the relative chip position is measured, the layout design (Fig. 9a) is adjusted (Fig. 9b) and the adjusted layout is applied lithographically (Fig. 9c) [20], [21]. This adaptive layout technique, thus, provides a means of taking full advantage of the CFP concept. It can also be instrumental in applying layout adjustments to global interconnects on thin and embedded chips due to chip warpage. Economic constraints of laser lithography can be addressed by exploiting mix&match lithography [20], [21].

B. STRESS AND WARPAGE MANAGEMENT

Both approaches, i.e., direct chip embedding or CFP, are sensitive to stress and warpage. Process induced stress can lead to an initial warpage of the thin chips which may

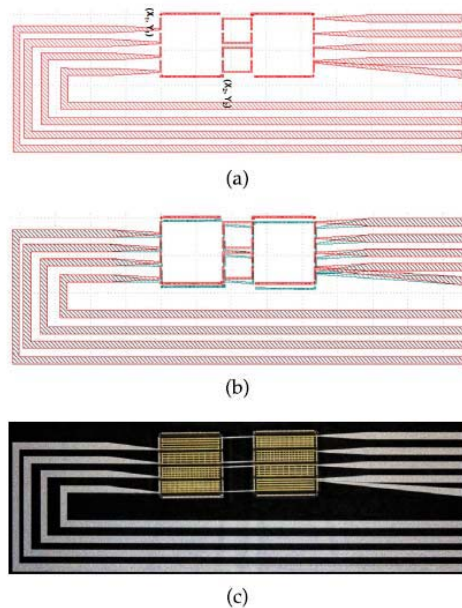

FIGURE 9. Illustration of the adaptive layout technique to accommodate for alignment errors in chip embedding: (a) original layout, (b) adjusted versus original layout based on measurement in the maskless laser lithography tool, and (c) plan view of the fabricated CFP with embedded chips and interconnects with adapted layout.

hamper chip embedding (Fig. 10), [22]. That warpage can be tailored and minimized either by means of chip layout considerations [23] or by adjusting the wafer process technology [22], [24]. After embedding the thus planar chip into the foil additional warpage due to process related stress may occur. In CFP technology the process conditions can be tailored to arrive at minimum final warpage [24] which may be crucial for proper implementation of the CFP into the global foil carrier. However, also the final implementation of the CFP into the flexible substrate of the HySiF may cause renewed warpage. As a conclusion, warpage management during CFP fabrication and implementation into a HySiF are crucial.

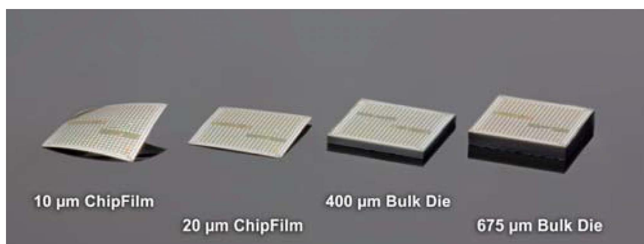

FIGURE 10. Chips singulated from a common 150-mm silicon wafer (675 µm), after thinning prior to conventional packaging (400 µm), and by using ChipFilm technology to realize ultra-thin chips (20 µm and 10 µm). Warpage due to process induced stress increases considerably towards smaller chip thickness.

C. HYSIF MANUFACTURING ISSUES

The System-in-Foil (SiF) approach has been adopted from printing on paper substrates. At first glance, this makes roll-to-roll (R2R) printing of organic electronics the manufacturing process of choice [4], [25]. This technology concept clearly aims to high throughput and low-cost manufacturing of SiF. Unfortunately, the carrier mobility in organic semiconductors is 10 to 100-fold lower than that of silicon, there is no viable complementary TFT technology established yet, operating voltages are ranging between 10 V and 100 V, and organic materials tend to degrade in humid ambient, hence requiring a sophisticated barrier technology. However, recent progress in submicrometer fabrication of organic thin-film transistors (TFTs) and their operation at voltages far below 10 V gives hope that OTFT technology can further be improved and be made compatible with high-performance CMOS microelectronics and, thus, be extended to HySiF [26], [27]. For that purpose, electronic chiplets fabricated in silicon technology should be attached to the foil substrate in a massively parallel approach rather than in serial mode [28]. The main disadvantage of R2R, particularly when extended to HySiF manufacturing, is that the slowest process step limits the overall throughput.

Other than the R2R approach, sheet-to-sheet (S2S) integration of HySiF allows for decoupling the consecutive process steps and modules and, thus, to arrive at an overall more economic manufacturing for HySiF. It seems obvious that the required fabrication process can be adopted from the readily available TFT display manufacturing technologies [29] provided that a final layer transfer process from glass to foil is available [30], that ultra-thin bendable glass foils can be employed [30], or that ultra-low processing on foil carriers is feasible [31].

IV. LARGE-AREA AND HYBRID ELECTRONIC DEVICES

Large-area electronics relates to electronic devices that can widely be spread across a rather large substrate in contrast to the dense and highly integrated devices on a silicon chip. Such devices can – in spite of the large substrate – be monolithically integrated [29] or be assembled on that substrate in a hybrid fashion. It is a matter of compatibility of device fabrication processes and related materials if the monolithic or hybrid approach is to be preferred. However, as indicated by its name, in HySiF, in which numerous and fundamentally different technologies are implemented to form a complex microsystem, hybrid electronic devices and components are a necessity.

A. THIN-FILM TRANSISTORS

In addition to the OTFTs mentioned in Section III-C, TFTs based on amorphous silicon [32], polysilicon [33], recrystallized large-grain quasi-monocrystalline silicon [34] and metal-oxide materials [35] can be employed if higher process temperatures are feasible, such as on glass and thin-glass substrates.

B. ON-CHIP VERSUS OFF-CHIP SENSORS

Sensing elements are an essential part of HySiF. They can either be integrated on a thin silicon chip or be fabricated directly on the foil substrate. Sensors on chip are

the preferred choice if close vicinity to the electronic signal processing is crucial [35], if the sensor is complex and needs to be compact (e.g., image sensor), if the piezoresistive effect in silicon can be exploited (e.g., stress [36], [37], pressure and acceleration sensors) and, in general, if the sensor area can be small and only a single sensor or a few sensors are needed. Off-chip sensors are chosen if wide-spread distribution of numerous sensing elements is required, if the sensing area needs to be large and if the implementation off chip provides economic advantages [38].

C. ACTUATORS AND DISPLAYS

Actuators, such as thermal heaters used in flow meters and piezo elements can be implemented in or on the foil substrate and be driven by electronics on a thin chip in the HySiF. Displays should be operated at low power, e.g., electrophoretic, if the HySiF is standalone and powered by battery or possibly through energy harvesting. High-quality and power hungry displays, such as organic light emitting diodes (OLEDs) can be employed if the HySiF is wire connected.

D. WIRELESS COMMUNICATION

Wireless transceivers can be implemented by using RF CMOS circuitry on thin chips. Large passive components such as antenna's, inductors and transformers can be embedded into the foil periphery of those chips. This points directly to the CFP technology which allows seamless interconnection of the electronics on chip and such metal passives off chip.

E. ENERGY SUPPLY

HySiF may be wire connected, may work wirelessly with energy supply from a battery, or may rely on energy harvesting. In all cases an implemented flexible battery will be required for buffering purposes, as sole energy supply, or as an energy reservoir. Batteries can be assembled in HySiF as components, such as thin flexible Li-ion cells [39] or be integrated using PVD process technologies [40]. It may be required to combine those battery power supplies with flexible micro super capacitors for buffering abrupt high demands of energy [41].

V. HYSIF DESIGN CONSIDERATIONS

From a structural point of view, HySiF's are composites of thin silicon chips, plastic films and metal layers, which are bent so that compressive and tensile strains build up at its front and back surfaces. The apparent stress levels depend on those strains and on the E-moduli and the thickness of the particular layers [42]. The relationship between bending radius and, thus, strain and apparent stress, also depends on the way of applying the HySiF. If it is free standing, the strain-stress relationship depends on the material structuring within the HySiF. If it is attached to a bent surface, then also the underlying materials will affect the apparent stress in the HySiF, depending on the strength of the attachment [42].

A. LEVERAGING THE NEURAL LINE OF STRESS

While maximum tensile and compressive stresses appear at the outer surfaces of the HySiF, there will always be a neutral line of stress within the composite, at which the apparent stress is zero. If the HySiF composite could be designed so that the neutral line of stress coincides with the active region of the embedded CMOS chip, i.e., near the chip surface, the piezoresistive effect can effectively be suppressed [42]. Also, at the interconnect transitional region at the chip edges, where the E-modulus alters abruptly by a factor of ∼100, the interconnects will be protected from mechanical stress impact, thus leading to improved micromechanical reliability. Also, the apparent stress at the structured surface of the CMOS chip is suppressed. This is beneficial since that particular surface of the thin chip limits the maximum applicable stress and, thus, the mechanical stability of the chip [22].

However, the degree of freedom in positioning the neutral line of stress within the HySiF stack is limited due to the 100-fold higher E-modulus in silicon compared to that of the foil materials. This can be circumvented by stacking a silicon dummy die with tailored thickness on top of the thin active CMOS chip [43]. Given the fact that the most stress sensitive surface of the CMOS chip is effectively protected from stress impact, the two-chip stack could exhibit better mechanical stability than the sole CMOS chip in spite of the greater thickness [44]. Instead of a dummy chip a second active CMOS chip could be stacked on top of the first CMOS die. If those two stacked CMOS chips are interconnected by means of through silicon vias at the top die, a HySiF microsystem with a stress-sensitive top layer for stress sensing functions and a stress compensated bottom layer for stress-insensitive signal processing purposes can be built [45].

B. CIRCUIT DESIGN UNDER IMPACT OF STRESS

In cases in which only one CMOS chip is embedded in the HySiF, other means of stress management need to be employed. A rather simple approach is to empirically consider the impact of the orientation dependent stress on the channel mobility in NMOS and PMOS transistors in the process corners of the circuit simulator, which, obviously, sacrifices circuit performance [46].

A more performance-aware approach comes with intentionally exploiting the different polarities and degrees of piezoresistive effects in NMOS and PMOS transistors laid out in longitudinal or transversal orientation in combination with suitable circuit building blocks [36], [47].

Moreover, the circuit designer needs to be aware of possible deviations of externally applied stress and apparent stress levels on chip, if stress should be detected through MOS transistors or resistors. Depending on the strength of the glue attachment of the CMOS die to the foil carrier in assembly, a uniaxial applied external stress can be transformed into a biaxial stress, thus leading to quite unexpected stress levels on chip [48].

C. THERMAL DESIGN ISSUES

It is common believe that thinning down a chip prior to assembly in the package will lead to an improvement as far as thermal power dissipation is concerned. However, if the chip is embedded in a stand-alone HySiF, where power dissipation occurs by means of heat convection at its surface exposed to the ambient, thinning down to very small thickness might be counterproductive. This is because of the then large lateral thermal resistance and the lack of a low-resistive thermal path from ambient to the backside of the chip, which will lead to considerable self-heating [49], as also known for SOI technology [50]. Engineering solutions come from using metal heat spreaders or from using thicker chips, reducing local self-heating, and the latter in a trade-off with bendability [49].

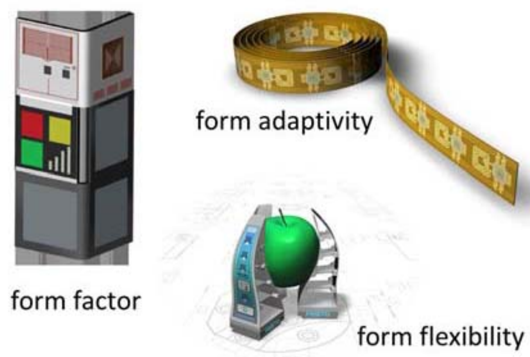

FIGURE 11. HySiF applications to form factor aspects [48], form adaptivity issues [49] and to form flexibility needs [48].

VI. APPLICATION DEMONSTRATORS

HySiF can provide unique technical solutions wherever form factor, form adaptivity or firm flexibility are crucial requirements (Fig. 11). One example of a HySiF satisfying needs for form factor improvement is a safety switch that was transformed from a macroscopic component of mm to cm dimensions into an electronic scotch tape component [31]. Form adaptivity is the key criteria for a smart label which can be applied to industrial products and parts thereof in the context of smart industry [50]. Form flexibility is needed in applications for robotics where haptic gripping processes are required [30].

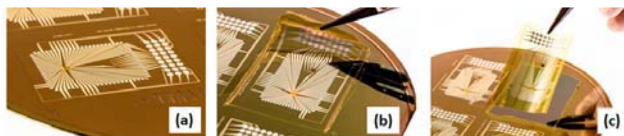

FIGURE 12. Two commercial chips [51], [52] that are embedded and interconnected in a foil interposer patch using CFP technology and adaptive layout lithography. The CFP is shown (a) while still residing on the wafer carrier, (b) after cutting and start of peeling off that carrier, and (c) after complete detachment.

Fig. 12 shows a fully functional application demonstrator, i.e., the embedding and interconnecting of a commercial microcontroller chip (Ambiq micro Apollo 1, [51]) with a near-field communication (NFC) chip (NF4: Dual interface NFC Forum Type 4 tag IC, [52]) using CFP technology and the adaptive layout technique. The Apollo chip is an ultra-low power microcontroller largely used in wearable electronics. The NF4 chip implements the near-field communication protocol and should be connected to an external NFC antenna which resides on the foil carrier onto which the CFP is to be mounted [18], [23]. On the patch, the digital I/O's of the NF4 (wireless communication chip) are connected to the Apollo die (wired communication and signal processing chip). Also all of the NF4 and most of the Apollo pads are connected to the larger pads on the foil carrier.

VII. CONCLUSION

HySiF represents the next level of systems-in-foil in terms of performance and application diversity. They satisfy specific requirements in form factor, form adaptivity and form flexibility, which conventional electronic components cannot meet. HySiF, thus, features a paradigm shift in integrated electronics. In HySiF, thinned highly integrated and high-performance chips are combined with large-area electronics in order to merge the merits of both classes of electronics. Technological challenges come with the abrupt, >100-fold change in metal interconnect pitch and in E-Modulus from chip to foil, limiting I/O count and mechanical reliability. Those challenges can best be met by using a CFP interposer. This allows for a joint global interconnect scheme between chip and surrounding foil area and, thus, a considerably higher I/O count. Also, the neutral line of stress can be exploited in designing the foil-chip compound, thus dramatically improving mechanical reliability. The HySiF technology will, therefore, involve large-area electronics, CFP components including thin chips, as well as other flexible components. This will favor sheet-to-sheet rather than roll-to-roll manufacturing.

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