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Low-Voltage Programmable Gate-All-Around (GAA) Nanosheet TFT Nonvolatile Memory Using Band-to-Band Tunneling Induced Hot Electron (BBHE) Method

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ABSTRACT A low-voltage programmable gate-all-around (GAA) nanosheet poly-Si thin-film transistor (TFT) nonvolatile memory (NVM), which uses band-to-band tunneling induced hot electron (BBHE) programming, is demonstrated. The BBHE method is extremely efficient for programming data in the p-type GAA nanosheet TFT NVM because the GAA nanosheet structure enhances the source-to-drain component of the electric field in its channel. Therefore, the enhanced electric field of the BBHE phenomenon creates energetic electrons that surmount the tunneling oxide barrier easily and pass shallow traps in the charge trapping layer of the GAA TFT NVM. Consequently, the p-type GAA TFT NVM achieves low-voltage programming bias and satisfactory data retention.

INDEX TERMS Band-to-band tunneling induced hot electron (BBHE), gate-all-around (GAA), nanosheet, thin-film transistor (TFT), nonvolatile memory (NVM).

I. INTRODUCTION

For scaling CMOS technology according to Moore's law, multi-gate MOSFETs, such as FinFETs and gate-all-around (GAA) Nanowire/Nanosheet FETs, are proposed to suppress the short channel effect (SCE). The entire channel of a multi-gate FET is close to the gate electrode. Thus, the multi-gate structure reduces the leakage path in the channel. Of these multi-gate structures, the GAA Nanosheet FET provides superior driving current with excellent gate controllability because the GAA Nanosheet FET has a flexible choice of the effective channel width and the channel surface area. Thus, the GAA Nanosheet is a promising candidate for sub-7nm technological nodes [1]–[5].

Numerous products utilizing silicon-oxide-nitride-oxide-silicon (SONOS) nonvolatile memory (NVM) have been developed, especially for 3D NAND applications, because the charge trapping layer stores charges in spatially isolated deep-level traps, and a single-leakage path does not cause serious threshold voltage degradation [6], [7]. To improve the programming efficiency of NVM, band-to-band tunneling induced hot electron (BBHE) programming has been proposed. Writing data through BBHE features low program bias and high BBHE charge injection efficiency (approximately 10^{-2}) [8], [9]. In SONOS NVM applications, the GAA Nanowire/Nanosheet structures enhance the vertical (gate-to-channel direction) electric field in tunneling oxide. Accordingly, the GAA Nanowire/Nanosheet structure improves the programming/erasing (P/E) efficiency of SONOS NVM [10], [11]. Here, a fast and low-voltage-programmable p-type GAA Nanosheet TFT NVM is demonstrated. According to the experimental results, the GAA Nanosheet structure enhances not only the vertical

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electrical field but also the horizontal (source-to-drain direction) electric field, which can further reduce the programming bias of the BBHE programming method. Thus, this high-performance GAA Nanosheet NVM can be utilized for low-voltage one-time programmable (OTP) memory and flash memory on the glass substrate of active-matrix liquid-crystal display (AMLCD) and active-matrix organic light-emitting diode (AMOLED) display to realize system on panel (SOP) products.

II. FABRICATION

A p-type GAA Nanosheet TFT memory was fabricated by depositing a 400 nm-thick wet oxide on 6-inch Si wafers. The active layer was a 50-nm-thick amorphous Si (α-Si) layer which was deposited through low-pressure chemical vapor deposition (LPCVD) at 550 °C. Solid phase crystallization (SPC) process was then performed at 600 °C for 24 hours in a nitrogen ambience. Ten nanowires were patterned by e-beam direct writing and transferred by reactive-ion etching (RIE), followed by dipping in HF solution to form the GAA Nanosheet structure. The schematic top view of the ten nanowires is shown in Fig. 1(a), and Fig. 1(b) shows the schematic side view along the A-A' direction depicted in Fig. 1(a) after dipping in the HF solution. The thickness of the active layer was trimmed by growing thermal oxide [Fig. 1(c)]. Subsequently, a 20-nm-thick thermal SiO_2 layer was grown as the tunneling oxide. Above the thermal SiO_2, Si_3N_4/a-Si/Si_3N_4 (N/α/N) were deposited as a charge trapping layer through LPCVD, and the thicknesses of Si_3N_4/a-Si/Si_3N_4 are 3, 2, and 3 nm, respectively. An 18-nm-thick *tetra-ethyl-orthosilicate* (TEOS) SiO_2 was deposited as the blocking oxide. Next, a 200-nm-thick in situ doped n+ poly-silicon was deposited and transferred through e-beam direct writing and RIE as a gate electrode with a gate length of 0.43 um. The schematic top view of the GAA Nanosheet TFT memory is shown in Fig. 1(d). Then, the self-aligned source and drain regions were implanted with phosphorous ions at a dose of 5×10^{15} cm^{-2} and activated by rapid thermal annealing at 1050 °C for 1 second in a nitrogen ambience. A 200-nm-thick SiO_2 passivation layer was deposited, and metal contacts were patterned by e-beam direct writing and transferred by RIE. Finally, Al–Si–Cu metallization was performed to a thickness of 300 nm and all samples were sintered at 400 °C in a nitrogen ambience for 30 minutes. Fig. 1(e) lists the key processes of the GAA Nanosheet TFT memory.

III. RESULTS AND DISCUSSION

Fig. 2(a) shows the schematic cross-sectional view of the Nanosheet of a p-type GAA Nanosheet TFT NVM with 5-nm-thick channels. A p-type tri-gate TFT NVM with a channel thickness of 25 nm was also fabricated for comparison, and a schematic cross-sectional view of the tri-gate TFT NVM is shown in Fig. 2(b). The tri-gate TFT NVM has exactly the same channel width and dielectric layers as the GAA Nanosheet TFT NVM. The gate length and

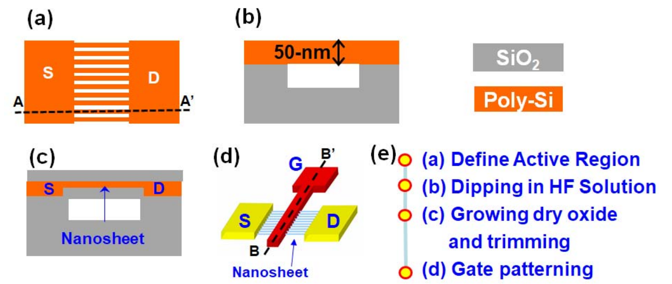

FIGURE 1. (a)-(b) The key process flows for the fabrication of the GAA Nanosheet TFT NVM, and (e) the brief interpretation of Fig. 1(a) to Fig. 1(d).

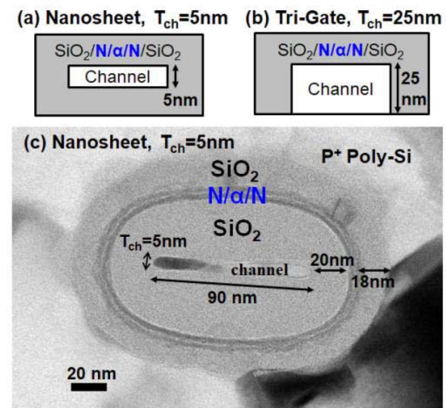

FIGURE 2. (a)-(b) Schematic cross-sectional views along the B-B' direction depicted in Fig. 1(d) in the GAA Nanosheet TFT NVM and in the tri-gate TFT NVM. (c) TEM cross-sectional image in the channel of the GAA Nanosheet TFT NVM.

the nanowire width of the GAA Nanosheet TFT NVM and the tri-gate TFT NVM are 0.43 μm and 90 nm, respectively. Fig. 2(c) shows a transmission electron microscope (TEM) cross-sectional image of the GAA Nanosheet TFT NVM. The Si_3N_4/a-Si/Si_3N_4 (N/α/N) is utilized as a charge trapping layer. The SONOS memory stores charge in the trap sites in the charge trapping layer as programming. The ultra-thin α-Si layer in the charge trapping layer can create high-density trap sites. High-density trap sites in the charge trapping layer lead to good charge capture rate and enhances the programming efficiency. Fig. 3 shows the transfer characteristics of the GAA Nanosheet TFT NVM and the tri-gate TFT NVM; the drain current is normalized by the effective channel width. The subthreshold swing of the fresh GAA Nanosheet TFT NVM and the fresh tri-gate TFT NVM are 158 mV/dec and 257 mV/dec, respectively. The GAA Nanosheet TFT NVM shows the transfer characteristics superior to those of the tri-gate TFT NVM because the GAA Nanosheet structure reduces leakage path effectively in its ultra-thin channel. Although the normalized drain current of the GAA Nanosheet TFT NVM and the tri-gate TFT NVM are similar, the actual driving current of the GAA Nanosheet TFT NVM is higher than that of the tri-gate TFT NVM because of the wider effective channel width

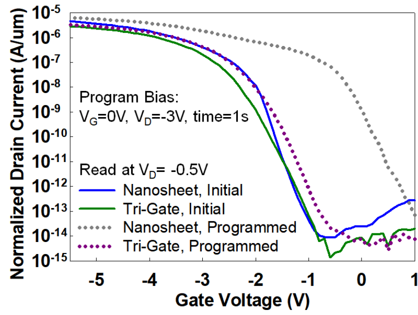

FIGURE 3. I_D-V_G curves of the GAA Nanosheet TFT NVM and the tri-gate TFT NVM at $V_D = -0.5V$ and $V_S = 0V$ in the initial state and the programmed state. Both devices are programmed at $V_G = 0V$, $V_D = -3V$, and $V_S = 0V$ for 1s from fresh devices.

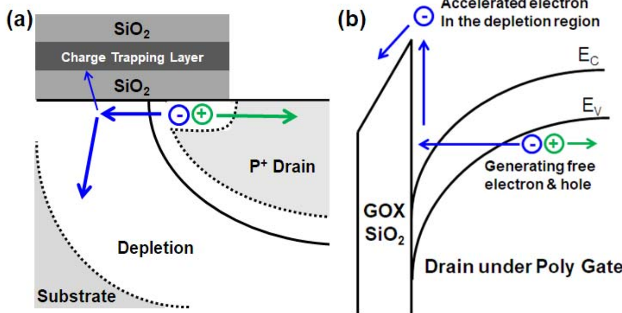

FIGURE 4. (a) Schematic cross-sectional view of a SONOS memory to illustrate the BBHE injection. The electrons gain energy in the depletion region. (b) Energy band diagram of a SONOS memory in the BBHE operation. Free carriers are generated from the band-to-band tunneling in the BBHE operation.

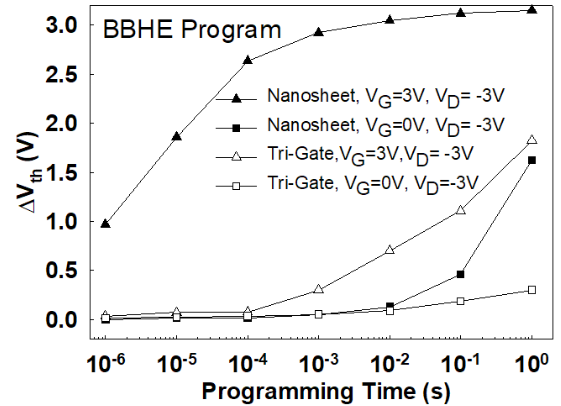

FIGURE 5. BBHE programming characteristics of the GAA Nanosheet TFT NVM and the tri-gate TFT NVM.

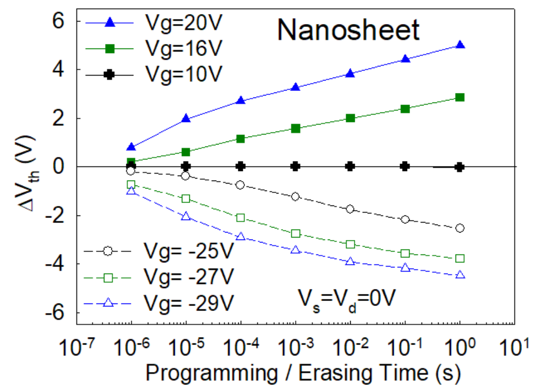

FIGURE 6. FN programming and FN erasing characteristics of the GAA Nanosheet TFT NVM.

of the GAA Nanosheet TFT NVM. The transfer characteristics of the programmed GAA Nanosheet TFT NVM and the programmed tri-gate TFT NVM are also presented in the Fig. 3. The programming bias is $V_G = 0V$, $V_D = -3V$ and $V_S = 0V$ for 1s. The programming mechanism of the p-type GAA Nanosheet TFT NVM and the p-type tri-gate TFT NVM is BBHE. The charge trapping layer stores electrons to change memory state in the BBHE operation. The GAA Nanosheet TFT NVM demonstrates programming efficiency superior to that of the tri-gate TFT NVM depicted in Fig. 3. The following sections will discuss this advantage of the GAA Nanosheet TFT NVM.

A negative drain voltage and a positive gate voltage are applied to a SONOS memory in a BBHE operation. The voltage difference between the gate and the drain creates a high vertical electric field. The drain voltage builds a depletion region at the boundary of the drain and body as depicted in Fig. 4(a). Fig. 4(b) graphs the band diagram of a SONOS memory in the BBHE condition. The band bending is steep in the overlap region of the gate and the drain due to the high vertical electric field in the BBHE condition. A large number of free electrons are generated through the band-to-band tunneling due to steep band bending. Then the free electrons are accelerated in the depletion region near the drain. Some of the accelerated electrons gain enough energy to surmount the tunneling oxide and stay in the trap sites of the charge trapping layer. The BBHE injection has a greater vertical electric field at the injection point than the channel-hot-electron (CHE) injection method has. Thus, the BBHE charge injection efficiency achieves 10^{-2}, which is much higher than the CHE charge injection efficiency (10^{-4}–10^{-5}) [8].

Fig. 5 plots the programming characteristics of the GAA Nanosheet TFT NVM and the tri-gate TFT NVM through BBHE programming. The programming voltage is from the pulse generator unit (PGU). The BBHE programming method operates at $V_G = 3$ V and $V_G = 0$ V with a negative drain bias of -3 V. The GAA Nanosheet TFT NVM shows high BBHE programming efficiency, which is vastly superior to that of the tri-gate TFT NVM. Fig. 6 plots the P/E characteristics of the GAA Nanosheet TFT NVM through the Fowler–Nordheim (FN) P/E method. Although the voltage difference between the drain and the gate is only 6 V, the BBHE programming efficiency of the GAA Nanosheet TFT NVM is considerably higher than the FN programming efficiency. The FN erasing of the GAA Nanosheet TFT NVM is inefficient because a hole with heavy effective mass faces a large barrier height. It should be noted that the delta V_{th} of the BBHE programming method

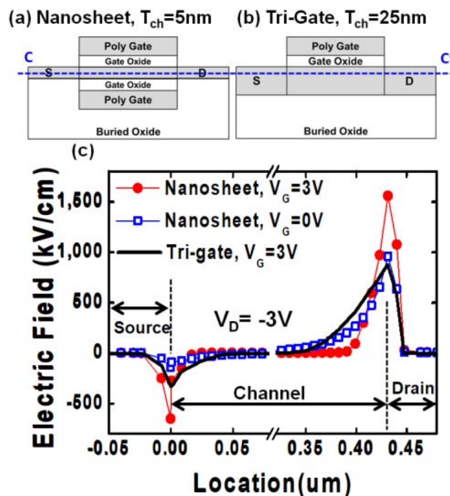

FIGURE 7. (a) Schematic cross-sectional view of the GAA Nanosheet TFT NVM parallel to S/D. (b) Schematic cross-sectional view of the tri-gate TFT NVM parallel to S/D. (c) Source-to-drain component of the electric field of the GAA Nanosheet TFT NVM and the tri-gate TFT NVM through TCAD simulation, which is along the A-A' of Fig. 7(a) and 6(b).

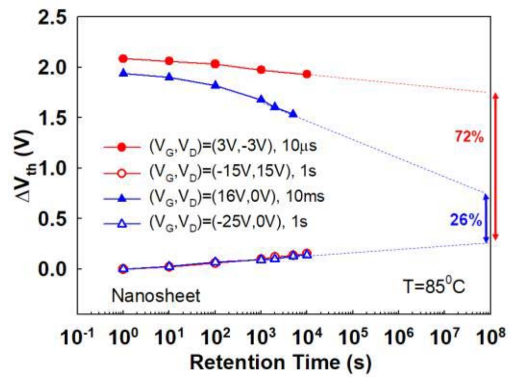

FIGURE 8. Retention characteristics of the GAA Nanosheet TFT NVMs through BBHE programming method and FN programming method.

saturates at 3 V, which is lower than the delta V_{th} of the FN programming method. The charges in the charge trapping layer prevent carrier injection into the charge trapping layer because the voltage difference between the drain and the gate is small in the BBHE programming operation for the GAA Nanosheet TFT NVM. Accordingly, a saturated V_{th} shift is observable for the BBHE method.

Fig. 7(c) shows the channel horizontal electric field of the GAA Nanosheet TFT NVM and the tri-gate TFT NVM along the S/D [C-C' cut of Fig. 7(a) and 7(b)] through technology computer-aided design (TCAD) simulation. The maximum horizontal electric field of the GAA Nanosheet TFT NVM is over 1500 kV/cm at $V_G = 3$ V and $V_D = -3$ V. However, the maximum horizontal electric field of the GAA Nanosheet TFT NVM is only approximately 1000kV/cm at $V_G = 0$ V, $V_D = -3$ V. The maximum horizontal electric field of the tri-gate NVM is also approximately 1000 kV/cm at $V_G = 3$ V, $V_D = -3$ V. What has to be noticed is that the channel electron concentrations of the GAA Nanosheet TFT NVM and the tri-gate TFT NVM are different in the same BBHE condition. First, the gate capacitance of the GAA Nanosheet TFT NVM is higher than that of the tri-gate TFT NVM. Hence, the GAA Nanosheet TFT NVM induces more electrons in its channel than does the tri-gate TFT NVM. Second, the channel volume of the GAA Nanosheet TFT NVM is smaller than that of the tri-gate TFT NVM. Relative to the tri-gate device, the GAA Nanosheet TFT NVM with an ultra-thin body has a higher electron concentration owing to the larger total number of induced electrons in the smaller volume of the channel in the BBHE condition. The tri-gate TFT NVM has a thicker body and does not have a bottom gate. Therefore, the electron concentration in the channel of the tri-gate TFT NVM does not increase obviously at $V_G = 3$ V, $V_D = -3$ V. The horizontal electric field is enhanced by the gate bias in the GAA Nanosheet TFT NVM because of the high concentration gradient between the channel and the drain of the GAA Nanosheet TFT NVM in Fig. 7(c). The GAA Nanosheet TFT NVM has an electron-rich channel in the BBHE condition. To balance the carrier concentration between the electron-rich channel and the drain, the horizontal electric field further increases in the depletion region of the drain when the gate bias is applied to the ultra-thin GAA Nanosheet TFT NVM [12].

To program data through the BBHE method, the free electron created from the band-to-band tunneling must be accelerated by a high horizontal electric field in the depletion region [8]. Therefore, the GAA Nanosheet TFT NVM reveals high programming speed because of the high horizontal electric field in the GAA Nanosheet structure. When gate voltage is zero, the programming efficiency of the GAA Nanosheet TFT NVM decreases obviously due to the low electron-hole pair generation rate of band-to-band tunneling. As mentioned before, this low BBHE efficiency at $V_G = 0$V occurs also because the gate bias can enhance the horizontal electric field in the GAA Nanosheet structure. The gate bias can force energy band bending in the channel of the GAA Nanosheet TFT NVM. A gate bias of $V_G = 3$ V leads to steep energy band bending in the channel. Consequently, the conduction band is close to the Fermi-level in the ultra-thin channel of the GAA Nanosheet TFT NVM, which causes high electron concentration for the whole channel during BBHE operation. Therefore, the gate voltage is essential to enhance the electron-hole pair generation rate and to increase the electron energy of the GAA Nanosheet TFT NVM during BBHE operation.

Fig. 8 plots the retention characteristics of the GAA Nanosheet TFT NVM using the BBHE programming method and the FN programming method. The memory windows of the GAA Nanosheet TFT NVM using the BBHE programming method and the FN programming method are 72% and 26%, respectively, after ten years at 85°C. To further discuss the retention characteristics, we discuss the electron behavior in the charge trapping layer for BBHE and FN programming operations. Because the electrons gain insufficient energy in the channel through FN-tunneling, the

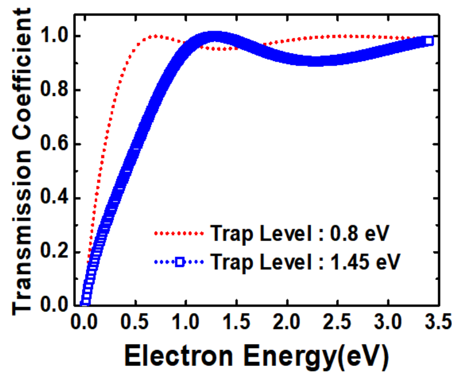

FIGURE 9. Transmission coefficient with electron energy from 0 eV to 3.4 eV for the trap levels of 0.8 eV and 1.45eV.

electron net velocity is much smaller than thermal velocity. Thus, the electrons suffer enormous collisions because of their random behavior when the electrons pass through the tunneling oxide in the FN-tunneling operation. In the BBHE operation, the net velocity of the BBHE electrons is the same order of magnitude of thermal velocity (approximately 10^7 cm/s). Relative to the FN-tunneling electrons, these energetic BBHE electrons have fewer collisions in the tunneling oxide and preserve more energy in the charge trapping layer. The transmission coefficient of a free electron with mass = m_e and energy = E for a shallow and narrow quantum well with the depth = $-V_0$ is as follows [13]:

$$T^{-1} = 1 + \frac{{V_0}^2}{4E(E+V_0)}\sin^2\left(\frac{d}{h}\sqrt{2m_e(E+V_0)}\right)$$

where h is Planck's constant and d is the width of the quantum well. The trap level in the SONOS NVM is 0.8eV to 1.45eV in the charge trapping layer [14]. The capture cross-section area of the SONOS NVM is approximately 10^{-13} cm^2 to 10^{-14} cm^2 (diameter~1nm) [15]. Based on the information and the aforementioned equation, the transmission coefficient versus the electron energy is calculated and shown in Fig. 9 for the trap levels of 0.8 eV and 1.45eV. We should notice that transmission coefficient = 1 means the trap becomes "transparent" for the electrons [13]. The shallow trap with trap level = 0.8 eV is transparent for electrons with energy over 0.7 eV. The deep trap with trap level = 1.45 eV is transparent for the electrons with energy over 1.27 eV which is much larger than that with trap level = 0.7 eV. Accordingly, energetic free electrons created by BBHE tend to pass through shallow traps in the charge trapping layer and stay in deep trap sites. Consequently, the GAA Nanosheet TFT NVM programmed by the BBHE programming method reveals more satisfactory retention characteristics than does the GAA Nanosheet TFT NVM programmed by the FN programming method. However, further optimizations for the thickness and the uniformity of the tunneling oxide are necessary to improve the endurance characteristics of the GAA Nanosheet TFT NVM. The thick tunneling oxide of the GAA Nanosheet TFT NVM results in high erasing bias. The guaranteed P/E cycle of the Nanosheet TFT NVM is less than one hundred times due to the high erasing bias which stresses the non-uniform oxide in the GAA structure.

IV. CONCLUSION

A low-voltage BBHE programming method is successfully demonstrated in the GAA Nanosheet TFT NVM. The gate bias enhances the horizontal electric field in the ultra-thin channel of the GAA Nanosheet TFT NVM. Accordingly, this enlarged horizontal electric field generates energetic hot electrons that surmount the tunneling oxide easily. Therefore, the GAA Nanosheet TFT NVM can achieve low-voltage programming bias. In addition, these energetic electrons tend to pass shallow trap sites and remain in deep trap sites in the BBHE programming process. Consequently, the BBHE programming method shows better retention characteristics than does the FN programming method in the GAA Nanosheet TFT NVMs. Furthermore, this investigation examines the feasibility of the p-type GAA Nanosheet TFT NVM for future AMLCD SOP and three-dimensional layer-to-layer stacked high-density flash memory applications.

REFERENCES

[1] B. S. Doyle *et al.*, "High performance fully-depleted tri-gate CMOS transistors," *IEEE Electron Devices Lett.*, vol. 24, no. 4, pp. 263–265, Apr. 2003.
[2] B. Yu *et al.*, "FinFET scaling to 10 nm gate length," in *IEDM Tech. Dig.*, 2002, pp. 251–254.
[3] T.-C. Liao *et al.*, "Novel gate-all-around poly-Si TFTs with multiple nanowire channels," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 889–891, Aug. 2008.
[4] N. Loubet *et al.*, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," in *VLSI Tech. Dig.*, 2017, pp. T230–T231.
[5] T. M. Lee *et al.*, "Accurate performance evaluation for the horizontal nanosheet standard-cell design space beyond 7nm technology," in *IEDM Tech. Dig.*, 2017, pp. 29.3.1–29.3.4.
[6] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *IEEE Circuits Devices Mag.*, vol. 16, no. 4, pp. 22–31, Jul. 2000.
[7] K.-T. Park, D.-S. Byeon, and D.-H. Kim, "A world's first product of three-dimensional vertical NAND flash memory and beyond," in *Proc. NVMTS*, 2014, pp. 27–29.
[8] T. Ohnakado *et al.*, "Novel electron injection method using band-to-band tunneling induced hot electrons (BBHE) for flash memory with a P-channel cell," in *IEDM Tech. Dig.*, 1995, pp. 11.5.1–11.5.4.
[9] M.-T. Wu, H.-T. Lue, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, "Study of the band-to-band tunneling hot-electron (BBHE) programming characteristics of P-channel bandgap-engineered SONOS (BE-SONOS)," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 699–706, Apr. 2007.
[10] Y. Sun *et al.*, "Demonstration of memory string with stacked junctionless SONOS realized on vertical silicon nanowire," in *IEDM Tech. Dig.*, 2011, pp. 223–226.
[11] S.-C. Chen *et al.*, "A novel nanowire channel poly-Si TFT functioning as transistor and nonvolatile SONOS memory," *IEEE Electron Device Lett.*, vol. 28, no. 9, pp. 809–811, Sep. 2007.
[12] L.-C. Chen *et al.*, "The physical analysis on electrical junction of junctionless FET," *AIP Adv.*, vol. 7, no. 2, Jan. 2017, Art. no. 025301.
[13] D. J. Griffiths, *Introduction to Quantum Mechanics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 1995, ch. 2, pp. 78–82.
[14] Y. Yang and M. H. White, "Charge retention of scaled SONOS nonvolatile memory devices at elevated temperatures," *Solid-State Electron.*, vol. 44, no. 6, pp. 949–958, 2000.
[15] C.-C. Chao and M. H. White, "Characterization of charge injection and trapping in scaled SONOS/MONOS memory devices," *Solid-State Electron.*, vol. 30, no. 3, pp. 307–319, 1987.

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