Received 9 November 2018; accepted 9 December 2018. Date of publication 13 December 2018; date of current version 1 March 2019.
The review of this paper was arranged by Editor C.-M. Zetterling.

Digital Object Identifier 10.1109/JEDS.2018.2886635

Different Isolation Processes for Free-Standing GaN p-n Power Diode With Ultra-High Current Injection

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This work was supported by the Ministry of Science and Technology under Grant 105-2622-E-007-004 -CC2 and Grant 105-2218-E-007-017-.

ABSTRACT In this paper, we report on the fabrication and high performance of power p-n diodes grown on free-standing (FS) GaN substrate. The key technique to enhance the high breakdown voltage and suppress the surface leakage current is the isolation process. The mesa-structure diode is generally formed by utilizing the inductively coupled plasma reactive ion etching; however, it always induces high surface damages and thus causes a high leakage current. In this paper, we propose a planar structure by employing the oxygen ion implantation to frame the isolation region. By following the crucial process, the fabricated mesa- and planar-type diodes exhibit the turn-on voltages of 3.5 and 3.7 V, specific on-resistance ($R_{ON}A$) of 0.42 and 0.46 mΩ-cm^2, and breakdown voltage (V_B) of 2640 and 2880 V, respectively. The corresponding Baliga's figures of merit (BFOM, i.e., $V_B^2/R_{ON}A$) are 16.6 and 18 GW/cm^2, respectively. The BFOM of 18 GW/cm^2 is the highest reported value for FS-GaN diode. From the temperature dependent measurements, the planar-type diode also shows the better leakage current and thermal stability than the mesa-type diode.

INDEX TERMS GaN substrate, planar diode, implantation, leakage current, breakdown voltage, Baliga's figure of merit.

I. INTRODUCTION

Most commonly used in power generation, industrial drives or distribution system is medium voltage converters (MVC) [1]–[3]. It is limited by switching loss and low conversion efficiency for silicon device properties. Nevertheless, gallium nitride (GaN) devices provided another solution to the problem. GaN-based device is one of the most promising candidates for high-voltage, high-frequency, and high-temperature operation because of its superior material properties such as wide band-gap energy, high breakdown field, and high electron saturation velocity [4], [5]. However, the devices are generally fabricated by heteroepitaxial growth on foreign substrates such as silicon and sapphire, which are lateral structures [6], [7]. The major challenge is their high density of threading dislocations (10^8–10^{10} cm^{-2}), originating from the large differences in the lattice constants and thermal expansion coefficients in the strained heteroepitaxial growth on the foreign substrate [8]. It would cause the crucial leakage of current. For high-power device applications, to improve the quality of GaN epitaxial layers can raise the breakdown voltage (V_B) and reduce the specific on-resistance ($R_{ON}A$) by reducing the crystal defects. Thus, the homoepitaxial structure on a free-standing (FS) GaN substrate is advantageous in achieving a higher V_B and lower $R_{ON}A$ [9], [10]. FS-GaN can offer a threading dislocation density less than 10^6 cm^{-2}, which shows the promise for the fabrication of high quality vertical GaN p-n diodes [11]–[14], and provides the ultra-low leakage current, low $R_{ON}A$, and avalanche capability. Conventional GaN diodes, in spite of those grown on sapphire, silicon, SiC, and GaN bulk substrates, were fabricated by inductively coupled plasma reactive ion etching (ICP-RIE) to form the mesa structure for the isolation. Although the dielectric materials, such as Al_2O_3 or SiO_2, are usually deposited to protect

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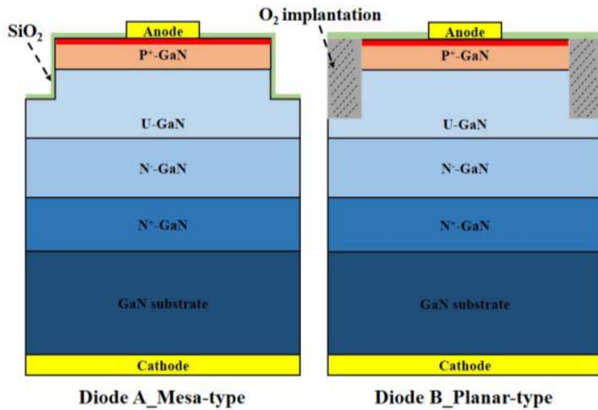

FIGURE 1. Cross sections of FS-GaN *p-n* diodes with Diode A (mesa-type) and Diode B (planar-type).

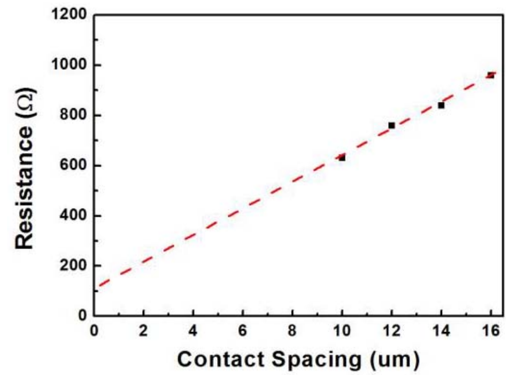

FIGURE 2. TLM analyses of ohmic contact between p-electrode and p-GaN for the diodes.

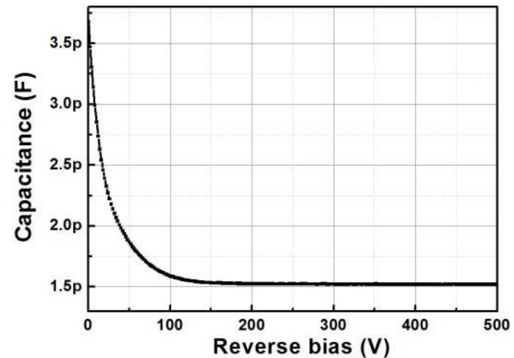

FIGURE 3. Typical capacitance versus reverse bias plot for GaN p-i-n diodes.

the etched sidewall damages, the effects of surface damages on mesa still exist. These damages of mesa would cause the current leakage and degrade the diode performance. Up to date, the best reports of the quasi-vertical GaN diodes grown on silicon and sapphire substrates have demonstrated the Baliga's figures of merit (BFOM) of 2.0 and 0.908 GW/cm^2, respectively [6], [7]. On the other hand, the vertical FS-GaN diodes have shown a record BFOM of 16.5 GW/cm^2 [11]. In this article, we exploit the ion implantation process to frame a high-resistivity amorphous region by replacing the dry etched mesa [15]. This implantation process will lead to fabricate the planar-type diode structure. Then, we further compare the characteristics of mesa- and planar-type FS-GaN diodes. The fabricated planar FS-GaN diodes will present the highest reported BFOM of 18 GW/cm^2 with an $R_{ON}A$ of 0.46 mΩ-cm^2 and V_B of 2880 V.

II. DEVICE STURCTURES AND FABRICATION

The GaN homojunction epitaxial layers were grown on a 400 μm n-type GaN substrate by metal-organic chemical vapor deposition (MOCVD). The epitaxial layers consisted of (i) a 2.0 μm n^+-type GaN layer, (ii) a 15 μm n^--type GaN layer ($n \sim 1 \times 10^{16}$ cm^{-3}), (iii) a 5 μm undoped GaN layer ($n < 1 \times 10^{16}$ cm^{-3}), (iv) a 0.5 μm p^+-GaN ($N_A \sim 1 \times 10^{18}$ cm^{-3}), and (v) a 0.03 μm p^{++}-GaN ($N_A \sim 5 \times 10^{18}$ cm^{-3}) as contact layer. The isolation of the active regions was defined by two methods of processing: One was by ICP-RIE and the other was by ion implantation. The dry etching rate is 3 nm/s. The implantation was performed by using oxygen ions with the dose concentrations of 5×10^{13}, 1×10^{14}, and 5×10^{14} cm^{-2} at the implanted energies of 50, 100, and 200 keV, respectively. The depth of isolation region was 0.5 μm measured by film thickness profile measurement (α-step) and TRIM software for simulation. After the isolation process, the anode metals Ni/Au (20/120 nm) were deposited onto p^+-GaN top layer and annealed at 550°C for 10 min in O_2 ambient to form ohmic contact. Then, a 200 nm SiO_2 film was deposited by plasma-enhanced chemical vapor deposition (PECVD) as passivation layer to smooth out the sidewall damages. Finally, Ti/Au (30/120 nm) were deposited as cathode on the substrate backside without annealing. Fig. 1 shows the cross sections of FS-GaN Diodes A and B. Diode A has a mesa structure by utilizing the ICP-RIE to form the isolation region, while Diode B has a planar structure by using ion implantation to form the isolation region. The fabricated diodes have a size of 500 x 500 μm^2 with an active-region diameter of 100 μm. The electric characteristics of forward current-voltage (I-V) and high reverse voltage (>100 V) were measured by Keysight B1505A source meter. The measured temperature range was from 300K to 425K. All measurements were performed on the Cascade Microtech Tesla probe station.

III. RESULTS AND DISCUSSION

Fig. 2 shows the contact resistance between p-electrode and p-GaN as a function of contact spacing for the diodes measured by transmission line method (TLM). The calculated transfer length (L_T) and the specific contact resistance (ρ_c) are 1.08 μm and 1.06 × 10^{-4} Ω-cm^2, respectively. All these values are good enough to ensure that the contact resistance of metal to semiconductor is negligible and all the applied voltages can effectively drop across the GaN p-i-n diode. Fig. 3 shows the typical junction capacitance

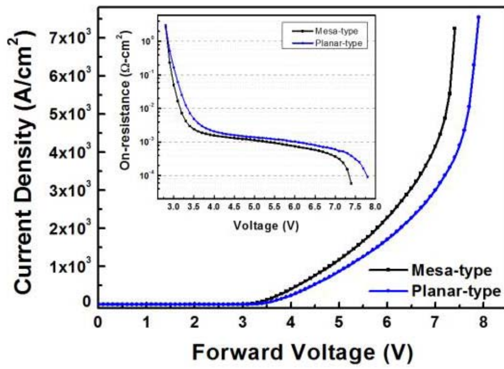

FIGURE 4. Forward electric characteristics for Diodes A and B. Inset: specific on-resistance versus forward bias for Diodes A and B.

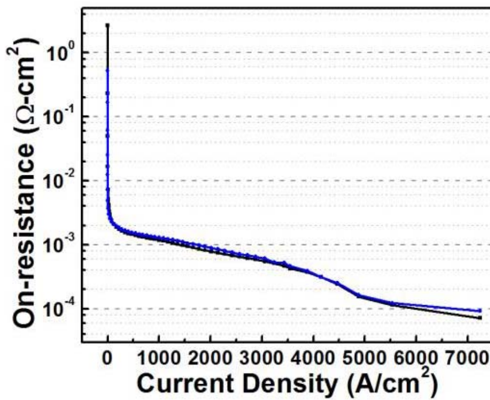

FIGURE 5. Specific on-resistance as a function of current density for Diodes A and B.

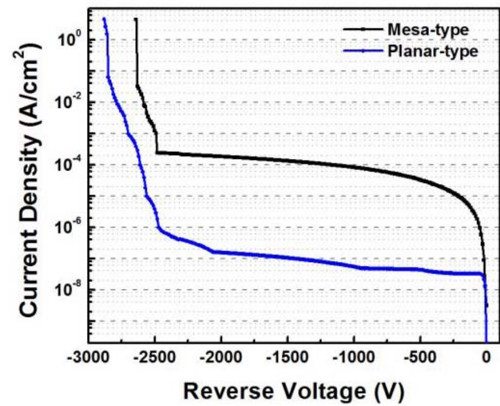

FIGURE 6. Reverse electric characteristics for Diodes A and B.

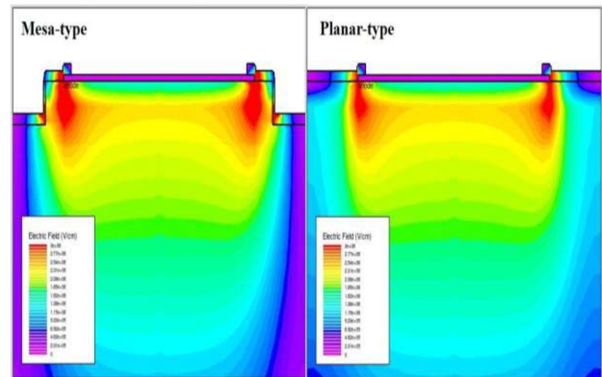

FIGURE 7. TCAD simulation of the reverse bias at −3000 V for Diodes A and B.

(C_J) as a function of reverse bias for the p-i-n diodes. When a negative bias is applied, most of the voltage drops across the drift region. The capacitance decreases with reverse bias due to the increase of depletion thickness. The double drift region, including the u-GaN and n^--GaN, can be completely depleted at the reverse voltage of −150 V. The concentration of drift region is calculated as about 3.7×10^{15} and 1.3×10^{16} cm^{-3}, respectively. It is in agreement with the designed structure.

Fig. 4 shows the current density as a function of forward bias for FS-GaN *p-n* Diodes A and B. The forward voltage (V_F) is defined as the voltage at the current density of 100 A/cm^2. Thus, the forward voltages are 3.5 and 3.7 V for Diodes A and B, respectively. The inset shows the specific on-resistance versus forward bias for Diodes A and B. The corresponding $R_{ON}A$ of Diodes A and B at the current density 3500A/cm^2 are 0.42 and 0.46 mΩ-cm^2, respectively. The ultra-low $R_{ON}A$ is attributed to the excellent epitaxial layer quality and decent ohmic contact process. Diodes A and B exhibit the extremely close of V_F and $R_{ON}A$ because the performance at forward bias is dominated by the intrinsic layer of GaN diode and the ohmic contact resistance.

Fig. 5 shows the relationship between specific on-resistance and current density under forward bias for Diodes A and B. In this study, the current density is deliberately increased for the observation of the declination of specific on-resistance. At the low current density of ∼1000 A/cm^2, the $R_{ON}A$ decreases to 1 mΩ-cm^2; while the current density exceeds 3,500 A/cm^2, the $R_{ON}A$ falls off by an order of magnitude. When the current density is over 5000 A/cm^2, Diode A has lower $R_{ON}A$ due to its higher junction temperature (as illustrated later) as compared to Diode B. Both the diodes can withstand the forward current density of over 7000 A/cm^2.

Fig. 6 shows the reverse-bias characteristics of FS-GaN Diodes A and B. The different isolation processes have obvious diversity. The mesa-type diode has actually etching damages; however, the planar-type diode has little lattice damage only. The breakdown voltages, which is defined as the voltage at the current density of 0.1 A/cm^2, are 2640 and 2880 V, respectively, for Diodes A and B. It reveals that the planar-type diode has much lower reverse leakage current. The excellent reverse bias characteristic is mainly attributed to the improvement of isolation process and SiO_2 passivation layer. The corresponding Baliga's figures of merit (BFOM, $V_B^2/R_{ON}A$) of FS-GaN Diodes A and B are 16.6 and 18 GW/cm^2, respectively. It is admirable that the high V_B and low $R_{ON}A$ of Diode B accomplish the record high

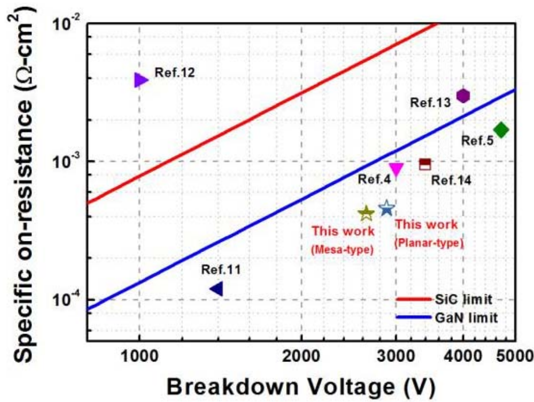

FIGURE 8. Specific on-resistance versus breakdown voltage plot of FS-GaN p-n diodes demonstrated in this work and the ones in previous reports.

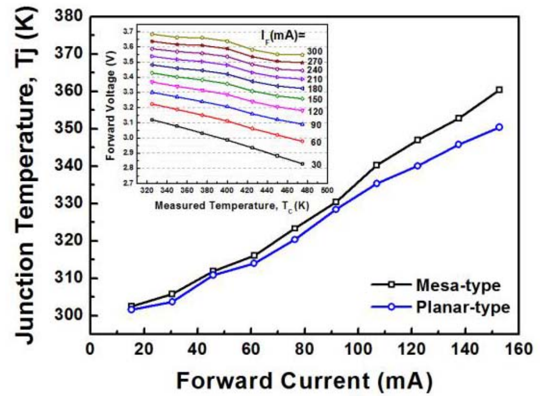

FIGURE 9. Junction temperature versus forward current plot by pulsed operation for Diodes A and B. Inset: Forward voltage as a function of measured temperature at different forward currents.

BFOM of 18 GW/cm^2, which is higher than the previous report of 16.5 GW/cm^2 [11].

Fig. 7 shows the electric field simulation for both Diodes A and B under the reverse bias of -3000 V. In addition to the higher electric field located below the p-electrode, the Diode B shows relatively uniform electric field than Diode A which presents the electric crowding near the etching mesa corner. Under the low reverse bias (< -100 V), there is no significant difference; however, if the reverse bias is further increased (> -600 V), the edge with high electrical field is easy to generate leakage current and cause the diode breakdown.

Fig. 8 shows the specific on-resistance as a function of breakdown voltage for comparison of the BFOM of FS-GaN *p-n* diodes in the previous works [4], [5], [11]–[14]. The result of Diode B with planar structure is also marked on this BFOM plot.

Beside the mentioned high current operation, the thermal stability measurement is another issue of these devices. Fig. 9 shows the junction temperature as a function of forward current by pulsed operation for Diodes A and B. The used pulse width was 100 μs and duty cycle was 0.5%. Inspection of Fig. 9 reveals the junction temperature of Diode A is slightly higher than that of Diode B at low forward currents, while the difference of junction temperature for both the diodes becomes larger at high forward currents [16]. The higher junction temperature of Diode A leads to the lower $R_{ON}A$, as shown in inset of Fig. 2. The inset of Fig. 9 shows the forward voltage as a function of measured temperature at different forward currents. At the injection current of 150 mA, the juction temperature for Diodes A and B is 360K and 350K, respectively. It means the heat dissipation of the GaN substrate can be expected.

Fig. 10 shows the leakage current as a function of reverse voltage for Diodes A and B measured in the temperature range of 300K-425K. The leakage current increases with temperature. Besides, the leakage current increases rapidly with reverse voltage for Diode A, while it increases slowly for Diode B. The activation energies are calculated as 0.46 and 0.31 eV for Diodes A and B, respectively [17]. The higher leakage current induces the greater activation energy. For the Diode B, the lower reverse leakage current echoes the higher breakdown voltage, as shown in Fig. 4. Hence, it is confirmed that the planar-type diode has much more suitable to the applications of high current operation and low reverse leakage current than the mesa-type diode.

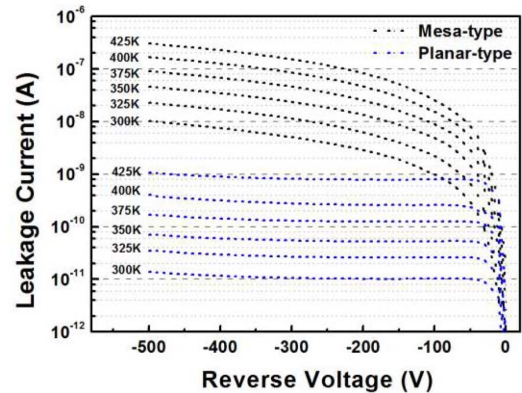

FIGURE 10. Leakage current as a function of reverse voltage for Diodes A and B measured at different temperatures.

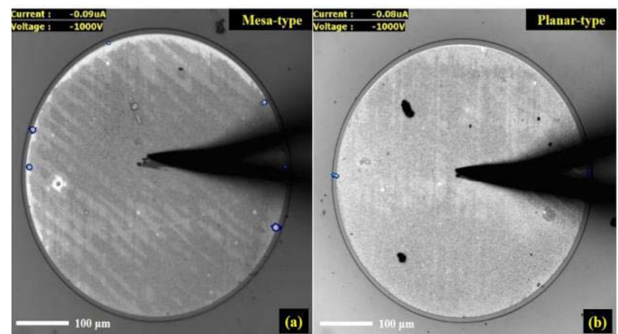

FIGURE 11. Images (a) and (b) of emission microscopy (EMMI) for Diodes A and B, respectively.

Figs. 11(a) and 11(b) show the images of emission microscopy (EMMI), which is one of the common methods of fault analyses. By illumination, the PN diodes under reverse bias have electron-hole pair recombination. The photons generated at this time will be detected by high-sensitivity CCD, and it can position the area of leakage current. As shown in Fig. 11(a), Diode A has 6 low-light bright spots at the reverse bias of -1000 V; while Diode B has only 2 low-light bright spots in Fig. 11(b). These areas mean the positions of leakage current paths. The leakage path of the diode is consistent with above discussion of leakage current and breakdown voltage.

IV. CONCLUSION

We have successfully fabricated the FS-GaN diodes with different isolation processes. One utilizes the ICP-RIE to form the mesa structure in Diode A, the other employs ion implantation to form the planar structure in Diode B. Both the diodes have a low specific on-resistance of ∼0.4 mΩ-cm^2 and withstand a forward current density of over 7000 A/cm^2. However, the planar-type diode exhibits a much lower leakage current of ∼10 pA at 300K and a high breakdown voltage of over 2880 V, achieving the highest BFOM of 18 GW/cm^2 so far. The junction temperature and activation energy can be further investigated by temperature-dependent I-V measurements. Besides, the leakage current path is confirmed by the EMMI analyses. All evidences reveal that the planar-type diode has better electric characteristics and thermal stability than the mesa-type diode.

REFERENCES

[1] S. X. Du, B. Wu, and N. R. Zargari, "Delta-channel modular multilevel converter for a variable-speed motor drive application," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6131–6139, Aug. 2018.
[2] Q. Song, B. Zhao, J. U. Li, and W. H. Liu, "An improved DC solid state transformer based on switched capacitor and multiple-phase-shift shoot-through modulation for integration of LVDC energy storage system and MVDC distribution grid," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6719–6729, Aug. 2018.
[3] S. X. Du, B. Wu, and N. R. Zargari, "Common-mode voltage elimination for variable-speed motor drive based on flying-capacitor modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5621–5628, Jul. 2018.
[4] Y. Hatakeyama *et al.*, "High-breakdown-voltage and low-specific-on-resistance GaN P–N junction diodes on free-standing GaN substrates fabricated through low-damage field-plate process," *Jpn. J. Appl. Phys.*, vol. 52, no. 2, pp. 1–3, Feb. 2013.
[5] H. Ohta *et al.*, "Vertical GaN P–N junction diodes with high breakdown voltages over 4 kV," *IEEE Electron Device Lett.*, vol. 36, no. 11, pp. 1180–1182, Nov. 2015.
[6] R. A. Khadar *et al.*, "820-V GaN-on-Si Quasi-vertical P–I–N diodes with BFOM of 2.0 GW/cm^2," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 401–404, Mar. 2018.
[7] Y.-F. Chang *et al.*, "Using two-step mesa to prevent the effects of sidewall defects on the GaN P–I–N diodes," *IEEE J. Quantum Electron.*, vol. 51, no. 10, pp. 1–6, Oct. 2015.
[8] T. Hino *et al.*, "Characterization of threading dislocations in GaN epitaxial layers," *Appl. Phys. Lett.*, vol. 76, no. 23, pp. 3421–3423, 2000.
[9] T. Sochacki *et al.*, "Preparation of free-standing GaN substrates from GaN layers crystallized by hydride vapor phase epitaxy on ammonothermal GaN seeds," *Jpn. J. Appl. Phys.*, vol. 53, no. 5, pp. 1–5, 2014.
[10] S. Woo *et al.*, "Novel in situ self-separation of a 2 in. Free-standing m-plane GaN wafer from an m-plane sapphire substrate by HCl chemical reaction etching in hydride vapor-phase epitaxy," *Crystengcomm.*, vol. 18, no. 40, pp. 7690–7695, 2016.
[11] Z. Hu *et al.*, "Near unity ideality factor and Shockley–Read–Hall lifetime in GaN-on-GaN P–N diodes with avalanche breakdown," *Appl. Phys. Lett.*, vol. 107, no. 24, pp. 1–5, Dec 2015.
[12] Z. Y. Hu *et al.*, "1.1-kV vertical GaN P–N diodes with p-GaN regrown by molecular beam epitaxy," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1071–1074, Aug. 2017.
[13] I. C. Kizilyalli, T. Prunty, and O. Aktas, "4-kV and 2.8-mΩ-cm^2 vertical GaN P–N diodes with low leakage currents," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1073–1075, Oct. 2015.
[14] K. Nomoto *et al.*, "GaN-on-GaN P–N power diodes with 3.48 kV and 0.95 mΩcm^2: A record high figure-of-merit of 12.8 GW/cm," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2015, pp. 9.7.1–9.7.4.
[15] J.-Y. Shiu *et al.*, "Oxygen ion implantation isolation planar process for AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 28, no. 6, pp. 476–478, Jun. 2007.
[16] Y. Xi and E. F. Schubert, "Junction-temperature measurement in GaN ultraviolet light-emitting diodes using diode forward voltage method," *Appl. Phys. Lett.*, vol. 85, no. 12, pp. 2163–2165, 2004.
[17] T.-T. Kao *et al.*, "Temperature-dependent characteristics of GaN homojunction rectifiers," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2679–2683, Aug. 2015.

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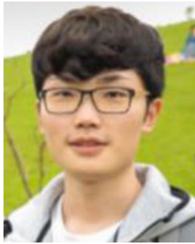

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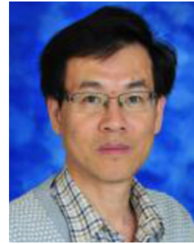

MENG-CHYI WU (SM'03) received the Ph.D. degree in electrical engineering from National Cheng Kung University, Taiwan, in 1986. He has over 30 years of research experience on III-V compound semiconductors, material characterization, optoelectronic devices, and epitaxial techniques consisting of liquid-phase epitaxy, metalorganic chemical vapour deposition (MOCVD), and molecular-beam epitaxy. He is the first one to fabricate the red AlGaAs/InGaP light-emitting diodes in Taiwan, which helps the development of visible LEDs grown by MOCVD. He also fabricated the long-wavelength InGaAsP/InP and AlGaInAs/InP laser diodes, which contain ridge-waveguide, distributed feedback, and vertical surface-emitting structures, for the fiber communication applications. He also fabricated the first InGaAs/InP and InGaP/GaAs p-i-n photodiodes (PDs) with high speed (10 GHz) and enhanced wide spectral range of 0.6–1.7 um and 300–900 nm, respectively. The PDs permit the applications for high-speed communication, optical storage systems such as CD-ROM, and red and blue laser DVDs. He also applied this p-i-n photodiode to integrate the ruby micro-ball-lens for the alignment tolerance enhancement. He has also developed micro-LEDs, vertical organic thin-film transistors and transparent conductive oxides for the applications on the optoelectronic devices and displays. He has published over 300 journal papers in the above areas.