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A Reliable Technology for Advanced SiC-MOS Devices Based on Fabrication of High Quality Silicon Oxide Layers by Converting a-Si

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ABSTRACT An alternative technological approach is proposed to obtain a SiO_2 film on SiC using processes that finally reduce the effective fabrication costs. Accordingly, we report achieving of a high-quality oxide on 4H-SiC substrate using a process flow that consists in a preliminary deposition by sputtering, at room temperature, of an amorphous Si thin layer, followed by its oxidation at a relative low temperature (1100 °C) for SiC MOS technology. The X-ray reflectivity measurements demonstrated that the resulted oxide has a comparable roughness with the one thermally grown and presents the advantage of an almost threefold thinner interfacial layer. The improvement of the oxide/semiconductor interface was further validated by the electrical investigation of the fabricated MOS structures, where a significant diminishing of the effective oxide charge density, interface traps density, and near interface oxide traps density was assessed. Thus, we demonstrated that, for a specified thickness of the oxide layer on SiC, the proposed technological flow not only significantly reduces the standard duration of the process necessary and consequently the associated fabrication cost, but, more important, leads to superior oxides and interfaces, in terms of both micro-physical and electrical properties.

INDEX TERMS Interface traps, MOS, near interface oxide traps, oxidized amorphous silicon, SiC.

I. INTRODUCTION

Fabrication of a very stable MOS device for harsh environment applications represents a real challenge, mainly because even obtaining a high-quality silicon dioxide (SiO_2) on silicon carbide (SiC) substrate is not a trivial step [1]. Thus, albeit the SiC based technology is expensive in comparison with the standard silicon (Si) one, when the devices' final applications are primarily related to industrial processes, where high temperatures, corrosion and hydrogen leakages are involved, the substrate material characteristics (i.e., wide band gap, low dielectric constant, high breakdown voltage, good thermal conductivity and chemical stability in reactive environments) makes SiC far superior to Si, and, consequently, development of reliable, cost-effective fabrication technology on SiC represents a necessity [2]. The oxide growth process represents a significant part from the general fabrication cost, usually increased by the special requirements of elevated temperatures and long reaction times, encountering also important associated drawbacks related to the film quality. Accordingly, the standard method for reaching high-quality SiO_2 films is based on thermal oxidation, but fabrication of thicker films entails time consuming processes at high temperatures (up to 1400 °C), from several minutes for few nm to hours for tens of nm of oxide. Increasing the process time leads, on the one hand, to high costs, and, on the other hand, to a large number of electrical defects at the SiO_2/SiC interface and an inevitable induced stress [3], [4]. It has been showed that the grown oxides on SiC present a very poor SiO_2/SiC interface [5], [6], with a high value of the traps density, usually with almost two orders of magnitude higher than the one reported for the standard SiO_2/Si interface [4]. These unwanted effects concerning the SiC thermal oxidation reverberate in high values of effective oxide charges (Q_{eff}), interface traps density (D_{it}) and near interface oxide traps density (D_{NIOTs}), respectively. The values might be improved above the threshold

temperature of 1100 °C, which corresponds to the softening temperature of a grown SiO_2 on SiC [7]. Moreover, different post-oxidation annealing (POA) treatments have been subsequently proposed based on incorporation of nitrogen [8], phosphorous [9], [10] or boron [11] atoms due to their beneficial role in passivation of the oxide defects and interface traps. Otherwise, in order to reduce the SiC oxidation time, a two steps process for obtaining the SiO_2 layer was proposed. This method consists in an initial deposition of a polysilicon thin film by chemical vapor deposition (CVD) technique, at temperatures ranging from 550 to 750 °C [12]–[14], further subjected to a thermal oxidation. However, the film roughness and the interface traps remained critical issues to be solved, because they lead to serious instabilities of the threshold voltage and also affect the mobility in the case of a MOS field effect transistor [15], [16]. Recently, we have successfully replaced the CVD polysilicon with an amorphous silicon (a-Si) deposited by sputtering at room temperature [17], achieving a higher oxidation rate compared to SiC dry oxidation, which could significantly diminish the effective cost for the SiC MOS processing. Herein, we explore the capability of obtaining different thicknesses of MOS oxides on 4H-SiC starting from a-Si thin films, and also, we perform an in-depth investigation of their quality, focused on the evaluation of the SiO_2/SiC interface, in terms of microphysical properties, including estimation of the interfacial layer of silicon oxycarbides (SiO_xC_y) and the resulted oxide roughness, as well as electrical properties, assessment of the interface charges that influence the stability of the fabricated SiC MOS capacitors, including Q_{eff}, D_{it} and D_{NIOTs}. Accordingly, we demonstrate that the drawback related to the high roughness of the obtained oxides via polysilicon encountered up to now is overcome. Regarding the interface charges, the trap densities estimated for the resulted oxides around 14 nm thickness were three times reduced compared to thermally grown oxide, fairly similar with the values reported when additional POA processes were used. This trend is preserved when thicker a-Si films were deposited, obtaining high-quality oxide layers of around 30 nm and 40 nm, respectively. Besides, the doping profile and the net charge density distribution in depletion region further confirmed the advantage of using the proposed technology for fabrication of SiC MOS devices.

II. FABRICATION OF THE SIC MOS CAPACITORS

The SiC MOS capacitor test structures were fabricated on n type, 4° off (11-20) oriented, 4 inches Si face 4H-SiC wafers with a 5 μm thick epi-layer doped with 10^{16} cm^{-3} of nitrogen, purchased from Dongguan Tianyu Semiconductor Technology Co. The wafers were firstly degreased for 5 min in acetone and methanol, followed by a soak in "Piranha" solution (H_2SO_4: H_2O_2 – 3:1 v/v) at 130 °C for 15 min and a rinse in deionized water (DIW). The resulted oxide was etched in buffered hydrofluoric acid (BHF 5 %) for 5 min. Finally, the wafers have been rinsed in DIW and blown dry in N_2. After the cleaning procedure, two batches of MOS capacitors have been fabricated in parallel using two alternative technological approaches to obtain the MOS oxide. Accordingly, the gate oxide of the first batch was fabricated using the standard process, a dry oxidation in pure oxygen at 1100 °C for 2 h, and the test structures were noted as **AO** (as-oxidized). For the second batch, the technological process flow consisted of the preliminary deposition by sputtering of three different thicknesses of a-Si (5, 10 and 15 nm) on 4H-SiC substrate using the DC Edwards BOC 500 system (temperature of 21 °C, power of 100 W and deposition rate of 0.1 nm/s) followed by dry oxidation in pure oxygen at 1100 °C, the structures being noted as **a-Si-5**, **a-Si-10**, **a-Si-15**, respectively. The oxidation time was settled at 30 min to assure, on the one hand, the complete oxidation of the a-Si films, and, on the other hand, to allow formation of an ultra-thin oxide layer originating from SiC substrate (i.e., consuming SiC) in order to obtain a robust interface with the substrate. Also, we had in mind to obtain, following this process flow, an oxide thickness close to the thermally grown one. Thus, after several iterations we found that a 30 min oxidation time of the sample with 5 nm a-Si film deposited on SiC led to about 14 nm of oxide (**a-Si-5** sample), fairly close to the **AO** sample. In the case of **a-Si-10** and **a-Si-15** samples, approximately 30 nm and 40 nm oxide layers were obtained.

In order to test the electrical characteristics and stability of the resulted oxide layers, a metallic sandwich - Cr (30 nm) / Au (100 nm) - was evaporated on the both sides of wafers to fabricate the gate and backside electrodes, respectively. The metallization has been performed after a preliminary removal of the native oxide using a wet etching process in BHF 5 %, followed by a soak in deionized water and blown dry in N_2. This metallic sandwich was used to endure the long-term operation of the packaged SiC MOS devices. In view of that, the Au top layer assures a good wire bonding (gold wires were used as outside electric leads), while the Cr bottom layer guarantees the good interface and adhesion between the oxide and the Au layer. Using standard photolithography and wet etching processes, MOS capacitors with 1 mm^2 area gate electrodes were fabricated.

III. MICROPHYSICAL CHARACTERIZATION USING XRR MEASUREMENTS

In order to obtain information about the structural and compositional properties of the resulted oxide layers, X-Ray reflectivity (XRR) measurements were performed on a Rigaku SmartLab diffractometer employing CuK_α radiation. Reflectivity curves were measured in the range $2\theta/\omega = 0 - 10$ ° with a step width of 0.001 ° and a scan rate equal to 0.2 °/min using a high-resolution set-up with a divergent height limiting slit equal to 5 mm. The incident and receiving slits are equal to 0.2 mm. The XRR results obtained for the fabricated samples were simulated with the parallel tempering algorithm of the GlobalFit integrated thin film analysis software, using two approaches: (i) the single

layer model considering a sharp border between the substrate and oxide, without an interfacial layer (IL) (*w/o IL*); and (ii) the two-layer model, where an interfacial layer of silicon oxycarbides (SiO_xC_y) is taken into account between SiO_2 and SiC (*w/ IL*) [18]. For each sample, the simulated curves obtained using the both fitting models are showed comparatively with the experimental ones in Fig. 1, together with the fitted parameters (i.e., oxide thickness, density, roughness) and the corresponding standard deviation of the overall fits (R, χ^2), which are summarized in the inserted tables. As it can be observed, in comparison with the simulated intensities obtained using the single layer model, the two layers model leads to a visible improvement and a better agreement with the experimental data, especially for the thicker oxide films. The visual inspection is confirmed by the values obtained for R and χ^2, which are smaller when the *w/ IL* model is used for all samples. Therefore, it is notable that analyzing the samples where the oxide layer has similar total thickness, **AO** and **a-Si-5**, the interfacial layer is almost three-fold smaller in the case of **a-Si-5** one, becoming thinner than 1 nm, comparable with other results reported in [19]. The high IL width obtained for **AO** sample (2.77 nm) might indicate a large number of SiO_xC_y species at the oxide/SiC interface. These carbonaceous compounds originate from SiC substrate due to the kinetically incomplete removal of the volatile CO molecules formed during the thermal oxidation process [20], [21] and they determine the presence of the interfacial oxide traps [22], [23]. Afanasev *et al.* showed that the energy distribution of the interface states over the SiC energy band gap is determined by the carbon clusters which are formed during the thermal oxidation at SiO_2/SiC interface, either graphene-like or sp^2-bonded carbon atoms, and also, by the oxygen related defects from the SiO_2 layer [24]–[26]. Thus, the SiO_xC_y layer appearing at the SiO_2/SiC interface (transition layer) is the main source of interface traps, contributing to both near interface oxide traps and interface traps density, and leads to critical aspects regarding the electrical behavior of the fabricated SiC MOS devices [27]–[29]. Most often, to overcome this problem, additional POA processes are necessary.

In the view of these evidences, having approximately the same thickness of the total MOS oxide (including here and the interfacial layers), 14.04 nm in the case of **AO** sample and 14.31 nm for **a-Si-5**, respectively, the oxide structure analysis indicates that the **a-Si-5** sample should present superior electrical performances regarding the stability of the oxide/semiconductor interface.

It is even more encouraging that the similar analyses performed for **a-Si-10** and **a-Si-15** samples, where thicker MOS oxide layers were designed, 29.56 nm and 39.74 nm, respectively, the thicknesses of the interfacial layers were 1.84 nm for **a-Si-10** and 1.11 nm for **a-Si-15**, respectively. Hence, the two steps oxidation process using an initial a-Si layer assures the presence of a relative small interfacial layer, considerable below the one calculated for the **AO** sample. The cause is probably the four times shortened thermal oxidation where,

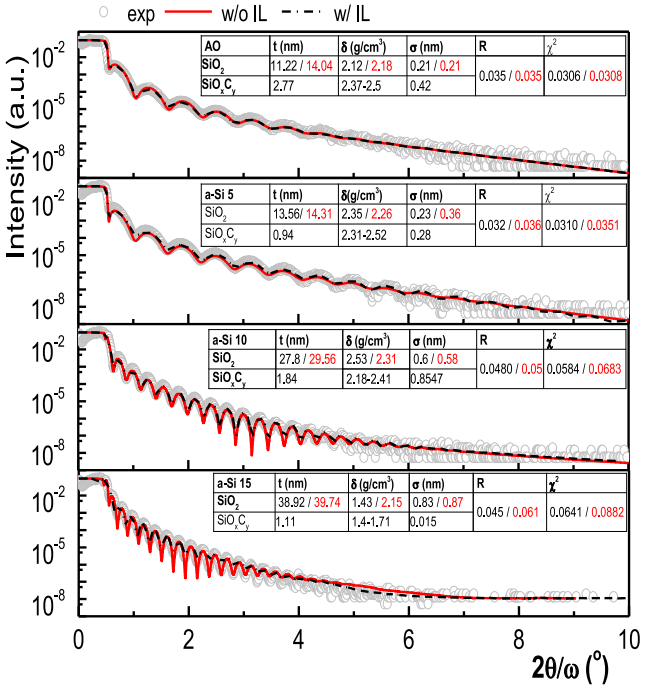

FIGURE 1. XRR analysis results (grey dot plots – experimental data; red plots – simulated intensities by single layer model; black dash-dot plots - simulated intensities by two-layer model).

in fact, two concomitant processes are taking place: oxidation of the a-Si layer and growing of a thin film of oxide, directly through SiC oxidation and which implies overall removal of a diminished amount of C atoms from substrate than in the case of **AO** sample during the oxide layer growth.

However, besides the interfacial layer, a roughness of both oxide surface and oxide/SiC interface can generate tunneling phenomena at low electric fields, caused by the trapped electrons near interface [30]. In this view, whereas substantial roughness of the both surface and oxide/semiconductor interface was reported for the polyoxides obtained via oxidation of a polysilicon thin film deposited at temperature above 650 °C, when the polysilicon was deposited as an amorphous phase (at a temperature of 560 °C), a smoother interface and a current with two orders of magnitude lower have been obtained, leading to a serious improvement of the electrical properties for the obtained polyoxides [31], [32]. Regarding the polyoxides obtained via oxidation of a polysilicon thin film deposited at temperatures above 650 °C by CVD technique, in order to decrease the roughness of the both surface and oxide/semiconductor interface, an additional treatment, like NF_3 annealing [33], was generally used. Therefore, an essential benefit offered by our technological approach is that oxidizing the a-Si layer deposited at the ambient temperature leads to reduced values for roughness. In our case, when the roughness of the oxide layers with similar thicknesses is analyzed, i.e., **AO** and **a-Si-5** samples, it is notable that albeit initially the a-Si was deposited by sputtering at ambient temperature, the resulted oxide layer has very good roughness,

comparable with the one obtained for the standard thermally grown MOS oxide, in the range of 0.22–0.23 nm. The fabricated samples with a thicker MOS oxide show a slightly rougher surface, $\sigma_{ox} = 0.58$ nm for **a-Si-10** sample and $\sigma_{ox} = 0.87$ nm for **a-Si-15** one.

Using the fitting results, the mass density profiles across the transition region were further calculated [19], [34] for the samples with closest oxide thicknesses, **AO** and **a-Si-5**, and the variation of the interface layers densities on the entire region between SiO_2 film and 4H-SiC is presented in Fig. 2.

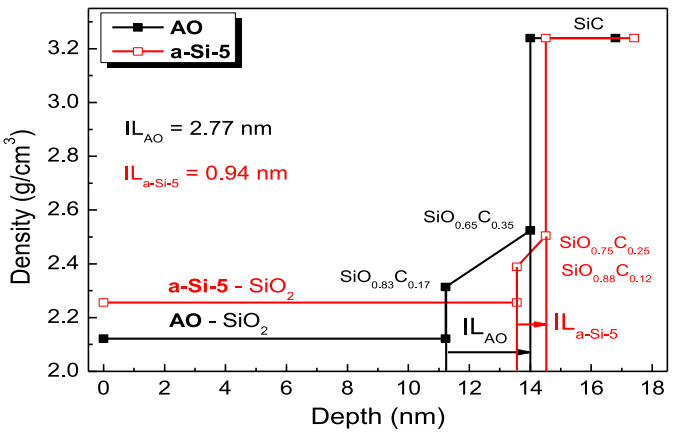

FIGURE 2. **In depth analysis of the density variation for both AO and a-Si-5 samples.**

As it can be observed, on the one hand, the oxide layer obtained via a-Si conversion is slightly denser (2.25 g/cm^3) than the classic one, thermally grown (2.12 g/cm^3). On the other hand, although both samples have approximately the same thickness of oxide, the quality of their interface with 4H-SiC substrate is different, more abrupt in the case of **a-Si-5** sample. Moreover, the stoichiometry of each oxycarbide compounds, calculated using the Vegard law, leads to a steeper slope for **a-Si-5** in comparison with the **AO** one and also to a reduced amount of carbon atoms at the SiO_2/SiC interface. These results indicate clearly that the a-Si layer was successfully converted into an oxide film with superior structural and chemical composition even comparing with the thermally grown one. For a better illustration of the SiO_2/SiC interface, a schematic cross-section view for the obtained oxide in the case of both **AO** and **a-Si-5** samples is shown in Fig. 3.

Accordingly, although both samples have approximately the same total thickness of the oxide, the interface layers have different values, indicating less C atoms at the SiO_2/SiC interface for the **a-Si-5** sample and consequently less electrical defects for the fabricated SiC MOS capacitors, which then assure an improved stability [22], [23].

IV. ELECTRICAL CHARACTERIZATION

The electrical properties of the resulted oxides were analyzed using a Keithley 4200-CVU semiconductor characterization

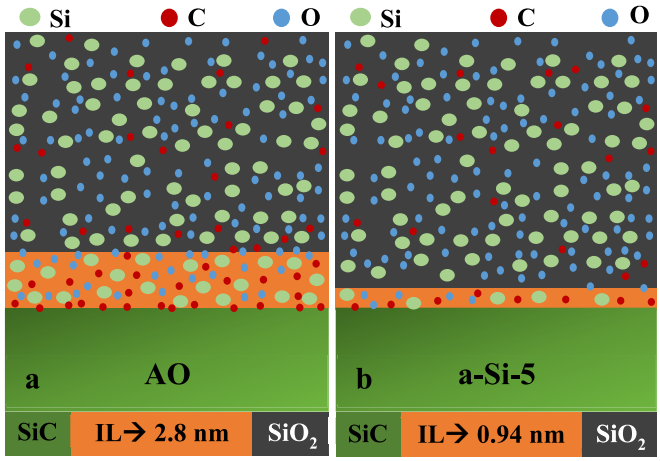

FIGURE 3. **Schematic cross-section view for the SiO_2/SiC interface layer in the case of: a) AO sample; b) a-Si-5 sample.**

system. The devices studied by taking three samples from each batch (i.e., **AO**, **a-Si-5**, **a-Si-10**, **a-Si-15**) exhibited similar qualitative C-V characteristics with minor deviation in the quantitative values. However, three sets of measurements were taken for each set of devices and the triplicate C-V data were averaged to get a mean value.

Using the results from XRR measurements regarding the oxides thickness, the relative permittivity (ε_r) of MOS oxides with similar thicknesses (**AO** and **a-Si-5** samples) have been determined from the maximum accumulation capacitance as follows:

$$C_{ox} = \varepsilon_0 \varepsilon_r \frac{S}{t_{ox}} \tag{1}$$

where C_{ox} is the oxide capacitance from accumulation regime, ε_0 is the vacuum permittivity, S is the active area and t_{ox} is the oxide thickness.

Accordingly, for the standard thermally grown oxide on SiC (**AO** sample) a value of 3.62 has been obtained, lower than the ideal one for the standard SiO_2 (3.9), which can be due to the reduced density of SiO_2, as it can be observed in Fig. 2. When the SiO_2 layer was obtained via oxidation of amorphous silicon (**a-Si-5** sample), a denser oxide was obtained, and the corresponding relative permittivity becomes very close to the ideal one, 3.88. The results are in very good agreement with the work of Hosoi *et al.* [35].

In Fig. 4 are presented the preliminary C-V curves recorded by biasing the fabricated SiC MOS capacitors from accumulation to deep depletion in order to determine the flat band voltage. The deviation of the C-V curves from the ideal characteristic is principally caused by the presence of the oxide charges, as well as the interface traps and the near interface oxide traps. The effective oxide charge (Q_{eff}) can be estimated based on the deviation of the flat band voltage from the ideal value when the test samples are biased from strong accumulation to deep depletion [36], using the

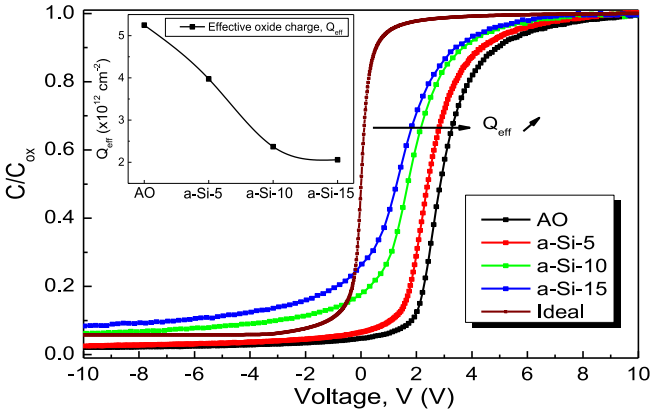

FIGURE 4. **C-V characteristics obtained by biasing the fabricated SiC MOS capacitors from accumulation to deep depletion; inset - Effective oxide charge density for the fabricated SiC MOS capacitors.**

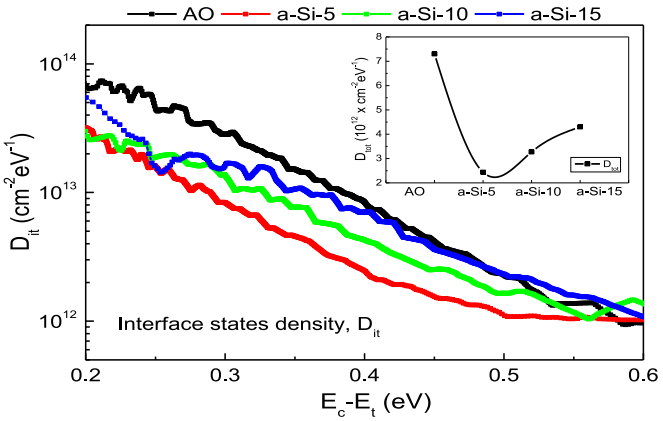

FIGURE 5. **Distribution of interface trap densities (D_{it}) evaluated with Terman method.**

equation:

$$Q_{eff} = \frac{\Delta V_{FB} C_{ox}}{qS} \tag{2}$$

where C_{ox}, q and S are the oxide capacitance, electronic charge and gate area, respectively.

The ideal flat band voltage has been determined from the ideal C-V curve calculated starting from the Poisson equation [36]; both the ideal and experimental flat band voltage values have been determined using the $1/C^2$ *vs.* V plots [37]. The resulted Q_{eff} values varies between 2.05 and 5.25 $\times$ 10^{12} cm^{-2}, and it is notable that the highest value was obtained for the standard grown oxide (**AO** sample). As it can be observed in the inset graph, at least 20 % reduction was achieved for the **a-Si-5** sample with comparable thickness of oxide. As the thickness of the a-Si deposited on SiC increases from 5 to 15 nm, a significant (two-fold) diminishing of Q_{eff} is observed, which can be attributed to the negative-charged trap density reduction at the SiO_2/SiC interface.

The slow traps densities at SiO_2/SiC interface and their distribution on energy levels between 0.2 eV and 0.6 eV in SiC band gap were further estimated using the Terman method [38], analyzing the experimental high-frequency C-V characteristics in comparison with the ideal C-V one. The energy level range of the D_{it} profile is set below the flat-band potential, $E_g/2 - \Phi_B$ (bulk potential), $\sim$ 0.2 eV for 4H-SiC at room temperature, being more accurate to assess in depletion mode [39]. The interface states density distribution is affected by the gate bias, causing a stretch-out of the experimental C-V curve which characterizes the surface potential variation with applied voltage ($d\Psi_s/dV$), allowing quantification of the D_{it} as follows [36]:

$$D_{it} = \frac{C_{ox}}{Sq}\left[\left(\frac{d\Psi_s}{dV}\right)^{-1} - 1\right] - C(\Psi_s) \tag{3}$$

where: C_{ox} is the oxide capacitance, S is the active area, q is the electronic charge, Ψ_s is the surface potential (band bending) – determined using the Berglund integral [40], [41]:

$$\Psi_s = \int_{V_{G1}}^{Vacc}\left(1 - \frac{C(V)_{QS}}{C_{ox}}\right)dV + \Psi_{s0} \tag{4}$$

where Ψ_{s0} is an integration constant given by the surface potential at a gate voltage (V_{G1}) from depletion regime of the investigated SiC MOS capacitor. The Ψ_{s0} value is determined with the intercept of the linear fit of the ($1/C^2 - 1/C_{ox}^2$) *vs.* Ψ_s plot [42] and it was estimated accordingly for the investigated structures.

The resulted D_{it} distribution on energy levels between 0.2 eV and 0.6 eV in SiC band gap for the fabricated SiC MOS capacitors is plotted in Fig. 5.

As it can be seen, the D_{it} values are between $10^{13} - 10^{14}$ $cm^{-2}eV^{-1}$ for the energy levels situated near the SiC conduction band and decrease to 10^{12} cm^{-2} eV^{-1} when they are deeper inside the gap for all the SiC MOS capacitors. Whereas the highest values of D_{it} are obtained for the **AO** sample on the energy levels, the **a-Si-5** sample presents lowest values on the entire energy range in the SiC band gap. Regarding the **a-Si-10** and **a-Si-15** samples, they exhibit a slight increase in D_{it} in comparison with **a-Si-5**, mostly due to the higher thickness of the oxides [43]. The total interface trap densities (D_{tot}) were calculated integrating the D_{it} values over the entire energy levels range (0.2 – 0.6 eV) [44]:

$$D_{tot} = \int_{0.2\ eV}^{0.6\ eV} D_{it}(E_c - E_t)d(E_c - E_t) \tag{5}$$

where, E_c and E_t are the energies of the conduction band and the interface traps, respectively.

Following the calculations, a total density of $\sim$ 7.3 $\times$ 10^{12} cm^{-2} eV^{-1} was obtained for the **AO** sample, which is more than three times higher than the one corresponding to **a-Si-5** sample ($\sim$ 2.4 $\times$ 10^{12} cm^{-2} eV^{-1}). Reduced values were obtained for **a-Si-10** (3.27 $\times$ 10^{12} cm^{-2} eV^{-1}) and **a-Si-15** samples (4.3 $\times$ 10^{12} cm^{-2} eV^{-1}), respectively - inset of Fig. 5.

Next, we investigated the near interface oxide traps with long time constant using high frequency (1 MHz) cycle capacitance-voltage (C-V) measurements, where the MOS capacitors are biased from depletion (V_{G1}) to strong accumulation (V_{acc}), successively increasing the start voltage at each approximately 0.05 V increment in surface potential [45], [46]. Accordingly, we firstly calculated the surface potential variation as a function of the gate voltage, from depletion to strong accumulation, based on the C-V characteristics (Fig. 6), taking into account the quantum confinement effect due to the Fermi level crossing of the SiC conduction band. Thus, when the capacitors are biased in strong accumulation, a very high electric field is produced and the electrons are captured by the traps located at energy levels above the SiC conduction band [47]. Comparing these data, we found that the surface potential presents a similar dependence on the starting voltage for the experimental SiC MOS capacitors, increasing gradually until it reaches a saturation regime, when all the traps are filled with electrons. In general, a lower variation for the surface potential corresponds to a higher amount of trap density at SiO_2/SiC interface [48].

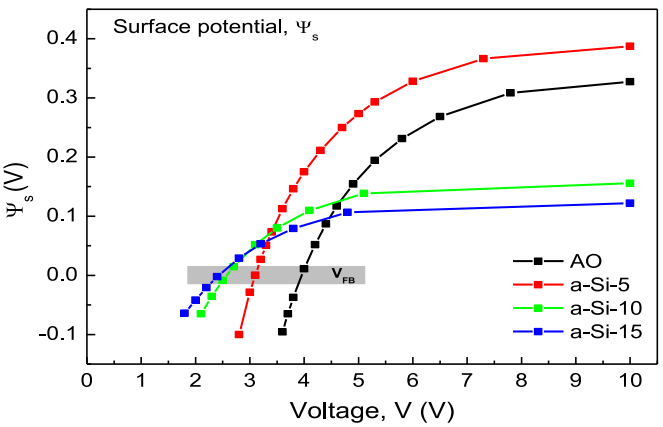

FIGURE 6. Surface potential variation from depletion to strong accumulation for experimental SiC MOS capacitors, highlighting the flat band voltages when the surface potential reaches the zero value.

The quantification of the D_{NIOTs} and their corresponding energy levels in SiC band gap was realized based on successive C-V characteristics performed from accumulation to deep depletion, starting from different gate voltages, previously calculated for approximately every 0.05 V increment in surface potential (Fig. 7).

The positive shifts observed starting from depletion to accumulation regions indicate the presence of electrons captured by the acceptor like deep interface states during the biasing in strong accumulation [9].

The resulted flat band voltage as a function of surface potential are plotted in Fig. 8 and a progressive decrease can be observed from the **AO** to **a-Si-5**, **−10**, and **−15** samples, respectively, indicating a reduction of the effective negative oxide charge.

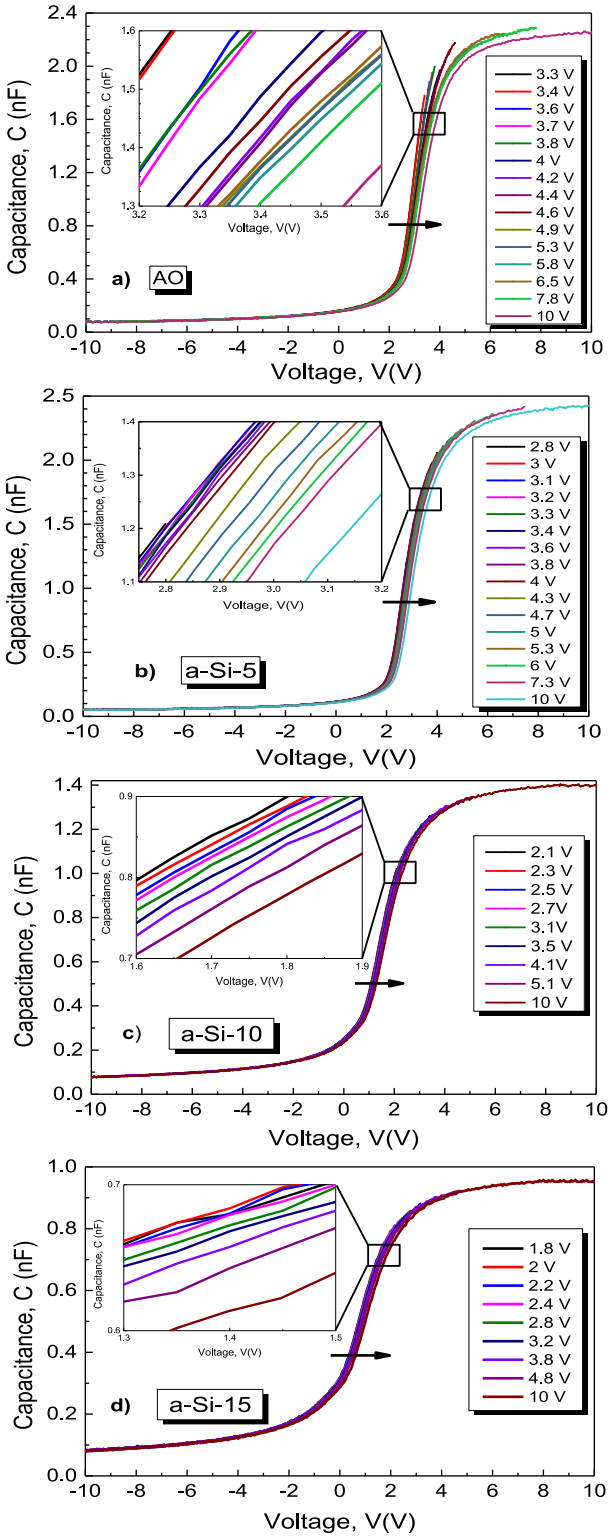

FIGURE 7. Sequential C-V characteristics with increased initial starting voltage corresponding to every 0.05 V increment in surface potential: (a) AO; (b) a-Si-5; (c) a-Si-10; (d) a-Si-15. The arrows indicate the direction of increasing starting voltage.

Regarding the **a − Si** samples, V_{FB} presents an almost linear variation with surface potential, and this behavior suggests that the electrons are systematically captured by the

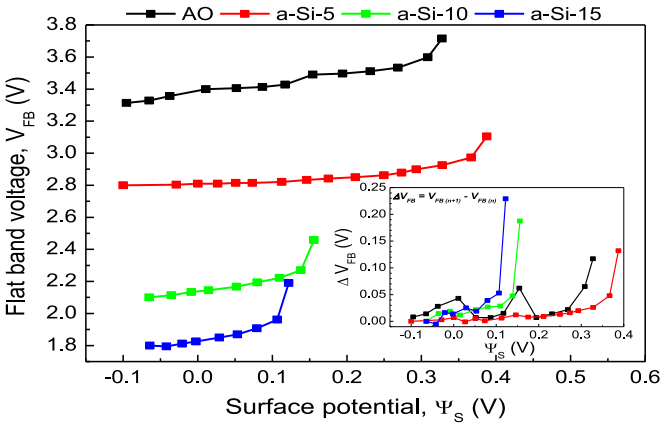

FIGURE 8. **Correlation between the flat band voltage and the surface potential for the fabricated SiC MOS capacitors; inset: the flat band voltage deviation from the previous value *vs.* surface potential.**

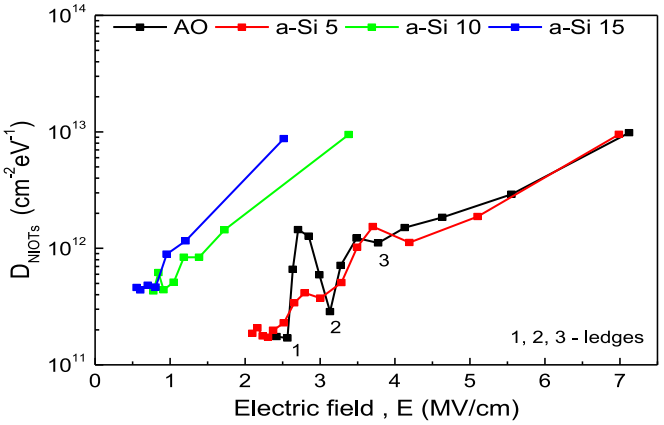

FIGURE 9. **Distribution of near interface oxide traps densities (D_{NIOTs}) as a function of the electric field across the gate oxide during charging.**

NIOTs [49], with a slight increase of the slope when the oxide layers have a higher thickness. On the contrary, a step like behavior is present in the case of the **AO** sample, which might determine an improperly electrical operation, affecting the stability of the fabricated SiC MOS devices. Moreover, the inset of Fig. 8 shows the dependence of the flat band voltage deviation from the previous value on the surface potential (ΔV_{FB} *vs.* Ψ_s). Firstly, it can be seen that all plots present two regimes of variation in function of the surface potential values. Thus, at low Ψ_s values, a linear variation of ΔV_{FB} is taking place, showing that the traps are slowly filled with electrons when the samples are biased near the flat band voltage. When the surface potential increases, up to accumulation regime, ΔV_{FB} rise rapidly, denoting that the electrons are quickly trapped. In the case of the **a − Si** samples with thicker oxides (**a-Si-10** and **a-Si-15** samples), the ranges corresponding to surface potential values are reduced, due to the more rapid approaching the saturation (Fig. 6).

The flat band voltage shifts determined from the experimental C-V measurements with increased start voltage were used further to estimate the D_{NIOTs} at different electric fields applied on the gate electrode [46]:

$$D_{NIOTs} = \frac{\triangle V_{FB} C_{ox}}{q \triangle \Psi_s} \tag{6}$$

where ΔV_{FB} is the flat band voltage variation between two consecutive start voltages, C_{ox} is the maximum capacitance from the accumulation regime – oxide capacitance, q is the electron charge and $\Delta\Psi_s$ represents the increment in surface potential.

The NIOT densities as a function of the applied electric field were estimated from the C-V dispersion analysis (Fig. 7) when the samples are biased from the flat band voltage to strong accumulation regime with an almost the same increment in surface potential. The resulted values are plotted in Fig. 9.

As it can be seen in Fig. 9, the NIOTs are filled under strong accumulation bias, and the density of the trapped electrons increases with increasing the accumulation bias (higher electric field). When the gate voltage is increased approaching the strong accumulation regime, a large number of electrons are captured by NIOTs and consequently a positive shift of the flat band voltage is taking place during the subsequent C-V measurement. This phenomenon observed in the distribution of the D_{NIOTs} can be also found in the flat band voltage variation with surface potential plots (see inset of Fig. 8), where ΔV_{FB} systematically increases with $\Delta\Psi_s$. Accordingly, the three ledges previously observed can be identified also in the case of the **AO** sample, preceded by steeper slopes, where the electrons are more easily captured by the near-interface oxide traps [47]. The a-Si samples show an approximately linear evolution of the D_{NIOTs} on the entire electric field range. Moreover, the samples with higher oxide thicknesses (**a-Si-10** and **−15**) present a slight increase of the D_{NIOTs} with a smaller range of the electric field across the gate oxide during the charging. When the samples are biased in strong accumulation, the values of the D_{NIOTs} correspond to the interface layer thicknesses estimated based on the XRR analyses, confirming the correspondence between their values and D_{NIOTs} ($IL_{\mathbf{a\text{-}Si\text{-}5}} = 0.94$ nm $< IL_{\mathbf{a\text{-}Si\text{-}15}} = 1.11$ nm $< IL_{\mathbf{a\text{-}Si\text{-}10}} = 1.84$ nm). Regarding the estimated densities values, our results are comparable with those reported when POA treatments were performed in different atmospheres like NO [47], N_2O [49] or $POCl_3$ [9].

The D_{NIOTs} substantially controls the doping profile, affecting the net charge density distribution in the depletion region. Therefore, in order to obtain information about the oping profile, differential capacitance measurements as function of gate bias have been performed for the fabricated structures. The free carrier charge density has a strong dependence in the depletion region on ionized dopant impurity concentration and the profile of the doping density (N_D) can be determined from the slope of the ($1/C^2$) vs. Ψ_s curves, using the following equations [50]:

$$N_D(W_D) = -2\left[q\varepsilon_0\varepsilon_r \frac{d}{d\Psi_s}\left(\frac{1}{C^2}\right)\right]^{-1} \tag{7}$$

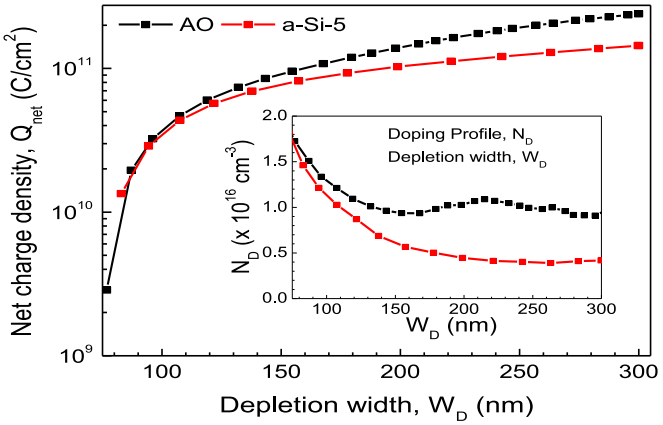

FIGURE 10. **Net charge density distribution in the depletion region for the fabricated SiC MOS capacitors; inset – the doping profile in the depletion region.**

$$W_D = \varepsilon_0 \varepsilon_r \left(\frac{1}{C} - \frac{1}{C_{ox}} \right) \tag{8}$$

where Ψ_s is the surface potential, W_D is the depletion region width, ϵ_o is the electrical permittivity of vacuum, ϵ_r is the electrical permittivity of SiC, q is the electronic charge.

The equations (7) and (8) are valid only if the charges from the depletion layer are originating from the ionized dopants and the depletion region width is larger than twice Debye length ($W_D > 2\lambda$), where λ is obtained using the formula [36], [50], [51]:

$$\lambda = \sqrt{\left(\frac{2kT\varepsilon_0\varepsilon_r}{q^2 N_D} \right)} \tag{9}$$

where k is the Boltzmann's constant, T is the temperature.

In our case, the Debye length is around 37.2 nm, indicating that the depletion approximation is valid for values of W_D higher than 75 nm, where the majority carrier concentration can be neglected in comparison to doping density. In Fig. 10 are showed both the resulted doping profile (see inset) and the net charge density distribution in the depletion region for the samples with similar thicknesses of the oxide layer (**AO** and **a-Si-5** samples). Since the doping density is inversely proportional to $dC/d\Psi_s$, its profile starts to decrease as a result of the D_{NIOTs} and D_{it} contribution, which affect the C-V characteristics even if the measurements have been performed at 1 MHz, noticeable through the appearance of some bumps in the depletion region [50]. Accordingly, these non-uniformities are more visible in the case of the **AO** sample, while, on the contrary, no such effect is evident in the case of the **a-Si-5** one, due to the significant lower values obtained for the interface traps, including the near interface oxide traps.

Furthermore, the lower values of both D_{it} and D_{NIOTs} lead to a diminished amount of additional charges in depletion region and might explain the differences between the net charge densities (Q_{net}) characteristics obtained by integrating the doping profiles. They become more important when the samples are biased from depletion to deep depletion region, due to the increased contribution of the additional charge originating from the minority carriers, which are attracted when a more negative voltage is applied.

V. CONCLUSION

In summary, we demonstrated that using a two-step process, consisting in depositing of an a-Si thin film by room temperature sputtering followed by oxidation, represents a valuable technological approach for fabrication of an oxide layer for SiC-MOS type devices, in terms of both technological steadiness and structure quality. Firstly, although apparently it is a more complicated technology, the budget necessary for SiC MOS processing is drastically reduced, especially when thicker SiO_2 layers should be obtained on SiC substrate. Thus, a simple preliminary deposition of an a-Si film shortens at least four-fold the length of the high temperature costly oxidation process. Secondly, even more important, this process flow assures not only cost-related benefits, but also, we demonstrated a significant improvement achieved for the electrical properties of the resulted oxide layers, principally due to the reduced amount of the effective oxide charges, the interface traps and the near interface oxide traps. The XRR structural investigations revealed that the thickness of the SiO_2/SiC interfacial layer, where these traps originate, becomes almost three-fold smaller in the case of the **a-Si-5** sample, thinner than 1 nm, in comparison with the **AO** one. Furthermore, even the thicker oxide layers fabricated present a reduced interfacial layer. The comparative analysis of the density variation performed for these samples confirmed the presence of the carbon-rich regions in the oxide side, but with a rapid decrease and consequently a reduced presence of C atoms into the oxide for **a-Si-5** that are the main source of the interface traps. The electrical measurements performed on the MOS capacitors with equivalent thickness of the oxide (**AO** *vs.* **a-Si-5**) further support these observations, showing a remarkable correspondence: the **a-Si-5** sample, with three-fold thinner interface layer led to a three-fold reduction of the total interface trap density, D_{tot}. Regarding the structures with thicker oxides, a two-fold diminish of the Q_{eff} is reached for **a-Si-15** structure. Moreover, the estimated D_{NIOTs} values lie in the range of $10^{11} - 10^{13}$ cm^{-2}eV^{-1} for all the investigated structures, and these results are confirmed by the doping profile and the net charge density distribution in depletion region, which finally control the stability of the SiC MOS devices.

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