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Automatic Fault Detection Circuit for Integrated Gate Drivers of Active-Matrix Displays

BYUNG-CHANG YU[1], JONGBIN KIM[1], SEUNG-HYUCK LEE[1], HOON-JU CHUNG[2], AND SEUNG-WOO LEE[1] (Senior Member, IEEE)

1 Advanced Display Research Center, Department of Information Display, Kyung Hee University, Seoul 02447, South Korea
2 School of Electronic Engineering, Kumoh National Institute of Technology, Gumi 39177, South Korea

CORRESPONDING AUTHOR: S.-W. LEE (e-mail: seungwoolee@khu.ac.kr)

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ABSTRACT This paper presents automatic fault detection circuit for integrated gate drivers. The proposed circuit consists of one capacitor and two TFTs per scan line. The circuit can detect three types of faults, such as line disconnection (LD), low voltage stuck (LVS), and high voltage stuck (HVS) for the gate driver due to external physical stress. Simulation results showed the proposed circuit operates well. In order to verify the circuit operation, it was fabricated with indium gallium zinc oxide thin film transistors process. The measurement results also verified that our proposed fault detection circuit could detect the types and locations of the LD and LVS of the gate driver successfully. However, we found that HVS can be detected, but further study is needed to accurately detect the position of HVS in the proposed circuit.

INDEX TERMS Fault detection, stretchable display, gate driver circuits.

I. INTRODUCTION

Fault detection has been studied to protect the safety and equipment of aircraft control systems, electronic medical systems, industrial controllers, and military systems, etc. In these applications, the faults can be fatal. For example, system faults on an aircraft can lead to a crash. Therefore, the fault detection has been widely used to prevent these faults from causing a fatal outcome to the system when faults occur in a critical part of the system. With the recent advances in display technology, a variety of applications have been researched and developed, such as transparent, rollable and stretchable displays [1]–[3]. In particular, the stretchable display has attracted attention as a future display since it is foldable, bendable, wrinkled and stretchable. However, it is very difficult to develop these new types of displays with high reliability because display components are vulnerable to external physical stress. As a part of these studies, researches such as flexible electrodes [4]–[6], substrate [7], [8], thin film transistor (TFT) [9]–[11], and materials [12] have been conducted. In 1992 and 1993, there were studies on fault-tolerant technology for display applications [13], [14], but the studies have not been cited so far. Recently, however, as the research on flexible displays has just started, the need for related research is emerging.

In the active matrix display, the gate driver is one of the key parts of assigning image data to each pixel. As demand for cost reduction, high resolution, and narrow bezel increases, the gate driver circuit with reliable TFTs has been integrated on a glass [15]. Due to integration on a glass, failures caused by the gate driver circuits have increased. In recent display products, many failures are directly related to the integrated gate drivers. If a display screen looks abnormal, it is necessary to analyze the gate driver to find a root cause and the failure location. However, it takes a long time to find root causes of the faults, since most of recent displays have high resolution and the number of stages of the gate driver is very large. In particular, it is difficult to figure out the exact types and locations of faults. For example, in the case of repeated output or no output, abnormal images may be observed over the whole screen. A fault in one stage causes the whole gate driver to fail since the current stage affects the next one. Therefore, if the position and type of the fault of the gate driver is clearly detected, it is very useful to analyze many failures for the gate driver quickly,

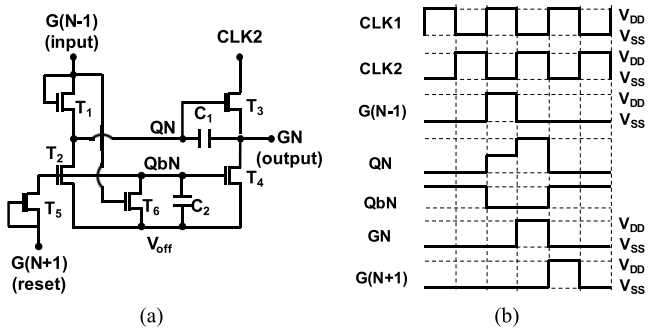

FIGURE 1. (a) Schematic of the gate driver circuit [16]. (b) Corresponding control signals and outputs.

which provides significant time savings and helps develop reliable display products.

In this paper, we propose an automatic fault detection circuit that can determine the position and type when the fault occurs at a specific stage of gate driver due to physical stress during display driving. The fault detection circuit consists of two TFTs and one capacitor per scan line. When a scan signal occurs at each stage, the proposed circuit detects three faults (line disconnection, low voltage stuck, and high voltage stuck). The proposed circuit operation is explained and verified with simulation and measurement results in the next section.

II. FAULTS OF GATE DRIVER

The physical stress applied to the gate driver can cause drift of TFT characteristics, surface crack of substrate, signal line disconnection etc. Since the capacitor and pull-up/-down TFTs of the gate driver have a large area, the probability of cracking caused by external stress is much larger than those of other circuit portions. Therefore, if disconnection or cracking of the TFTs occurs in the gate driver, output signals may not be generated. Or some outputs may be stuck to a low voltage or a high voltage. Here, we assume three failure cases, line disconnection (LD), low voltage stuck (LVS), and high voltage stuck (HVS). Fig. 1(a) and Fig. 1(b) show the gate driver used for this study and its timing diagram, respectively [16]. It comprises six TFTs and two capacitors. Each stage of the gate driver has four control signals. As shown Fig. 1(b), CLK1 and CLK2 are two-phase non-overlapping clocks.

Line disconnection (LD): A signal line is disconnected between the gate driver and the display panel. When the output signal of the stage N, GN is disconnected, GN is supplied to the stage (N+1), but GN is not supplied to the display panel because the line is disconnected.

Low voltage stuck (LVS): A particular output stage is stuck to a low voltage. When G(N+1) is stuck to low voltage, high pulses are repeatedly generated at the output GN. If the reset signal G(N+1) is low, QN cannot be discharged. And QbN keeps low level. QN is periodically bootstrapped by CLK2 and repetitive output is generated. After that, G(N+1) and G(N+2) remain low.

High voltage stuck (HVS): A certain output is stuck to high voltage. When G(N+1) is stuck at high, QbN is continuously charged by G(N+1). The pull-down transistor (T4) of the stage N is turned on and GN is maintained low. The G(N−1) generates the same repetitive output as when GN is stuck low. On the other hand, since Q(N+2) node is charged by high voltage of G(N+1) and then it bootstrapped periodically, G(N+2) generates repetitive output.

Even though output of the gate driver is not generated under normal conditions, repetitive scan signals for LVS and HVS cases are also generated in vertical blank period. The simulation results of the gate driver output for each fault are shown in Section III-B.

III. FAULT DETECTION CIRCUIT

It is necessary to detect whether scan signals of the gate driver are properly generated during operation. Fig. 2 shows our proposed circuit for the fault detection and how it works. A unit cell enclosed by a dashed line comprises two oxide TFTs (T_{WR} and T_{DR}) and one capacitor (C_{ST}). The driving TFT (T_{DR}) is used to charge or discharge V_{READ} node; the writing TFT (T_{WR}) to write data; and the storage capacitor (C_{ST}), to accumulate electric charges. V_{INIT} is a DC voltage for initializing the node V_{READ}. $V_{CONTROL}$ represents a write control signal. V_{WRD} maintains the T_{DR} in off state until the V_{PROG} is bootstrapped by the GN signal.

A. OPERATION

Figs. 2(a) and 2(b) show the proposed circuit for the fault detection of several gate signals and their timing diagram, respectively. The V_{DATA} represents charging or discharging voltage for the read line when T_{DR} is turned on by the scan signal. High or low voltage is alternately applied. Let's assume that V_{DATA} with high voltage is applied to odd lines during odd frames and low V_{DATA} to even lines during even frames. It is necessary to obtain the V_{READ} waveform during both odd and even frames to find out the location and types of faults. The operation of the fault detection circuit is divided into two steps: initializing and programming; charging and discharging.

Initializing and Programming: During period (0) as shown in Fig. 2(b), the $V_{CONTROL}$ rises to high, every T_{WR} turns on, and every V_{PROG} ischarged to V_{WRD}. At the same time, the read line (V_{READ}) is initialized to V_{INIT}.

Charging and Discharging: If the N-th scan signal GN goes high, T_{DR_N} is turned on by bootstrapping C_{ST_N}. Then, the read line is charged or discharged depending on V_{DATA}. As shown in Fig. 2(b), V_{DATA} is an alternating signal. During even frames, V_{DATA} becomes high for even time steps such as (2), (4), and so on. During odd frames, V_{DATA} becomes high for odd time steps such as (1), (3), and so on.

Thus, when the gate driver normally operates, the waveform of the node V_{READ} is exactly the same as the V_{DATA}. It is possible to detect whether the scan signal is properly applied to the display panel by checking the difference between V_{DATA} and V_{READ}.

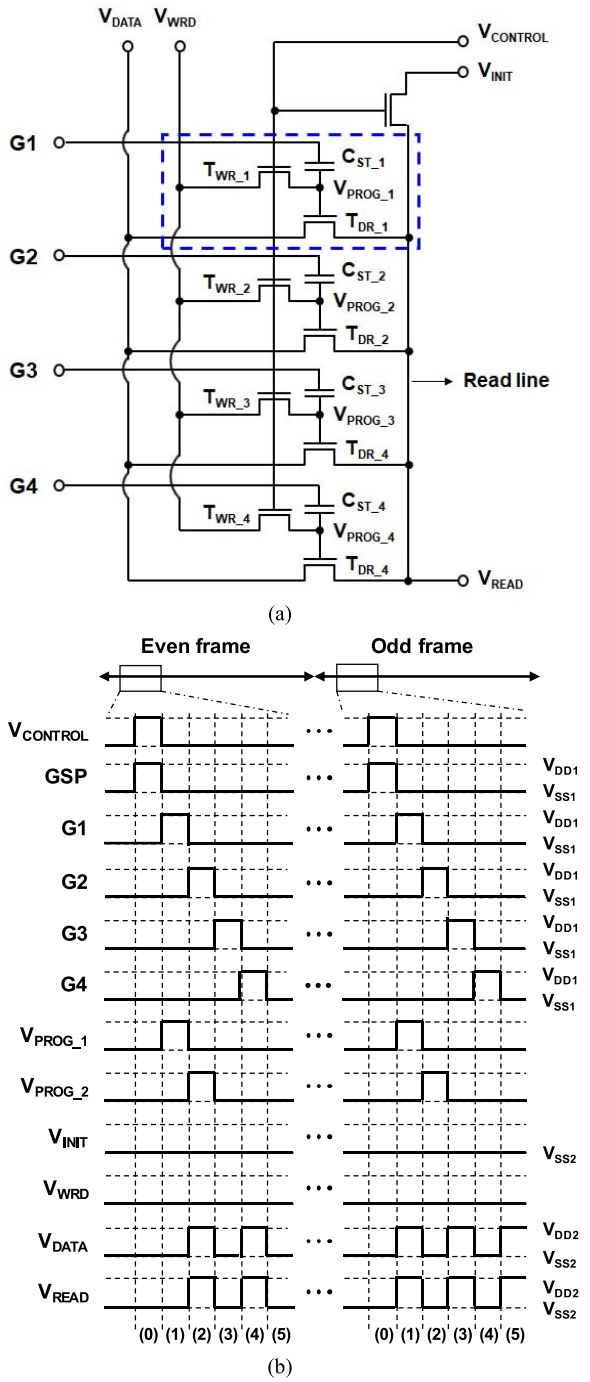

FIGURE 2. **(a) The proposed fault detection circuit and (b) its timing diagram.**

B. FAULT DETECTION METHOD

Here, we carried out circuit simulation using a commercial circuit simulator, Smart-SPICE. The oxide TFT simulation model is based on the widely accepted Rensselaer Polytechnic Institute (RPI) amorphous silicon (a-Si) TFT model (Level = 35) in Smart-SPICE [17]. The design parameters of the gate driver and the fault detection circuit are listed in Table 1. One frame time is divided into two parts; scanning period and vertical blank. During scanning period,

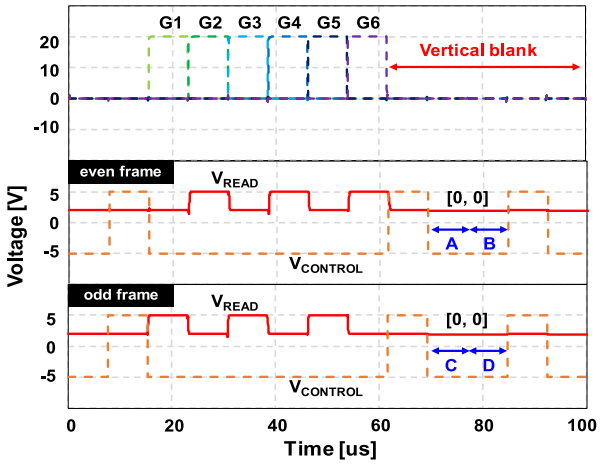

FIGURE 3. **Simulated results when gate driver operating properly.**

gate driver generates scanning pulse whereas there's no scanning pulses during vertical blank. Our proposed architecture detects where fault occurs during scanning period and distinguishes the type of the fault during vertical blank.

Fig. 3 shows simulated results when gate driver operates properly. The width of scan signal was set to 7.7 μs. In the scanning period, the V_{PROG} nodes of the fault detection circuit are sequentially bootstrapped by scan pulses and V_{READ} is charged or discharged depending on V_{DATA}. Since the V_{DATA} waveforms of two consecutive frames are completely reversed, the waveforms of V_{READ} of even and odd frames are reversed. Normally, there is no scanning pulse during the vertical blank. So, as shown in Fig. 3, V_{READ} is maintained to V_{INIT} after V_{READ} initialized in the both frames. We can get more information on the faults if we carefully investigate V_{READ} during vertical blank. The two values of V_{READ} right after resetting V_{READ} in even frame are assigned to A and B as shown in Fig. 3. The counterparts in odd frame are assigned to C and D. We can find that [A, B] and [C, D] are all [0, 0] if there is no error in the circuit.

Fig. 4 shows simulated results when the output line of the second stage is disconnected. In the scanning period of even frame, when the G1 signal is applied, V_{DATA} supplied to V_{READ}. At this time, V_{DATA} is the same as V_{INIT}, so it is kept low to 2 V. After that, since the scan signal of the second stage is not applied, the V_{PROG_2} node cannot be bootstrapped by G2. That is, V_{READ} during both frames follows V_{DATA} of the previous stage as shown in Fig. 4. After that, V_{READ} goes to alternately high and low states because other scan signals are normal. When the LD occurs, it is possible to accurately detect the position by checking where the V_{READ} maintains the previous value during scanning period. The yellow arrows in Fig. 4 indicate where LD occurs. Even though LD occurs, [A, B] and [C, D] are all [0, 0] as shown in Fig. 4.

Fig. 5 shows simulated results when LVS occurs. Let's assume the second output is stuck low. Then the third and next output signals stay low because no initial signal

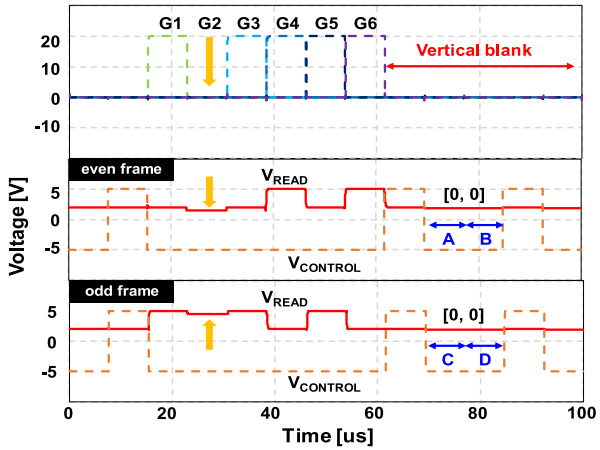

FIGURE 4. Simulated results when the second output line is disconnected.

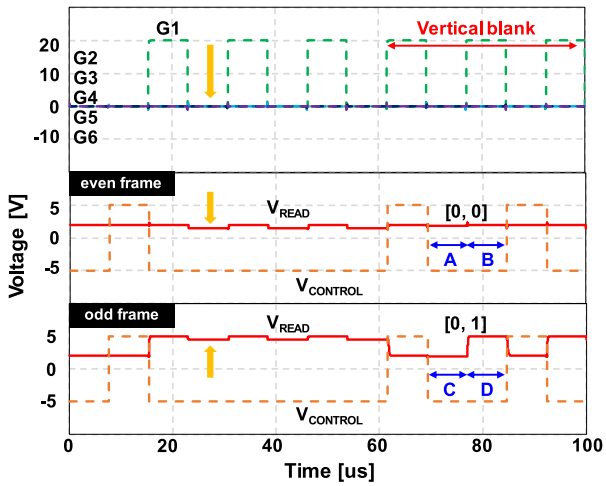

FIGURE 5. Simulated results when the second output stuck at low voltage.

comes into the third stage. But, G1 oscillates as shown in Fig. 5 because of no reset signal from the second stage. It is easy to accurately detect the LVS position by checking where the V_{READ} starts to maintain the previous value during scanning period. The V_{READ} keeps the value until V_{READ} is reset by $V_{CONTROL}$ at the beginning of the vertical blank as shown in Fig. 5. [A, B] and [C, D] are [0, 0] and [0, 1], respectively when LVS occurs at the second output stage.

Fig. 6 shows simulated results when the third stage is stuck at high voltage (HVS). When the fault occurs in the third output stage (G3), the first and fourth stages (G1 and G4) generate repeating pulses because the second output is forced to low by G3. It means that G1 and G4 look like two non-overlapping clock signals. No matter where HVS occurs, the two non-overlapping clock signals make V_{READ} exactly the same as V_{DATA}. For this reason, the V_{READ} shows the same waveform as that in the case of no fault. Therefore, it is difficult to detect if HVS occurs during scanning period. However, we can detect HVS since HVS forces V_{READ} alternating during vertical blank once HVS occurs whereas

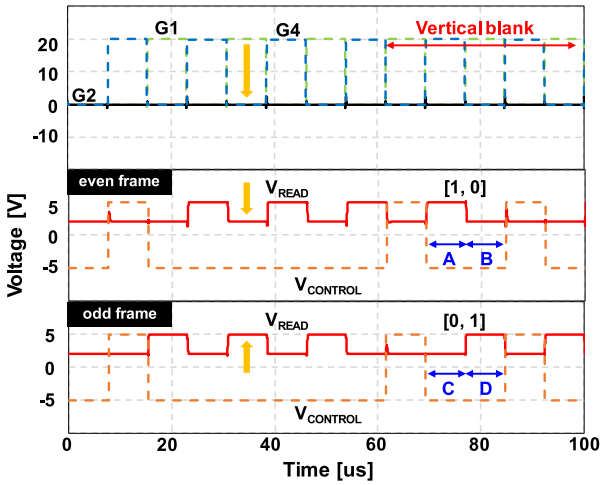

FIGURE 6. Simulated results when the third output stuck at high voltage.

V_{READ} maintains low when there is no fault as shown in Fig. 3. As shown in Fig. 6, after the V_{READ} is initialized to V_{INIT} during the vertical blank in the even and odd frames, V_{DATA} is applied to V_{READ}. Thus, [A, B] and [C, D] are [1, 0] and [0, 1], respectively. Therefore, if HVS occurs, we can detect it during only vertical blank.

Table 2 shows the detectable faults during scanning period and vertical blank. HVS is only detected during vertical blank. However, owing to LD and LVS are detectable independent of display driving, immediate and automatic feedback is possible to the display.

IV. RESULTS AND DISCUSSION

To verify the fault detection circuit, we fabricated the proposed fault detection circuit. First, a 150-nm-thick molybdenum (Mo) layer is deposited as a gate metal. Then, a 62-nm-thick silicon oxide (SiO_2) layer is deposited on the gate metal layer as a gate insulator. Then, 40-nm-thick indium gallium zinc oxide (IGZO) is deposited. Finally, 150-nm-thick Mo layer is deposited as a source/drain (S/D) metal. Table 1 shows the fabricated condition of fault detection circuit. The optical microscopy image of the fabricated fault detection circuit is shown in Fig. 7. Fig. 8 shows the transfer characteristic of the fabricated oxide TFT. The device shows Vth of −0.1 V. The Vth is defined as the gate voltage (V_G) corresponding to drain current (I_{DS}) of W/L×10 pA at $V_D = 0.1$ V. The subthreshold swing and field-effect mobility (μ_{FE}) of the TFT is 0.15 V/dec, and 69 cm^2/Vs, respectively. The number of stages of the fault detection circuit was four and the pulse width of scan signal was set to 100 μs. We could not operate the proposed circuit properly with the scan signal of 7.7 μs that was used for the simulation, since the load of the measuring equipment (oscilloscope including the measurement probe) was large. For this reason, we were able to verify only the circuit operation with the signal of 100 μs. We tried to measure the operation of the proposed circuit with a pico-probe that has

TABLE 1. Design parameters for the gate driver and fault detection circuit.

Gate Driver		Fault Detection Circuit	
T_1, T_5 (W/L)	25 μm/5 μm	T_{WR}, T_{DR} (W/L)	20 μm/20 μm
T_2, T_6 (W/L)	10 μm/5 μm	T_{INIT} (W/L)	80 μm/20 μm
T_3, T_4 (W/L)	250 μm/5 μm	C_{ST}	0.5 pF
C_1, C_2	0.5 pF	V_{DATA}	5 V to 2 V
V_{DD}	20 V	$V_{CONTROL}$	5 V to -5 V
V_{SS}, V_{OFF}	0 V	V_{INIT}	2 V
CLK Frequency	65 KHz	V_{WRD}	-2 V

TABLE 2. Detectable faults during scanning period and vertical blank.

Detectable faults			
Scanning period (additional data of fault position)		Vertical blank (additional data of fault type)	
LD	O	LD	X
LVS	O	LVS	O
HVS	X	HVS	O

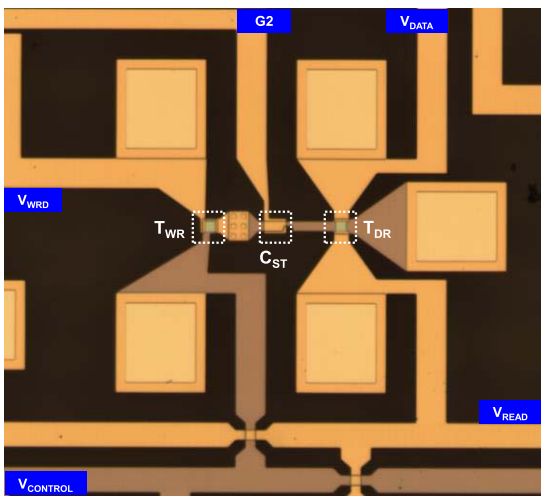

FIGURE 7. Optical microscopy image of the fabricated fault detection circuit.

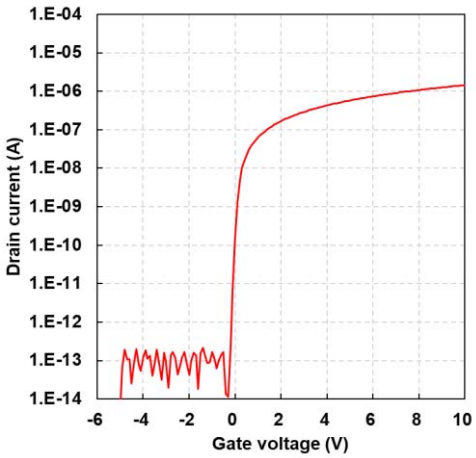

FIGURE 8. Transfer characteristic of the fabricated oxide TFT (V_{DS} = 0.1 V).

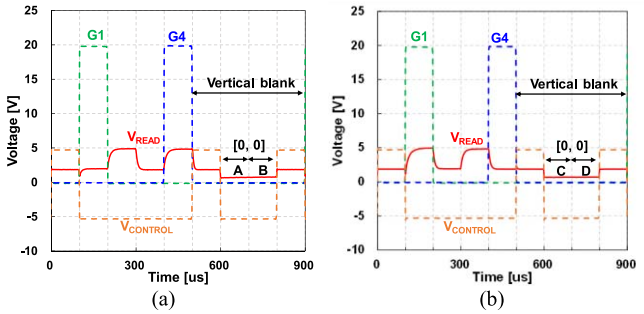

FIGURE 9. Results measured at (a) the even and (b) the odd frames when gate driver operating properly.

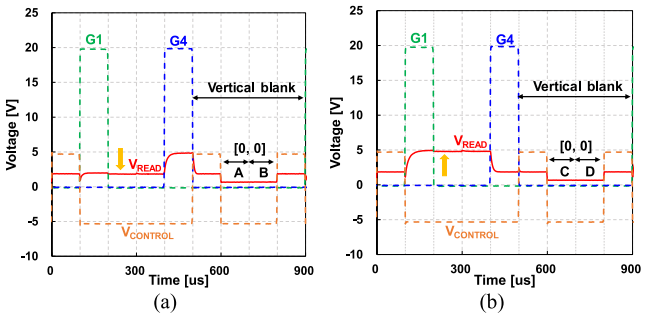

FIGURE 10. Results measured at (a) the even and (b) the odd frames when the second output line is disconnected.

ultra-low electric load. But, we could not get it. So, we had to measure it with a conventional oscilloscope whose electric load is so high.

Fig. 9 shows measurement results when there is no fault. Figs. 10, 11, and 12 show the results measured at the even and odd frames for LD, LVS, and HVS occurred, respectively. Signals were measured under the assumption that the second output line had LD as shown in Fig. 10. As shown in Figs. 10(a) and 10(b), V_{READ} kept its previous values as indicated by yellow arrows during scanning period. During vertical blank, the measured [A, B, C, D] was [0, 0, 0, 0] as shown in Figs. 10(a) and 10(b). Thus, we confirmed what we discussed earlier that [A, B, C, D] is the same as that obtained when the gate driver operates properly during vertical blank. More importantly, we can easily identify the fault as LD and find the fault location by comparing V_{READ} with V_{DATA} during scanning period.

LVS can be detected during both scanning period and vertical blank, but HVS can be detected only during vertical blank. As shown in Fig. 11 where LVS occurs, the measured [A, B, C, D] was [0, 0, 0, 1]. In the case of HVS as shown in Fig. 12, [A, B, C, D] was [1, 0, 0, 1]. V_{READ} is the same when we investigate it only one frame time as shown in Figs. 11(b) and 12(b). However, V_{READ} is different in even

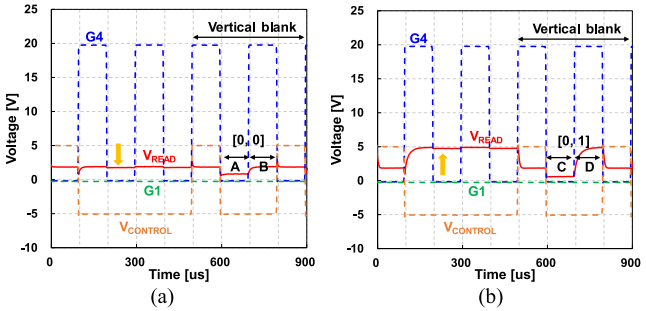

FIGURE 11. **Results measured at (a) the even and (b) the odd frame when the second stage stuck at low voltage.**

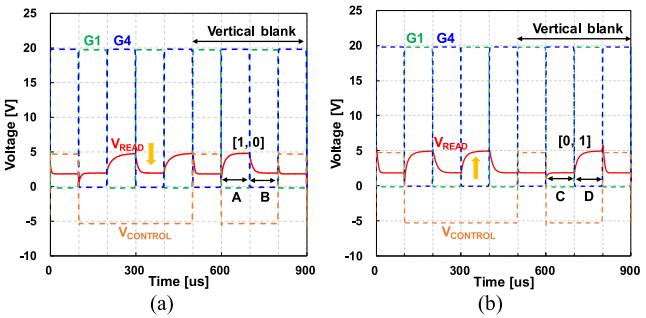

FIGURE 12. **Results measured at (a) the even and (b) the odd frame when the third stage stuck at high voltage.**

frames as shown in Figs. 11(a) and 12(a). In this way, LVS and HVS should be distinguished in the vertical blank for two frame times. As a result, the data for all LVS cases are [0, 0, 0, 1], [0, 1, 0, 0], [0, 0, 1, 1], and [1, 1, 0, 0]. In these four cases, it can be judged that the LVS has occurred. In the case of HVS, it is certain that the voltage change occurs in both frames as shown in Fig. 12, since two non-overlap scan signals are repeated. Thus, all the data when HVS occurs are [0, 1, 0, 1], [0, 1, 1, 0], [1, 0, 0, 1] and [1, 0, 1, 0]. In these four cases, it can be judged that the HVS has occurred. It is easy to accurately detect the position of the fault by checking where the V_{READ} maintains the previous value during scanning period, as shown in Figs. 10 and 11, where the LD and LVS occurs. However, the position of the HVS cannot be detected since V_{READ} alternates regardless of the position of the fault as shown in Fig. 12. Thus, we think more studies are needed in order to detect an accurate position of the HVS.

V. CONCLUSION

In this paper, we have proposed a new fault detection circuit with a simple structure composed of two oxide transistors and one capacitor per scan line. The fault detection circuit can determine the types and position of faults such as LD, LVS, and HVS quickly during operation. It is difficult to detect the position of the HVS accurately, which will be resolved by further study in the near future. The fault detection circuit can be used to analyze the gate driver of scalable display that is vulnerable to physical stress. We believe that our proposed technology will contribute to higher yield and reliability of the display products.

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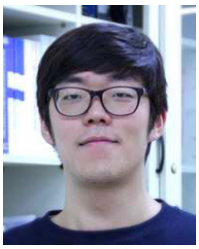
BYUNG-CHANG YU received the B.S. and M.S. degrees in information display from Kyung Hee University, Seoul, South Korea, in 2016 and 2018, respectively. He is currently a Research Engineer with Samsung Display.

JONGBIN KIM received the B.S. and M.S. degrees in information display from Kyung Hee University, Seoul, South Korea, in 2010 and 2012, respectively, where he is currently pursuing the Ph.D. degree with the Department of Information Display. His research interests include driving methods and circuits for various types of displays, including LCD and OLED displays.



SEUNG-HYUCK LEE received the B.S. and M.S. degrees in information display and the Ph.D. degree from Kyung Hee University, Seoul, South Korea, in 2011, 2013, and 2018, respectively. He is currently a Senior Research Engineer with LG Display.

HOON-JU CHUNG received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea, in 1994 and the M.S. and Ph.D. degrees from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 1997 and 2002, respectively. He is currently a Full Professor with the School of Electronic Engineering, Kumoh National Institute of Technology.

SEUNG-WOO LEE (SM'10) received the B.S. and M.S. degrees in electrical engineering and the Ph.D. degree from the Korea Advanced Institute of Science and Technology in 1993, 1995, and 2000, respectively, where he conducted research on integrated driver circuits for poly-Si TFT-LCDs.

He joined Samsung in 2000, where his work has focused on the development of key driving technologies for active-matrix liquid-crystal displays. He has played a key role in image quality enhancement, high-end LCD timing-controller design, FPGA evaluation of new driving schemes, next-generation LCD interface technologies, and advanced LCD driving schemes for large-size TV applications. He was also in charge of the development of analog–digital mixed-signal ICs for TFT-LCDs. He joined Kyung Hee University, Seoul, South Korea, where he has been studying novel display systems and visual perception and is currently a Full Professor with the Department of Information Display.

Prof. Lee was a recipient od the 2008 Chester Sall Award from IEEE Consumer Electronics Society in 2010. He has been active as a Senior Member of Society for Information Display since 2010.