Received 13 October 2018; revised 4 November 2018; accepted 5 November 2018. Date of publication 12 November 2018; date of current version 1 March 2019. The review of this paper was arranged by Editor C.-M. Zetterling.

Digital Object Identifier 10.1109/JEDS.2018.2880005

High Performance Single Crystalline Diamond Normally-Off Field Effect Transistors

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This work was supported by the National Key Research and Development Program of China under Grant 2018YFB0406504.

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ABSTRACT High performance normally-off hydrogen-terminated diamond (H-diamond) MOSFETs were fabricated on single crystalline diamond grown in our lab. The device with 2-μm gate length shows threshold voltage of -1.0 V, and a drain current of 51.6 mA/mm at $V_{GS} = V_{DS} = -4.5$ V and an on-resistance of 65.39 Ω·mm. The transconductance keeps increasing when V_{GS} shifts from V_{TH} toward more negative direction, and reaches the record high value of 20 mS/mm at V_{GS} of -4.5 V, which benefitted from the almost constant mobility of the holes in the gate voltage range of -4 V $< V_{GS} < -2$ V. The critical device process to realize these low on-resistance normally-off MOSFETs consists of 2-min UV ozone treatment of the H-diamond surface and thermal oxidation of aluminum film in the air to form an alumina gate dielectric.

INDEX TERMS Single crystalline diamond, normally-off, MOSFET.

I. INTRODUCTION

Compared with Si, GaN and SiC, diamond has wider bandgap, higher breakdown voltage, higher carrier mobility, higher thermal conductivity, higher hardness, and so on. It has tremendous potential to be used as a kind of semiconductor except its low bulk doping efficiency [1], [2]. The p-type surface conductivity of the hydrogen terminated diamond (H-diamond) has greatly motivated the application of diamond in electronics devices. The state-of-the-art H-diamond field effect transistors (FETs) have achieved the cutoff frequency of 53 GHz [3], and the maximum oscillation frequency of 120 GHz [4], and the breakdown voltage over 2 kV [5]. The thermal stability at 400 °C [6] has also been achieved on the devices passivated by Al_2O_3.

The thermal stability [7] and the radiation-resistant property [8] of diamond FETs have shown great potential to develop the logic circuits used in extreme environments. To promote the application of the diamond devices in logic circuits, it is necessary to develop the enhancement mode (normally-off) FETs [9]. However, most reported H-diamond FETs are the depletion mode (normally-on) devices.

Recently, the normally-off H-diamond metal oxide semiconductor field effect transistors (MOSFET) have been achieved by several different methods. Koide *et al.* obtained the normally-off H-diamond MOSFETs by using bilayer gate oxide deposited by atomic layer deposition (ALD) and sputtering deposition (SD) techniques and annealing (baking) the devices at 150-350 °C. Typical gate dielectric consist of SD-$LaAlO_3$/ALD-Al_2O_3 [10], [11], or SD-HfO_2/ALD-HfO_2 [12], or SD-TiO_2/ALD-Al_2O_3 [13]. A single oxide layer grown on H-diamond such as Y_2O_3 [14] was also reported leading to normally-off MOS channel. Kawarada *et al.* [5] demonstrated the 2-kV normally-off C-H diamond MOSFETs with partial C-O channel and ALD-Al_2O_3 gate dielectric. In addition, long time annealing H-diamond in the air at 180 °C in the preparation of the Al_2O_3 gate dielectric by thermal oxidation of aluminum also achieved the normally-off devices [15]. However, most reported normally-off H-diamond devices showed much higher on-resistance and lower output current compared to the normally-on devices with the same gate lengths. Therefore, it is necessary to

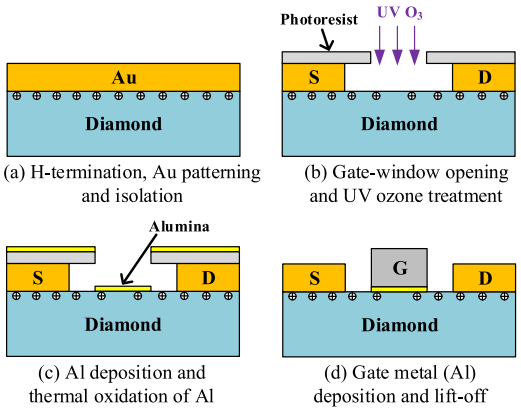

FIGURE 1. Process flow of our H-diamond MOSFET.

improve the performance of the H-diamond normally-off devices.

In this letter, we report the achievement of the H-diamond normally-off MOSFETs with high performance. The devices were fabricated on the single crystalline diamond grown by microwave power chemical vapor deposition (MPCVD) in our lab. The direct current (DC) and capacitance-voltage (CV) properties of the normally-off H-diamond devices were demonstrated.

II. EXPERIMENT

The colorless $4.5\times4.5\times1$ mm^3 single crystal diamond (SCD) used for device fabrication was grown in our 6 kW 2.45 GHz MPCVD system on a commercially available high-temperature high-pressure (HTHP) type-Ib (001) diamond substrate. The purity of the hydrogen and the methane we used is 6N and 5N5, respectively. During growth the pressure, temperature and microwave power are 290 mbar, 920 °C and 3.8 kW, respectively. The total gas flow rate of 200 sccm and the methane concentrations of 5% were used. After growth the epilayer was separated from the substrate and polished to the roughness below 1 nm. The devices were fabricated on the CVD epilayer.

The H-diamond surface was obtained by treating the SCD in the MPCVD chamber with hydrogen plasma for 20 min. During treatment, the hydrogen flow, microwave power and temperature are 600 sccm, 2 kW and 890 °C, respectively. The device process flow is shown in Fig. 1 and similar in details to that in Reference [16], except two points aiming to realize a low on-resistance normally-off MOSFET channel. The first is that after defining the gate window and wet-etching of gold using KI/I_2, the exposed H-diamond surface is treated by ultraviolet (UV) ozone for 2 min (Fig. 1(b)) to turn H-diamond surface into partially oxygen-terminated. The UV ozone treatment was performed by using PSD series digital UV ozone system (Novascan). The ozone was produced by the molecular excitation of oxygen in the air by UV light at both 185 nm and 254 nm. No other gas was introduced into the chamber. The second is that we use alumina as gate dielectric by oxidizing a thin aluminum layer (nominally 4 nm) by putting the sample on a hotplate and annealing it in air at 80 °C for half an hour. The aluminum is deposited by using electron beam evaporation system. The thickness of the alumina layer is 5.0 nm determined by using ellipsometer. Fig. 2 shows the surface morphology image of the alumina layer measured by atomic force microscopy (AFM), and the root-mean-square roughness is measured to be 0.513 nm. Finally, the H-diamond MOSFETs with a gate width (W_G) of 50 μm and different gate lengths (L_G) of 2 μm, 4 μm, 6 μm, 40 μm were achieved. The schematic cross section of our devices is shown in Fig. 1(d). The characterizations of the devices were carried out using Keithley 4200 semiconductor parameter analyzer at room temperature.

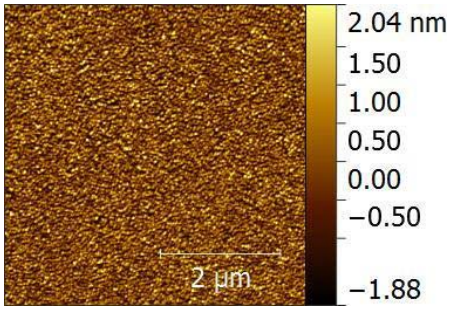

FIGURE 2. Surface morphology image of the alumina layer measured by AFM.

III. RESULT AND DISCUSSION

The output and transfer characteristics of the 2-μm MOSFET are given in Fig. 3 and Fig. 4. The device shows a maximum saturation drain current (I_D) of −51.6 mA/mm at the gate voltage (V_{GS}) equaling to the drain voltage (V_{DS}) of −4.5 V, and an on-resistance (R_{ON}) of 65.39 Ω·mm (1307.8 Ω), respectively. The transfer characteristics of the device at $V_{DS} = -0.1$ V are shown in Fig. 4(c). We find the point of maximum slope on the $I_{DS} \sim V_{GS}$ curve by a maximum in the transconductance, and fit a straight line to the curve at that point and extrapolate to $I_{DS} = 0$ to extract the threshold voltage (V_{TH}) [21]. The V_{TH} is extracted to be −1.0 V (Fig. 4(c)), so the device is in the normally-off operation mode. The transconductance (g_m) keeps increasing when V_{GS} shifts from V_{TH} towards more negative direction, and reaches the maximum value of 20 mS/mm at V_{GS} of −4.5 V. The on/off ratio is up to 10^8 (Fig. 4(b)), and it is mainly limited by the gate leakage current (I_G). The high on/off ratio indicates the good insulativity of our CVD grown SCD and the effectiveness of the device isolation. In the V_{GS} range between 0 V and the V_{TH}, the subthreshold swing (SS) is about 100-150 mV/dec, and the minimum SS reaches 77 mV/dec at $V_{GS} = 0.1$ V (Fig. 4(d)). Compared with the very recently reported normally-off 2-μm $LaAlO_3/Al_2O_3$/H-diamond MOSFET delivering a record large current [9], our device with a larger g_m shows a larger current and a lower R_{on} at the same $|V_{GS} - V_{TH}|$ value. Therefore our target high performance normally-off MOSFET channel is achieved.

The device performance is closely related to our device process inspired by two reported phenomena. One is that

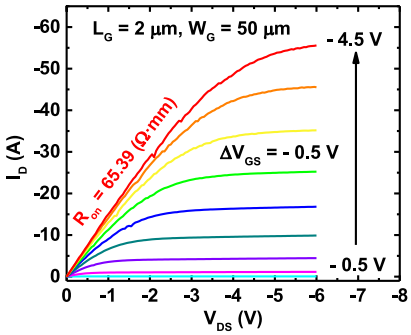

FIGURE 3. Output characteristics of the 2-μm H-diamond MOSFET.

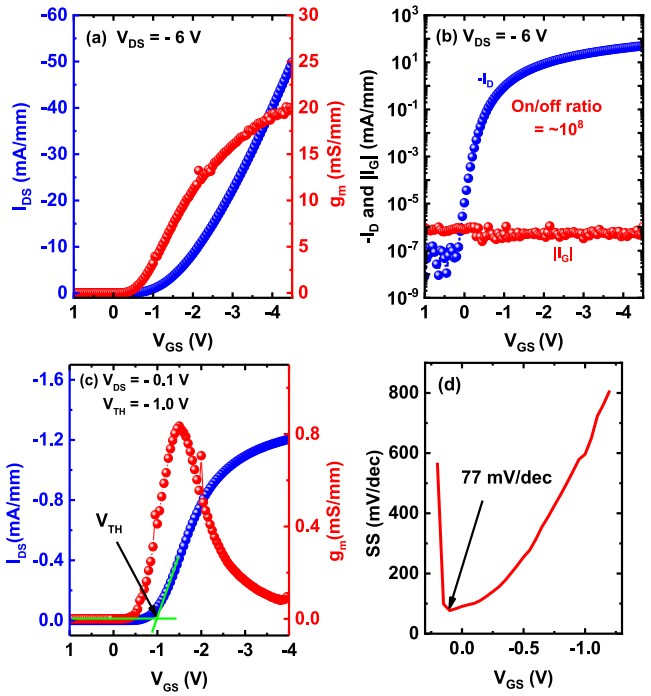

FIGURE 4. Transfer characteristics of the 2-μm device. (a) $-I_D$ and g_m in linear coordinate (b) $-I_D$ and $|I_G|$ in logarithmic coordinate (c) transfer characteristics at $V_{DS} = -0.1$ V, (d) subthreshold swing of the device.

UV ozone treatment can turn H-diamond surface to partially oxygen-terminated, and so the two-dimensional hole gas (2DHG) density can be reduced to some extent depending on the treating time [17]. The H-diamond MOSFETs with partial C–O channel and ALD-Al_2O_3 gate dielectric achieved a V_{TH} ranging in -2.5 V to -4 V [5]. The other is that annealing H-diamond covered by 4-nm aluminum layer in the air at 180 °C for 10 h also leads to normally-off MOSFETs with the alumina gate dielectric [15]. Our normally-off device process combines those from References [5] and [15] but is much simpler, and some process condition changes are critical to reduce the channel resistance. Compared with Reference [5], we shortened the time of UV ozone treatment, and the photoresist above the source-gate and drain-gate interspaces also alleviate the influence of UV ozone. As for the thermal oxidation of aluminum similar to Reference [15], both the temperature and the time are much reduced and it also helps to protect the p-type conductivity of the H-diamond exposed in the air.

In order to further comprehend the property of the alumina gate dielectric, the I-V and C-V characteristics of the gate-source diode of the devices with $L_G = 40$ μm were investigated. Fig. 5 (a) shows that the gate leakage current $|I_{GS}|$ is smaller than 10^{-6} A/cm^2 for $V_{GS} \geq -2.5$ V, and increases with the increasing of $|V_{GS}|$, and reaches the maximum value of 4.46×10^{-6} A/cm^2 at $V_{GS} = -4.5$ V. This leakage is at the same level to that of the Al_2O_3 prepared by oxidation of 3-nm aluminum reported by Hirama *et al.* [18].

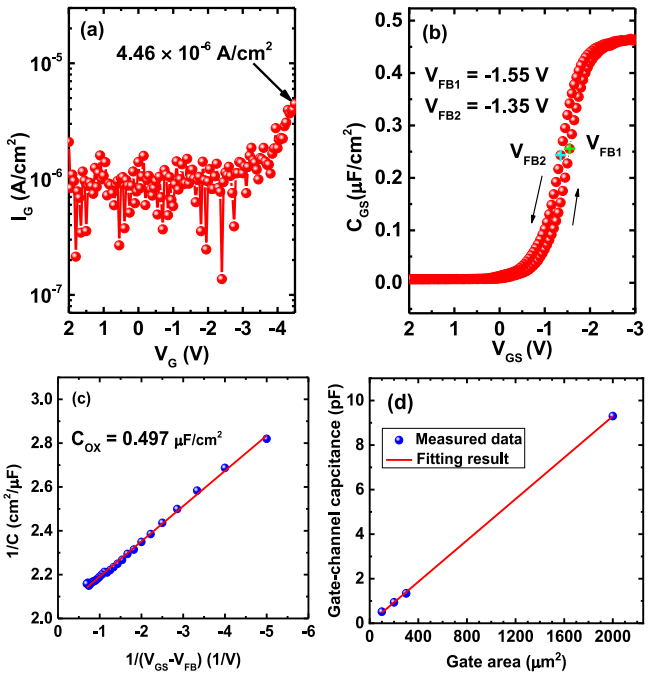

FIGURE 5. Measured (a) I-V, (b) C-V characteristics and (c) 1/C vs. $1/(V_{GS} - V_{FB})$ relation of the gate-source diode of our normally-off H-diamond MOSFETs with $L_G = 40$ μm. (d) Gate-to-channel capacitance dependent on gate area.

The C-V curve was measured at the frequency of 1 MHz (Fig. 5 (b)). The obvious accumulation and depletion mode regions are observed. For the Al/alumina/H-diamond structure, the theoretical flat-band voltage (V_{FB0}) is calculated to be 0.62 V based on the work functions of aluminum and H-diamond as 4.28 and 4.9 eV [19], respectively. The experimental flat-band voltage of the device can be extracted by using the method reported in Reference [20], and those for the forward-direction sweeping (V_{FB1}) and the reverse-direction sweeping (V_{FB2}) were -1.55 and -1.35 V, respectively. The negative shift of the experimental flat-band voltages relative to the theoretical one indicates the presence of positive fixed charge in the alumina layer, which contributes to reduce the hole density of our MOS channel. As the aluminum is oxidized at a quite low temperature of 80 °C, oxygen vacancies may exist in the alumina and result in the positive charge. The V_{FB} difference between forward and the reverse direction is 0.20 V, which could be induced

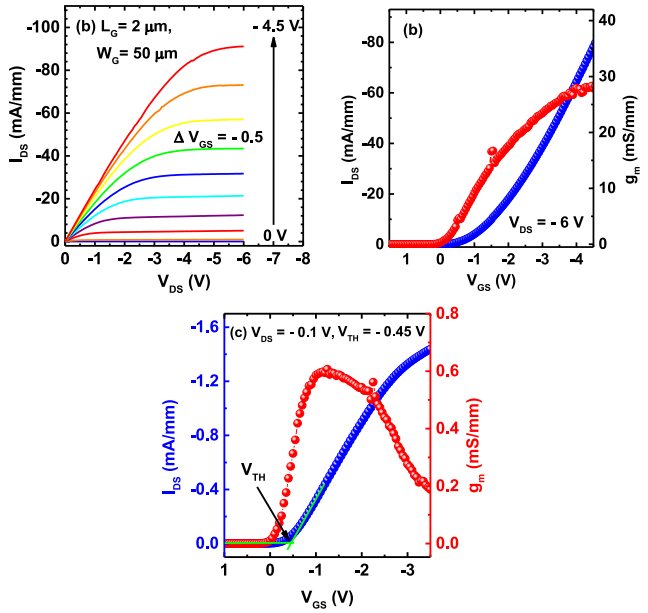

FIGURE 6. **(a) Output characteristics and (b) transfer characteristics of the 2-μm Al/alumina/H-diamond MOSFET without UV ozone treatment. (c) Transfer characteristics at $V_{DS} = -0.1$ V.**

by the existence of positive mobile ions in the dielectric. The maximum oxide capacitance is extracted to be 0.497 μF/cm^2 by using Vincent method (Fig. 5(c)) [21], [22]. Based on the thickness of 5.0 nm of the alumina layer, the permittivity is calculated to be 2.7, which is at the same level with the results of Wang *et al.* [15] and Hirama *et al.* [18]. However, this value is lower than the reported value of 6∼9 [23]–[25]. The alumina in this study is formed by oxidizing aluminum at low temperature on hotplate in the air. Thus, the quality of the alumina is not at the same level with those prepared by atomic layer deposition (ALD) or plasma enhanced chemical vapor deposition (PECVD). There could be many defects and voids in the film, which could induce the low value of the permittivity. The results of gate capacitance dependent on gate area are summarized in Fig. 5(d). The capacitance is fundamentally proportional to the gate area, which indicates that the carriers uniformly distributed under the gate electrode.

To investigate that the normally-off MOS channel benefits more from the UV ozone treatment or from the annealing during alumina formation, we also fabricate the control MOSFET on another lab-grown SCD by the same device process except that no UV ozone treatment was performed. The output and transfer characteristics are shown in Fig. 6. The device shows an I_D of −86.3 mA/mm at $V_{GS} = V_{DS} = -4.5$ V. The extracted V_{TH} is −0.45 V (fig. 6(c)). Thus, the device is also in the normally-off operation mode. However, its $|V_{TH}|$ is lower than those of both our UV ozone treated devices and the device with 180 °C oxidized alumina [15]. Therefore, the positive charges in the alumina layer do contribute to the achievement of normally-off MOS channel, and UV ozone treatment induces the further increase of $|V_{TH}|$.

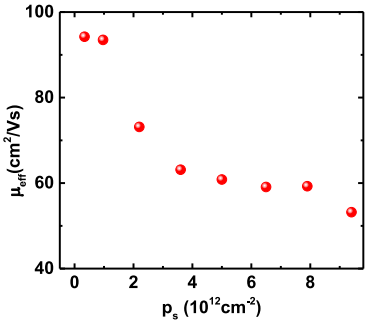

FIGURE 7. **Effective mobility μ_{eff} of the 40 μm normally-off H-diamond MOSFET as a function of hole density.**

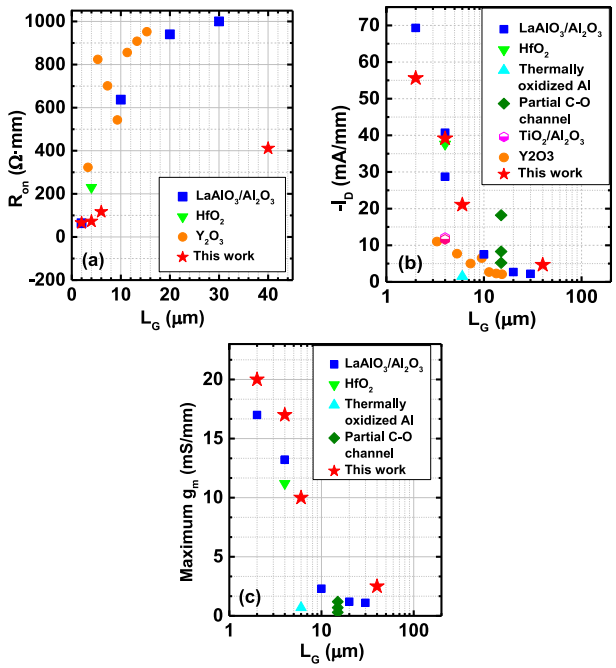

FIGURE 8. **(a) R_{on} and (b) $-I_D$ and (c) maximum g_m of reported normally-off H-diamond MOSFETs dependent on the gate length. The gate dielectric or the type of the channel is given.**

In order to further understand the hole transport properties, we extracted the effective mobility (μ_{eff}) from the combination of the R_{on} vs. V_{GS} relation and C-V characteristics of the device with the gate length of 40 μm. The hole density (p_s) is obtained by $\int C_{GS} dV_{GS}$ and the maximum value reaches 9.4×10^{12} cm^{-2} at $V_{GS} = -4.5$ V. Fig. 7 shows the μ_{eff} vs. p_s relation. The maximum μ_{eff} is 94.2 cm^2/V·s. Compared to reported results of H-diamond normally-off MOSFET with other dielectrics, only the reported mobility of the device with $LaAlO_3$/ALD-Al_2O_3 gate dielectrics (65∼104 cm^2/Vs) [10] is a little higher than our results. The high mobility of the channel carrier contributes heavily to the achievement of the high performance of our devices. In addition, it should be note that μ_{eff} is almost a constant of 60 cm^2/V·s for -4 V $< V_{GS} < -2$ V, which contributes to the continuous increasing of g_m.

Fig. 8 summarized the recently reported L_G-dependent device parameters of normally-off H-diamond MOSFETs with different gate dielectric or fabrication processes as we know [5], [9]–[15]. In the L_G range of 2∼40 μm, our devices show the record high g_m, and almost the lowest R_{on} except that for the 2-μm case (slightly higher than 63.5 Ω· mm of $LaAlO_3/Al2O_3$/H-diamond MOSFET [9]), and secondary largest $|I_D|$ for $L_G \leq 4$ μm. Further optimization of our normally-off devices and the passivation of the device for high temperature application will be carried out in the near future.

IV. CONCLUSION

The high-performance normally-off H-diamond MOSFETs have been achieved on the SCD grown in our lab by adopting UV ozone treated channel and the alumina dielectric prepared by thermal oxidation of aluminum film. The device with a 2-μm gate has a V_{TH} of −1.0 V and shows record high g_m of 20 mS/mm at $V_{DS} = -6$ V, and an I_D of 51.6 mA/mm at $V_{GS} = V_{DS} = -4.5$ V and R_{on} of 65.39 Ω· mm. It was found that it was the UV ozone treatment and the positive charges in the alumina together induce the formation of normally-off channel, and UV ozone treatment is more important to increasing the value of $|V_{TH}|$. The high g_m and low R_{on} of the devices benefit from the short time and mild property of both normally-off channel processes. In addition, the hole mobility extracted from the combination of C-V and I-V curves shows that the carrier mobility is almost a constant in the gate voltage range of -4 V $< V_{GS} < -2$ V, which contributes to the successive increasing of g_m with the increasing of V_{GS}. Optimization of the device process and structure will be our future work.

ACKNOWLEDGMENT

The authors would like to thank Beijing NAURA Microelectronics Equipment Co., Ltd. for experiments and discussions.

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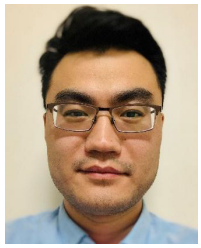

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