Electrical Properties of Vertical InAs/InGaAs Heterostructure MOSFETs

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ABSTRACT Vertical InAs/InGaAs nanowire MOSFETs are fabricated in a gate-last fabrication process, which allows gate-lengths down to 25 nm and accurate gate-alignment. These devices demonstrate high performance with transconductance of 2.4 mS/μm, high on-current, and off-current below 1 nA/μm. An in-depth analysis of the heterostructure MOSFETs are obtained by systematically varying the gate-length and gate location. Further analysis is done by using virtual source modeling. The injection velocities and transistor metrics are correlated with a quasi-ballistic 1-D MOSFET model. Based on our analysis, the observed performance improvements are related to the optimized gate-length, high injection velocity due to asymmetric scattering, and low access resistance.

INDEX TERMS Vertical, nanowire, InAs, InGaAs, MOSFET, heterostructure.

I. INTRODUCTION

Vertical MOSFETSs are considered to improve the device performance at the 5 nm node and beyond. The main benefit of the vertical design is the possibility to decouple gate-length and contact length from the footprint, therefore improving the packing density [1]. The main focus on vertical MOSFETs have been on III-V transistors, as there is no known process to introduce strain on vertical MOSFETs, which is necessary for Si transistors. For vertical III-V nanowire MOSFET both top-down and bottom-up approaches have been investigated.

Bottom-up vertical vapor-liquid-solid (VLS) nanowires are an interesting option, as they are not restricted by lattice matching, therefore III-V nanowires can easily be integrated on Si and axial/radial heterostructures can be fabricated. Radial heterostructure offer an excellent way for modulation doping while axial heterostructure allows method for bandgap engineering, hence offering a way for reduction of parasitic effects such as band-to-band tunneling. The vertical design further allows easy fabrication of the gate-all-around (GAA) structure, which allows thicker body devices at the same gate-length compared to the other gate-structures due to the improved electrostatics, hence reducing the surface scattering [2], [3]. All of these properties are of interest for the digital transistor, but they are also interesting options for high-speed transistors. Possibility for thicker body devices and heterostructures will reduce on-resistance (R_{on}) and improve intrinsic voltage gain ($g_{\mathrm{m}}/g_{\mathrm{d}}$), which are important metrics for high-speed devices.

Recently, high-performance vertical III-V nanowire MOSFETs have been presented [4]–[7]. Vertical InAs/InGaAs heterostructure MOSFETs in particular have shown record-high on-performance in vertical nanowire MOSFETs, low off-current, and improved breakdown voltage [4], [7]. Improvements have mainly been attributed to the suppressed band-to-band tunneling due to a wider band-gap material on the drain side and scaled gate-length. In this paper, the concept is explained more exhaustively and origin of improvement are discussed. We present in-depth analysis using DC and RF-measurements. In this experiment; the gate-length, gate-location and spacer thickness are varied. The device data is interpreted using a virtual source model [8]. We show that the on-performance of these MOSFETs can be attributed to InAs MOSFETs, while lower off-current is achieved with the InGaAs drain. The device ballisticity and origin of the access resistances are analyzed. The access resistance is further analyzed by cold FET measurement. We also show that the empirical
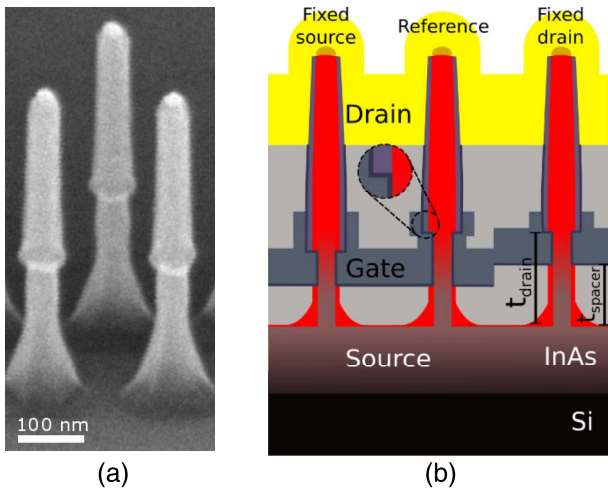
FIGURE 1. An SEM picture of the device after the fabrication of source and drain contacts (a), and schematic illustration of the vertical MOSFET structure (b). In the illustration two different gate alignments and the reference are shown.

Virtual Source compact model [8] originally constructed for modeling 2D MOSFETs work well with the nanowire FETs, and give estimates for the injection velocity.

II. DEVICE FABRICATION

Scanning electron micrograph (SEM) and a schematic illustration of the fabrication are shown in figure 1. The devices are fabricated on p-type Si substrate. At the first step, 300-nm-thick InAs source contact is grown by Metalorganic Vapor Phase Epitaxy (MOVPE). Vertical nanowires are grown using seed-particle vapor-liquid-solid (VLS) growth in MOVPE. The growth includes three steps: 1) a 100-nm-long unintentionally doped InAs segment; 2) a 100-nm-long unintentionally doped graded segment from InAs to $In_{0.5}Ga_{0.5}As$; and 3) a 300-nm-long highly doped $In_{0.5}Ga_{0.5}As$ segment. At the last growth step, the III/V-ratio is increased, therefore n^+-InGaAs overgrows the unintentionally doped bottom segments and forms a highly doped foot, as shown in figure 1a, which reduces the access resistance at the source side. A more detailed material analysis of a similar structure has been presented in [9].

In the next step, the drain contact is fabricated; the fabrication is started by spin coating 400-nm-thick hydrogen silsesquioxane (HSQ). The thickness of the HSQ is then defined using electron beam lithography (EBL) [10]. The drain contact is fabricated by sputtering 20 nm Mo and ALD depositing 3 nm TiN. The metal layer is anisotropically dry etched and the HSQ layer is removed, leaving metal only on the sidewalls. The device structure after drain and source contact fabrication is shown in figure 1a.

A HSQ bottom spacer is applied by spin coating and the thickness is defined by EBL, leaving a predefined opening between the top metal contact and bottom HSQ spacer. This opening defines the effective gate length, and allows a local thinning of the channel by digital etching. The digital etching

is done by oxidizing the nanowire surface in O_3 and removing the oxide by HCl. The etching is repeated until the highly doped shell is removed from the channel region. The process is followed by ALD deposition of bilayer Al_2O_3/HfO_2. 1-nm-thick Al_2O_3 is deposited at 300 °C and 4-nm-thick HfO_2 is deposited at 120 °C that results approximately in an EOT = 1.5 nm. The gate is formed by sputtering of 60-nm-thick W gate. The device is finalized by S1813 spacer definition and deposition of Ni/Au (15 nm/150 nm) contacts for measurements.

The definition of the drain-substrate distance (t_{drain}) and bottom spacer thickness (t_{spacer}) by HSQ in two steps allows different gate alignment on the same sample. In figure 1b, two different gate-alignments and reference structure are shown. In the reference, the bottom spacer is aligned with the overgrown foot (t_{spacer} = 120 nm) and the drain metal is aligned with the grading (t_{drain} = 200 nm). In fixed source, the bottom spacer is fixed at t_{spacer} = 120 nm and t_{drain} is varied. In fixed drain, the drain is fixed at t_{drain} = 200 nm and t_{spacer} is varied. This variation allows systematic investigation of the asymmetric transistor behavior.

III. DC CHARACTERIZATION

Transfer characteristics and output characteristics of a device with L_g = 70 nm and diameter 27 nm are shown in figure 2. The device is an array of 120 nanowires and the source is fixed at t_{spacer} = 120 nm. The device exhibits good on- and off-states, with g_m = 1.9 mS/μm, SS_{sat} = 85 mV/dec and I_{on} = 407 μA/μm at I_{off} = 100 nA/μm and V_{dd} = 0.5 V. All of the metrics are normalized by nanowire circumference and the dimensions are measured by SEM. In figure 2b, the output characteristics of the device is shown, a low R_{on} = 450 Ωμm is achieved while still maintaining good saturation.

The device characteristics are modeled by the physics based empirical virtual source (VS) model. The modeling follows the guidelines from [8]. The model fit is shown by the black solid line in figure 2. The model has three main fitting parameters: injection velocity (v_{inj}), low-field mobility
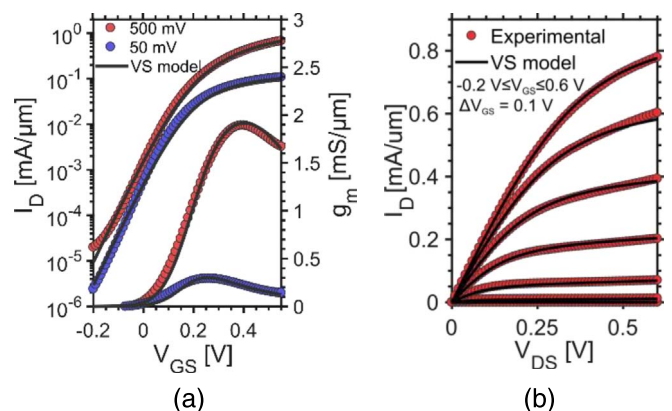
FIGURE 2. (a) Transfer characteristics at V_{DS} = 500 mV and V_{DS} = 50 mV. The device has L_g = 70 nm and diameter 27 nm. (b) Output characteristics from the same device. Black solid line in both of the figures represent the fitted virtual source model.
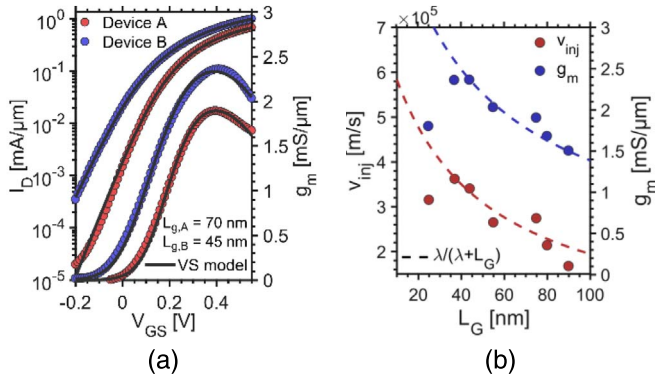
FIGURE 3. (a) Transfer characteristics at $V_{DS} = 0.5$ V of the two devices, device A and device B. Device A has $L_g = 70$ nm and device B has $L_g = 45$ nm. (b) Effect of gate-length scaling on v_{inj} and g_m. Dashed lines represent fitted transmission $T = \lambda/(\lambda + L_G)$.

and access resistances [8]. The device current in saturation is described by a formula

$$I_D/W = Q_{x0}v_{inj}, \tag{1}$$

where W is the gate-width, v_{inj} is the velocity at the virtual source and Q_{x0} is the charge density at the virtual source. The charge density is approximated with an empirical function and the total gate capacitance (C_{tot}) [8], and in simplified form in saturation can be given by $Q_{x0} = C_{tot}(V_{gs} - V_T - \delta V_{DS})$, where δ is the DIBL. In the modeling, the total gate capacitance C_{tot} is estimated from reference diode measurement, as the direct measurement for C_{tot} is difficult in vertical MOSFETs due to the parasitic capacitances. In this work a constant $C_{tot} = 1 \pm 0.2$ aF/nm per nanowire was used based on the previous vertical nanowire MOS capacitor measurements with similar gate-stack [11]. The simple expression will thus give a rough estimate of the mean injection velocity.

In figure 2a, good fit to the 50 mV and 500 mV data is achieved with DIBL = 90 mV/V. To further obtain a good fit from the VS model, substantially larger drain resistance is needed ($R_d \approx 5R_s$). The estimated source resistance ($R_s = 60 \pm 25\,\Omega\mu$m) is comparable to the resistance in the state-of-the-art lateral devices [12] and confirms that good contacts can be achieved also on vertical MOSFETs. The low R_s is attributed to a large overgrowth at the foot of the nanowire as shown in figure 1a. The origin of the highly asymmetric access resistance and confirmation for the magnitude of the resistance is discussed later in the paper. From the fitting, injection velocity of $2.7 \cdot 10^7$ cm/s is obtained.

To demonstrate fitting and the effect of gate-length scaling, transfer characteristics from two different devices, device A and device B, are shown in figure 3a. The device A is the same as in figure 2 and device B is an array with the highest g_m. In both of the devices source is fixed at $t_{spacer} = 120$ nm. Device B is an array of 144 nanowires with an average diameter 26 nm and $L_g = 45$ nm. The device has

$g_m = 2.4$ mS/μm and $SS_{sat} = 140$ mV/dec. Scaling the gate-length degrades the electrostatics and therefore 100 nA/μm limit is not achieved with the device B. However, substantial improvement in g_m is achieved. The improvement is due to improved transmission $v_{inj} = 3.4 \cdot 10^7$ cm/s and $R_{on} = 410\,\Omega\mu$m for the device B.

Similar fitting was achieved for seven devices that had gate length ranging from 25 to 90 nm. The gate on these devices was aligned with the foot (fixed source), therefore the bottom spacer thickness was 120 nm and the scaling was done by moving the top metal. Gate-length scaling of v_{inj} and g_m are presented in figure 3b. These devices can be considered to operate in the quasi-ballistic regime, where $g_m \approx T \cdot g_{m,ballistic}$ and the transmission (T) is approximately $T = \lambda/(\lambda + L_G)$, where λ is the mean-free-path. Fitting of T to the experimental data is shown in figure 3b, where $\lambda = 35 \pm 15$ nm. This will give approximately 45% transmission at $L_G = 45$ nm.

The injection velocity, presented in figure 3b, can similarly be related to the ballistic injection velocity. In 1-D ballistic MOSFETs, the injection velocity at high drain bias, when a single sub-band is assumed can be modeled by

$$v_{inj,max} = v_t \frac{F_0(\eta_F)}{F_{-\frac{1}{2}}(\eta_F)}, \tag{2}$$

where $v_t = \sqrt{2k_BT/\pi m^*}$ is the thermal velocity, F_n is nth order Fermi-Dirac integral, and $\eta_F = (E_F - \in (0))/k_BT$ [13]. Using this formula, $v_{inj,max} = 8.5 \cdot 10^7$ cm/s can be derived from 1-D single sub-band model with EOT = 1.5 nm and $m^* = 0.031 m_e$ (based on non-parabolic band structure approximation [2]). When multiple sub-bands are added, the velocity goes slightly down under similar biasing conditions ($v_{inj,max} = 7.5 \cdot 10^7$ cm/s at $V_{ov} = 0.3$ V), which is due to decreased degeneracy. Notably, 45% ballisticity can be derived ($v_{inj}/v_{inj,max} = 3.4/7.5 = 45\%$) in agreement with $v_{inj} = T \cdot v_{inj,max}$, as shown in figure 3a. Previously, similar injection velocity values have been presented for InAs HEMTs [14] and InAs MOSFETs [15]. The drop in injection velocity for devices with $L_G < 45$ nm is an artifact from the VS model, which with a constant C_{tot} does not correctly model strong short channel effects. For well-behaved devices, a reasonable prediction of L_G scaling can be achieved by changing v_{inj} with the transmission.

One of the main benefits of the heterostructure channel is asymmetric scattering, as the transmission is dependent on scattering in the channel. In figure 4b band diagram of the heterostructure is presented. If the scattering happens close to the source, the carrier has high probability to return to the source. The probability decreases drastically, when the scattering happens closer to the high-field region. In our MOSFETs, the scattering on the drain side is expected to be larger due to increased effective mass ($m^*_{InAs} < m^*_{InGaAs}$), which is beneficial, as it is not as detrimental for the performance. This asymmetric scattering can be observed in figure 4a, where a device with 120 nanowires, a diameter 27 nm and $L_G = 80$ nm is
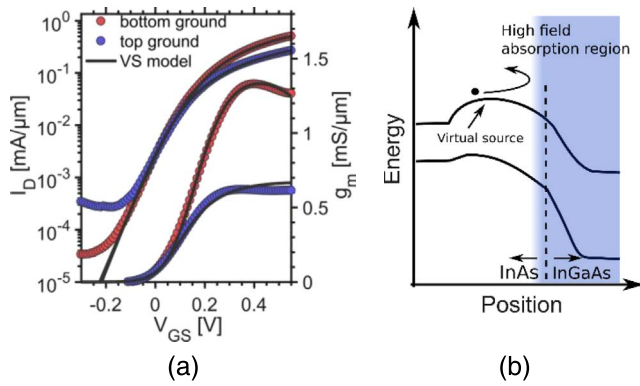
FIGURE 4. (a) Transfer characteristics of the device (L_G = 80 nm, 120 NWs and d = 27 nm) biased in two different configurations. Black solid line represents fitted virtual source model. (b) Band diagram describing expected heterostructure.

FIGURE 5. Minimum off-current at different gate-lengths is shown in (a). Off-current stabilizes below 100 nA/μm at L_G > 50 nm. Linear fit in R_{on} versus L_G plot (b) gives R_{access} = 300 Ωμm. Inset in (b) shows average on-resistance as a function spacer thickness.

biased in two different directions, drain at the top (bottom grounded) and drain at the bottom (top grounded). In the top grounded configuration g_m is substantially lower, which cannot be explained by asymmetric access resistance only. From the virtual source model, where the difference in access resistance is included, $v_{inj,tg} = 0.87 \cdot 10^7$ cm/s in the top grounded configuration and $v_{inj,bg} = 1.5 \cdot 10^7$ cm/s for bottom grounded. This large difference in injection velocities can be explained by increased scattering in the InGaAs as compared to InAs, as based on equation (2) $v_{inj} \sim 1/\sqrt{m^*}$. The ratio $v_{inj,bg}/v_{inj,tg} = 1.7$ is slightly larger than expected based on InAs and $In_{0.5}Ga_{0.5}As$ effective masses. The difference can be explained by increased scattering due to reduced material quality in InGaAs and the introduction of doping.

Another noticeable difference in figure 4a is the lower off-current in the bottom grounded configuration. The difference is attributed to the difference in band-gap on the drain side. In the bottom ground configuration, the drain material is InGaAs, therefore band-to-band tunneling is suppressed as compared to InAs. This difference is more clearly seen in figure 5a, where the minimum off-current of fixed drain devices with drain on InGaAs (t_{drain} = 200 nm) and drain on the graded segment (t_{drain} = 170 nm) are shown. When the drain is on the graded InGaAs segment, off-current seems to stabilize at 10 nA/μm, while it is placed on the InGaAs segment the off-current of 1 nA/μm limit is achieved. The off-current difference is attributed band-to-band tunneling on the drain side [9], [16], [17] augmented by parasitic bipolar effect. The gate-length dependence of this effect is attributed in part to the gate-length dependent electron-hole recombination in the channel [16]. The steep increase in the off-current at the shortest gate-length can also partly be due to the electrostatics. The natural length scale (λ_n) gives a measure for short-channel effects [2], [3]. For these devices λ_n is between 8 to 9.5 nm depending on the device diameter. Good electrostatics is maintained, when $L_G > 5\lambda_n$. The same effect also explains the drop in g_m at $L_g < 35$ nm in figure 3b.
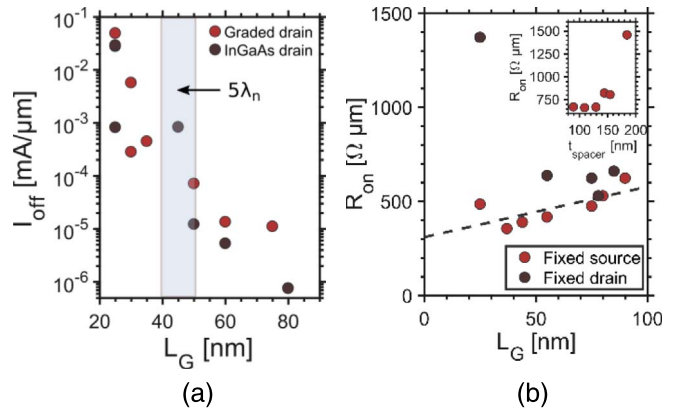
In figure 5b, R_{on} versus L_g for the devices with highest performance are shown. The devices are divided in two different groups, fixed source and fixed drain devices, as shown in figure 1b. The fixed source devices follow the expected trend and $R_{access} = 300 \pm 50$ Ωμm can be derived. For the fixed drain devices, the R_{on} increases with the decreasing L_g at short gate lengths. This increase happens when the bottom spacer is thicker than the foot height, therefore increasing the resistance on the source side. This can be seen more clearly in the inset of figure 5b, where the average R_{on} for devices versus spacer thickness (t_{spacer}) is shown. The height of the overgrown foot is approximately 130 nm and as can be seen from the figure, R_{on} starts to increase at $t_{spacer} >$ 130 nm. Therefore, for these devices it is essential to align the gate with the highly doped foot.

To further highlight the material quality of the VLS grown nanowires, in figure 6 the devices are benchmarked against other state-of-the-art III-V MOSFETs on Si. In the figure, I_{on} at $I_{off} = 100$ nA/μm and g_m are plotted against the gate-length. All of the devices are measured at $V_{DS} = 0.5$ V. Our devices are nanowire arrays, which averages out the performance. Our VLS grown nanowire MOSFETs have the highest I_{on} as well the highest g_m. High g_m values are especially encouraging for the integration of high-frequency MOSFETs on Si.

IV. RF MEASUREMENTS
To further validate the resistances from independent measurements and to characterize the extrinsic properties of our transistors, Cold FET [18] S-parameter measurements up to 67 GHz were performed. In the measurements, a high-frequency compatible design was used [19]. The devices were fabricated from similar nanowires as the DC transistors, but with different drain structure and gate-fingers. Contact pads were de-embedded by open/short structures. The difference on the drain structure and the process variability increased the total on-resistance. The measurements were performed to get confirmation on the access resistance.
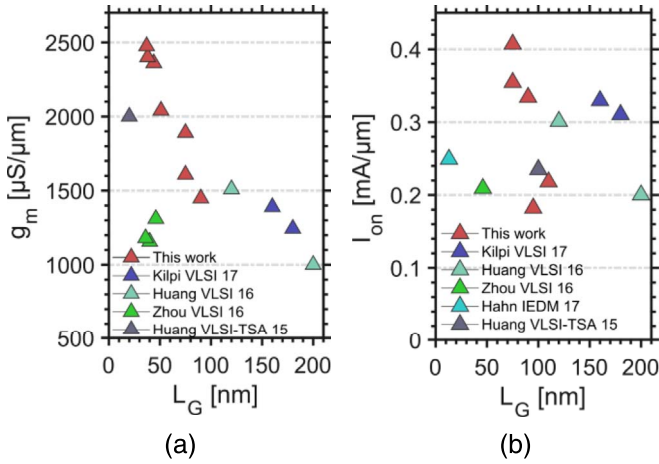
FIGURE 6. Benchmarking (a) g_m and (b) I_{on} at I_{off} = 100 nA/μm against state-of-the art III-V MOSFETs on Si [7], [17], [20]-[22]. All the metrics are taken at V_{DS} = 0.5 V.
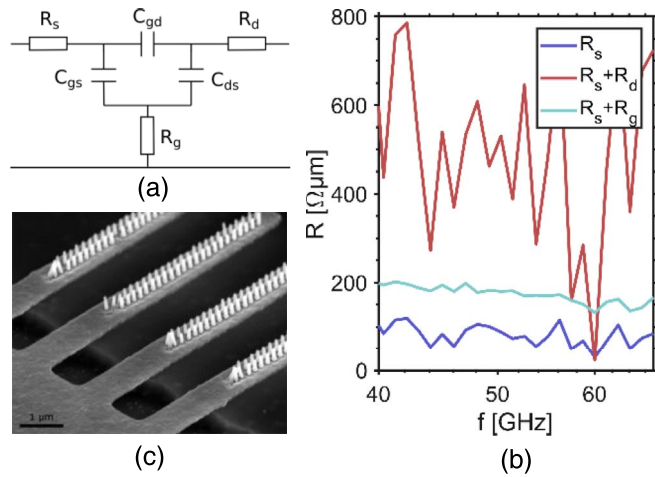
FIGURE 7. (a) Equivalent circuit of the MOSFET in off-state. (b) Cold-FET measurement results confirm low R_s = 75 ± 35Ωμm. (c) Finger-gate structure used in high-frequency compatible design.

The transistor was biased at V_{DS} = 0 V and V_{GS} = −0.2 V to measure the access resistance. The equivalent circuit in the off-state and the finger gate design are shown in figure 7a,c. From the equivalent circuit, at the high frequency, access resistances can be extracted by using the z-parameters:

$$R_s = Re(z_{12}) = Re(z_{21}), \qquad (3)$$

$$R_d = Re(z_{22}) - R_s. \qquad (4)$$

The extracted values are shown in figure 7b. The determined resistance values are fairly constant starting at 40 GHz for R_s and R_g. The source resistance is estimated R_s = 75 ± 35Ωμm, which is similar as what was extracted with the VS model, confirming the determined values. The drain resistance on the RF sample is considerably higher than DC-devices, which is attributed to the process variability and RF-compatible design.

V. CONCLUSION

Vertical heterostructure InAs/InGaAs MOSFETs with high performance are demonstrated. The device characteristics are modeled by virtual source model with a very high accuracy and the magnitude of the injection velocity and access resistances are determined. Injection velocity is compared to the ballistic model showing approximately 45% ballisticity. Effect of heterostructure and gate-alignment are more thoroughly discussed demonstrating the benefit of a low effective mass segment (InAs) on the source side for efficient injection and a wider band gap material on the drain side to limit parasitic effects.

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